TP65H480G4JSG

650V SuperGaN® GaN FET in PQFN 5 x 6 Performance Package (source tab)

Description

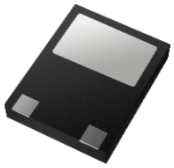
The TP65H480G4JSG 650V, 480mΩ Gallium Nitride (GaN) FET is a normally-off device using Renesas' Gen IV platform. It combines a state-of-the-art high voltage GaN HEMT with a low-voltage silicon MOSFET to offer superior reliability and performance while enabling reduced system size and cost.

The Gen IV SuperGaN® platform uses advanced epi and patented design technologies to simplify manufacturability while improving efficiency over silicon via lower gate charge, output capacitance, crossover loss, and reverse recovery charge.

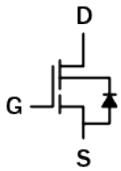
Benefits

- Achieves increased efficiency in both hard- and soft-switched circuits
  - Increased power density
  - Reduced system size and weight
  - Overall lower system cost
- Easy to drive with commonly used gate drivers

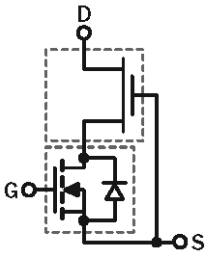
Product/Schematic Diagrams



TP65H480G4JSG PQFN 5x6 PP



Cascode Schematic Symbol



Cascode Device Structure

(MOSFET has integrated ESD Protection Circuit)

Features

- Gen IV technology
- JEDEC-qualified GaN technology
- Dynamic R_{DS}(on)eff production tested
- Robust design, defined by
  - Transient over-voltage capability
  - Operation with E-mode Gate drivers without need for Zener protection
- Negligible Qrr
- Reduced crossover loss
- RoHS compliant and Halogen-free packaging
- 2kV HBM ESD rating

Applications

- Consumer
- Power adapters
- Low power SMPS
- Lighting

Key Specifications

V_{DS} (V)	650
$V_{DSS(TR)}$(V)	800
$R_{DS(on)}$ (mΩ) maximum [1]	560
Q_{OSS} (nC) typical	9.2
Q_G (nC) typical	5.2

1. Dynamic RDS(on); see Figure 17 and Figure 18.

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1. Pin Information

1.1 Pin Assignments

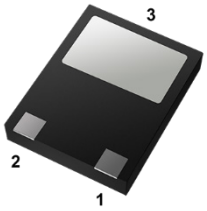


Figure 1. Pin Assignments – Bottom View

1.2 Pin Descriptions

Pin Number	Pin Name	Description
1	G	Gate.
2	D	Drain.
3	S	Source.

2. Specifications

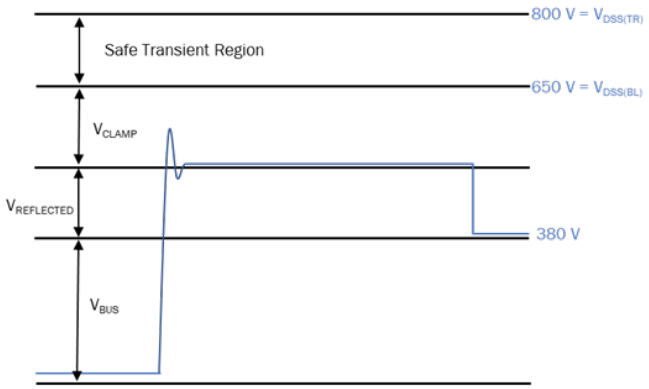
2.1 Absolute Maximum Ratings

(T_c = 25°C unless otherwise stated.)

Caution: Do not operate at or near the maximum ratings listed for extended periods of time. Exposure to such conditions can adversely impact product reliability and result in failures not covered by warranty.

Symbol	Parameter	Minimum	Maximum	Unit
V_{DSS}	Drain to source voltage (T_J = -55°C to 150°C)	-	650	V
$V_{DSS(TR)\ ,\ non\text{-}repetitive}$	Transient drain to source voltage, non-repetitive [1]	-	800	
$V_{DSS(TR)\ ,\ repetitive}$	Transient drain to source voltage, repetitive [2]	-	750	
V_{GSS}	Gate to source voltage	-20	+20	
P_D	Maximum power dissipation at T_C = 25°C	-	25	W
I_D	Continuous drain current at T_C = 25°C	-	5	A
	Continuous drain current at T_C = 100°C	-	3.1	A
I_{DM}	Pulsed drain current (pulse width: 10µs)	-	16	A
T_J	Junction operating temperature	-55	+150	°C
T_S	Storage temperature	-55	+150	°C
T_{SOLD}	Reflow soldering temperature [3]	-	260	°C

1. In off-state, spike duration < 30µs, non-repetitive.
2. Off-state, spike duration < 5µs.
3. Reflow MSL3.



Primary Switch Voltage Stress (264 V AC)

2.2 Thermal Specifications

Symbol	Condition	Typical Value	Unit
$R_{\Theta JC}$	Junction-to-case	5	°C/W
$R_{\Theta JA}$	Junction-to-ambient [1]	50	

1. Device on one layer epoxy PCB for source connection (vertical and without air stream cooling, with 6cm² copper area and 70µm thickness).

2.3 Electrical Specifications – Forward Device

T_J = 25°C unless otherwise stated.

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Unit
$V_{DSS(BL)}$	Maximum drain-source voltage	V_{GS} = 0V	650	-	-	V
$V_{GS(th)}$	Gate threshold voltage	V_{DS} = V_{GS}, I_D = 0.5mA	1.5	2.0	2.5	V
$\Delta V_{GS(th)}/T_J$	Gate threshold voltage temperature coefficient		-	-5.8	-	mV/°C
$R_{DS(on)eff}$	Drain-source on-resistance [1]	V_{GS} = 6V, I_D = 3A	-	480	560	mΩ
		V_{GS} = 6V, I_D = 3A, T_J = 150°C	-	1000	-	
I_{DSS}	Drain-to-source leakage current	V_{DS} = 650V, V_{GS} = 0V	-	1	10	μA
		V_{DS} = 650V, V_{GS} = 0V, T_J = 150°C	-	5	-	
I_{GSS}	Gate-to-source forward leakage current [2]	V_{GS} = 20V	-	-	10	μA
	Gate-to-source reverse leakage current [2]	V_{GS} = -20V	-	-	-10	
I_{GSS}	Gate-to-source forward leakage current [2]	V_{GS} = 6V	-	-	0.1	μA
	Gate-to-source reverse leakage current [2]	V_{GS} = -6V	-	-	-0.1	
C_{ISS}	Input capacitance	V_{GS} = 0V, V_{DS} = 400V, *f* = 1MHz	-	465	-	pF
C_{OSS}	Output capacitance		-	8	-	
C_{RSS}	Reverse transfer capacitance		-	1.2	-	
$C_{O(er)}$	Output capacitance, energy related [3]	V_{GS} = 0V, V_{DS} = 0V to 400V	-	11.6	-	pF
$C_{O(tr)}$	Output capacitance, time related [4]		-	23	-	
Q_G	Total gate charge	V_{DS} = 400V, V_{GS} = 0V to 6V, I_D = 3A	-	5.2	-	nC
Q_{GS}	Gate-source charge		-	1.3	-	
Q_{GD}	Gate-drain charge		-	2.1	-	
Q_{OSS}	Output charge	V_{GS} = 0V, V_{DS} = 0V to 400V	-	9.2	-	nC
$t_{D(on)}$	Turn-on delay	V_{DS} = 400V, V_{GS} = 0V to 6V, I_D = 3A, RG = 20Ω, ZFB = 120Ω at 100MHz (see Figure 15)	-	23.2	-	ns
t_R	Rise time		-	3	-	
$t_{D(off)}$	Turn-off delay		-	53.6	-	
t_F	Fall time		-	10	-	

1. Dynamic $R_{DS(on)}$, 100% tested; see Figure 17 and Figure 18 for conditions.
2. Including leakage current of the integrated ESD protection circuit.
3. Equivalent capacitance to give same stored energy from 0V to 400V.
4. Equivalent capacitance to give same charging time from 0V to 400V.

2.4 Electrical Specifications – Reverse Device

T_J = 25°C unless otherwise stated.

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Unit
I_S	Reverse current	V_{GS} = 0V, T_C = 100°C, ≤25% duty cycle	-	-	3.1	A
V_{SD}	Reverse voltage [1]	V_{GS} = 0V, I_S = 1.3A	-	1.3	-	V
		V_{GS} = 0V, I_S = 2.6A	-	1.8	-	

1. Includes dynamic $R_{DS(on)}$ effect.

Note: Reverse recovery charge is negligible, enabled by the LV Si FET technology

3. Typical Performance Graphs

T_C = 25°C unless otherwise stated.

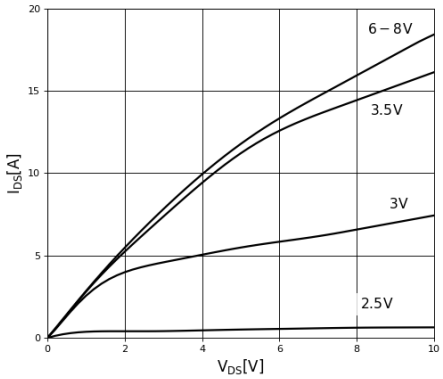


Figure 2. Typical Output Characteristics, T_J = 25°C

Parameter: V_{GS}

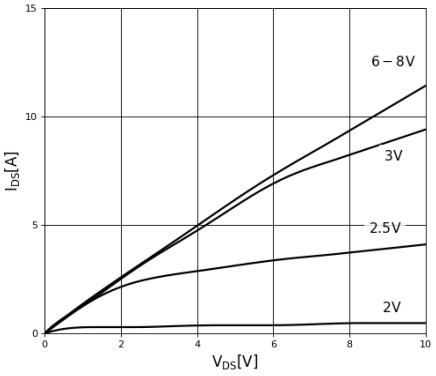


Figure 3. Typical Output Characteristics, T_J = 150°C

Parameter: V_{GS}

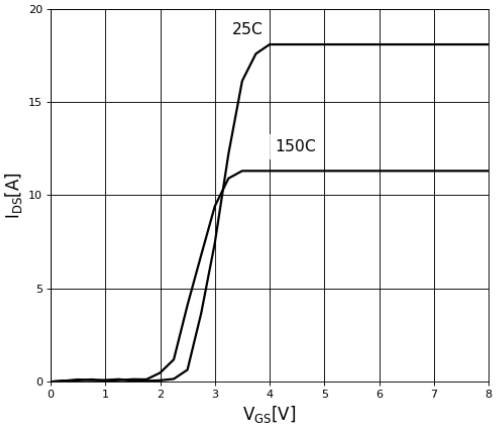


Figure 4. Typical Transfer Characteristics

V_{DS} = 10V, parameter: T_J

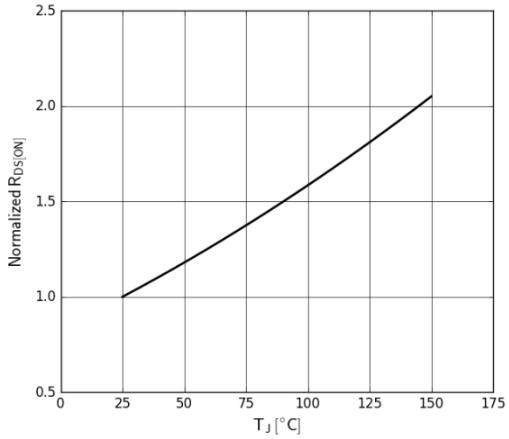


Figure 5. Normalized On-resistance

I_D = 3A, V_{GS} = 6V

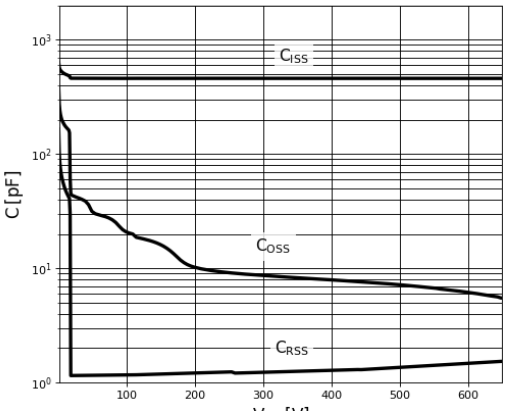


Figure 6. Typical Capacitance

V_{GS} = 0V, f = 1MHz

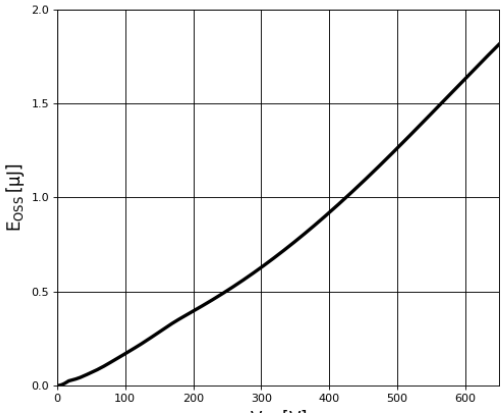


Figure 7. Typical C_{OSS} Stored Energy

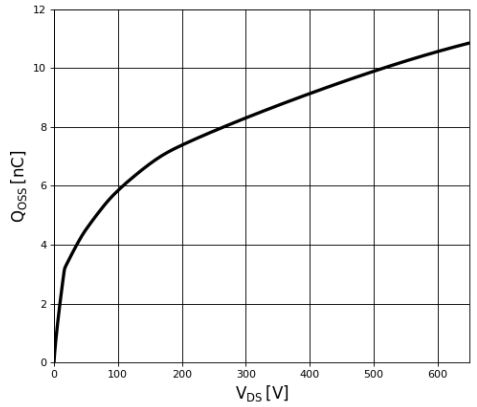


Figure 8. Typical Q_{OSS}

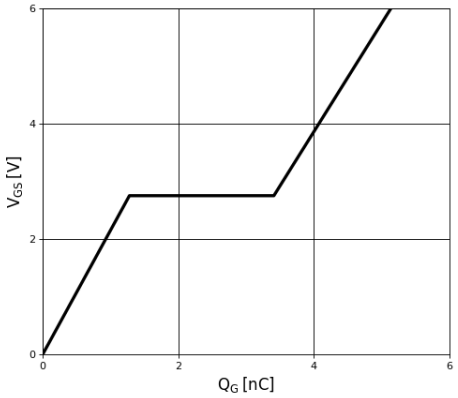


Figure 9. Typical Gate Charge

I_{DS} = 3A, V_{DS} = 400V

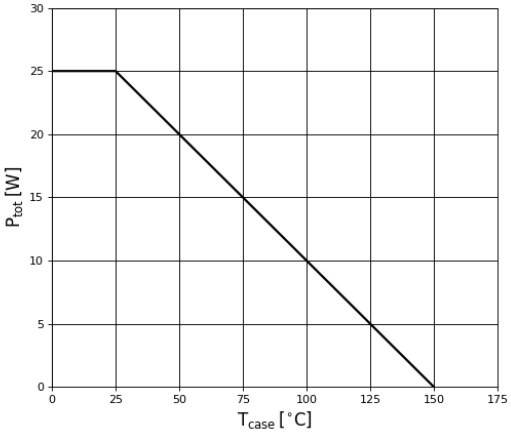


Figure 10. Power Dissipation

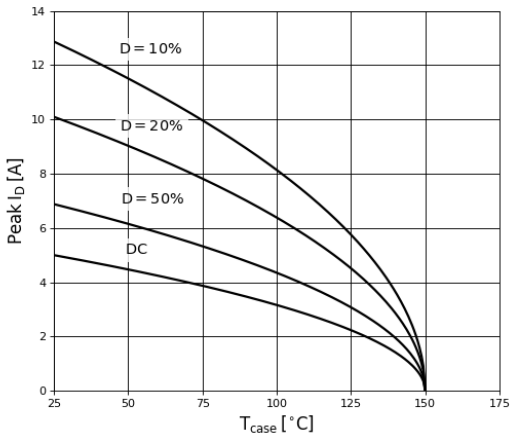


Figure 11. Current Derating

Pulse width ⩽ 10µs, V_{GS} ⩾ 6V

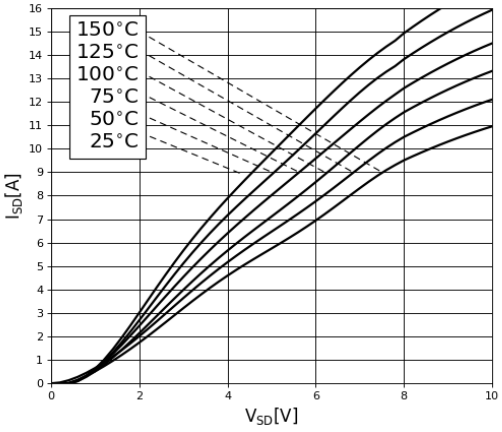


Figure 12. Forward Characteristics of Rev. Diode

$I_S = f_{(VSD)}$, parameter: T_J

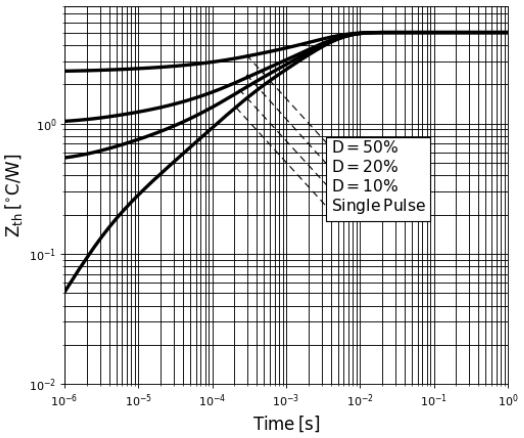


Figure 13. Transient Thermal Resistance

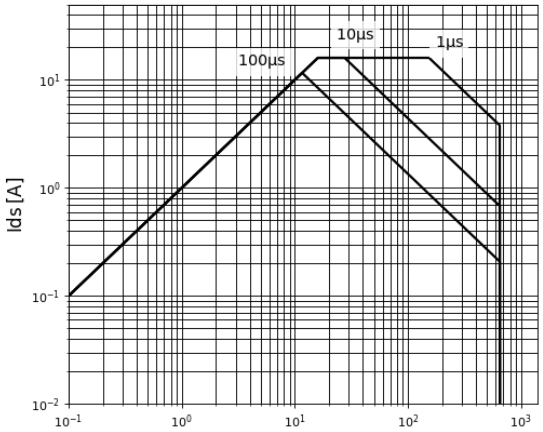


Figure 14. Safe Operating Area T_C = 25°C

4. Test Circuits and Waveforms

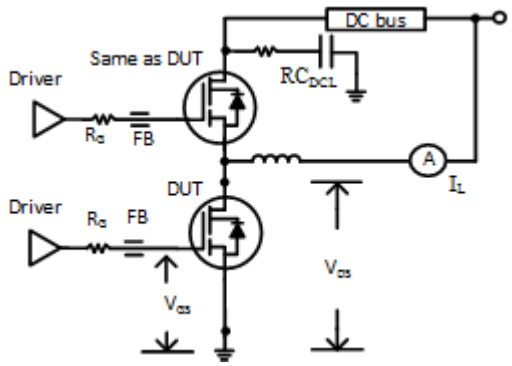


Figure 15. Switching Time Test Circuit

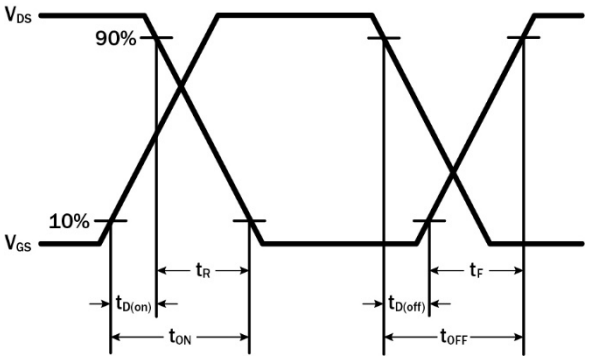


Figure 16. Switching Time Waveform

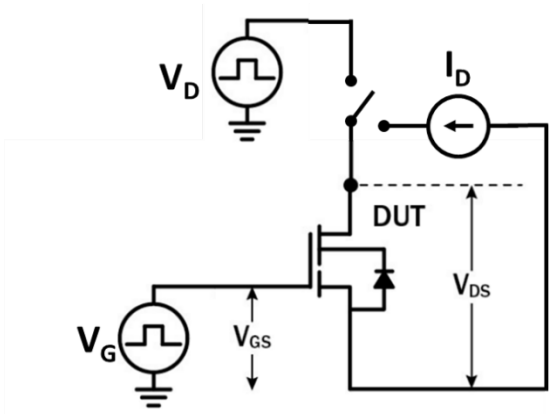


Figure 17. Dynamic $R_{DS(on)eff}$ Test Circuit

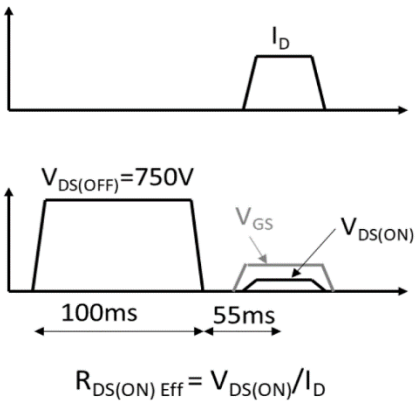
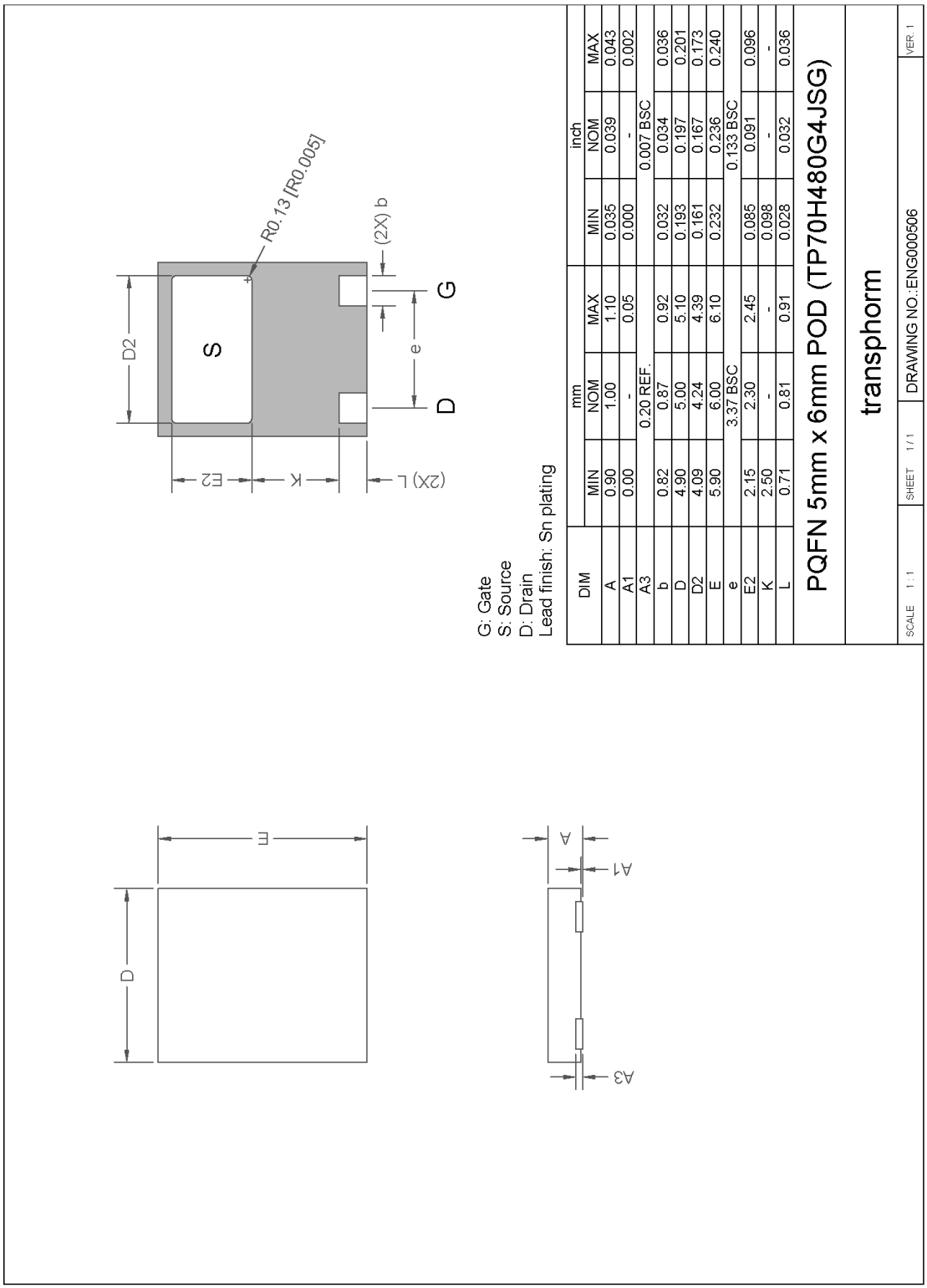


Figure 18. Dynamic $R_{DS(on)eff}$ Waveform

5. Package Outline Drawings



DIM	mm			inch		
	MIN	NOM	MAX	MIN	NOM	MAX
A	0.90	1.00	1.10	0.035	0.039	0.043
A1	0.00	-	0.05	0.000	-	0.002
A3		0.20 REF.			0.007 BSC	
b	0.82	0.87	0.92	0.032	0.034	0.036
D	4.90	5.00	5.10	0.193	0.197	0.201
D2	4.09	4.24	4.39	0.161	0.167	0.173
E	5.90	6.00	6.10	0.232	0.236	0.240
e		3.37 BSC			0.133 BSC	
E2	2.15	2.30	2.45	0.085	0.091	0.096
K	2.50	-	-	0.098	-	-
L	0.71	0.81	0.91	0.028	0.032	0.036

Figure 19. Package Outline Drawing – 5 × 6 PQFN

6. Related Information

All technical documents for Renesas GaN Power devices are accessible from the GaN Power Solutions page.

7. Ordering Information

Part Number	Package Description	Package Configuration
TP65H480G4JSG-TR [1]	5 × 6 PQFN PP	Source

1. “-TR” suffix refers to tape and reel.

8. Revision History

Revision	Date	Description
1.01	Nov 21, 2025	Updated the document's formatting; no technical changes were completed.
1.00	Aug 4, 2025	Initial release.

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