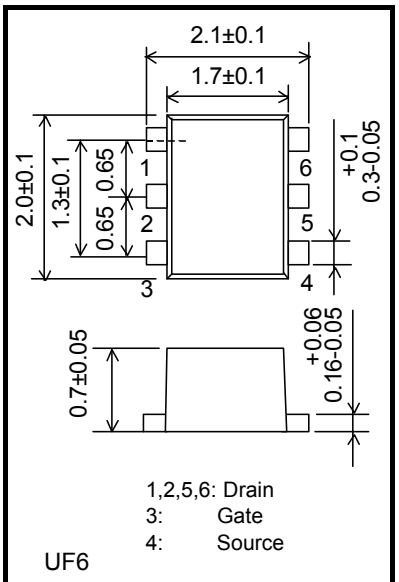
TOSHIBA Field-Effect Transistor Silicon P-Channel MOS Type (U-MOSⅥ)

SSM6J412TU

○ Power Management Switch Applications

- 1.5-V drive
- Low ON-resistance: $R_{DS(ON)}$ = 99.6 mΩ (max) (@V_{GS} = -1.5 V)
  $R_{DS(ON)}$ = 67.8 mΩ (max) (@V_{GS} = -1.8 V)
  $R_{DS(ON)}$ = 51.4 mΩ (max) (@V_{GS} = -2.5 V)
  $R_{DS(ON)}$ = 42.7 mΩ (max) (@V_{GS} = -4.5 V)

Unit: mm



JEDEC	―
JEITA	―
TOSHIBA	2-2T1D

Weight : 7.0mg (typ.)

Absolute Maximum Ratings (Ta = 25°C)

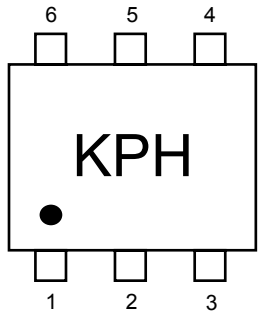
Characteristic		Symbol	Rating	Unit
Drain-source voltage		V_{DSS}	-20	V
Gate-source voltage		V_{GSS}	± 8	V
Drain current	DC	I_D	-4.0	A
	Pulse	I_{DP} (Note 1)	-16.0	
Power dissipation		P_D (Note 2)	1	W
Channel temperature		T_{ch}	150	°C
Storage temperature range		T_{stg}	−55 to 150	°C

Note: Using continuously under heavy loads (e.g. the application of high temperature/current/voltage and the significant change in temperature, etc.) may cause this product to decrease in the reliability significantly even if the operating conditions (i.e. operating temperature/current/voltage, etc.) are within the absolute maximum ratings.
Please design the appropriate reliability upon reviewing the Toshiba Semiconductor Reliability Handbook (“Handling Precautions”/“Derating Concept and Methods”) and individual reliability data (i.e. reliability test report and estimated failure rate, etc).

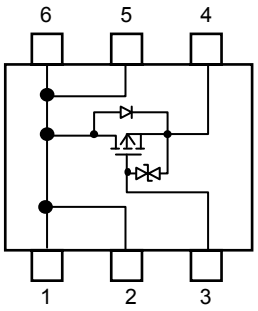
Note 1: Pw ≤ 10μs, Duty. ≤ 1%

Note 2: Mounted on a FR4 board.
(25.4 mm × 25.4 mm × 1.6 mm , Cu Pad: 645 mm^2)

Marking (Top View)



Equivalent Circuit



Start of commercial production
2010-03

Electrical Characteristics (Ta = 25°C)

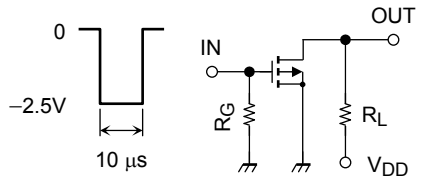
Characteristic		Symbol	Test Conditions		Min	Typ.	Max	Unit
Drain-source breakdown voltage		$V_{(BR)\ DSS}$	I_D = -1 mA, V_{GS} = 0 V		-20	—	—	V
		$V_{(BR)\ DSX}$	I_D = -1 mA, V_{GS} = 5 V	(Note 4)	-15	—	—	V
Drain cut-off current		I_{DSS}	V_{DS} = -20 V, V_{GS} = 0 V		—	—	-1	μA
Gate leakage current		I_{GSS}	V_{GS} = ±8 V, V_{DS} = 0 V		—	—	±1	μA
Gate threshold voltage		V_{th}	V_{DS} = -3 V, I_D = -1 mA		-0.3	—	-1.0	V
Forward transfer admittance		$\|Y_{fs}\|$	V_{DS} = -3 V, I_D = -1.0 A	(Note 3)	4.5	9.1	—	S
Drain–source ON-resistance		$R_{DS\ (ON)}$	I_D = -3.0 A, V_{GS} = -4.5 V	(Note 3)	—	36.9	42.7	mΩ
			I_D = -2.5 A, V_{GS} = -2.5 V	(Note 3)	—	42.8	51.4	
			I_D = -1.5 A, V_{GS} = -1.8 V	(Note 3)	—	50.6	67.8	
			I_D = -0.5 A, V_{GS} = -1.5 V	(Note 3)	—	58.6	99.6	
Input capacitance		C_{iss}	V_{DS} = -10 V, V_{GS} = 0 V f = 1 MHz		—	840	—	pF
Output capacitance		C_{oss}			—	118	—	
Reverse transfer capacitance		C_{rss}			—	99	—	
Switching time	Turn-on time	t_{on}	V_{DD} = -10 V, I_D = -2.0 A V_{GS} = 0 to -2.5 V, R_G = 4.7 Ω		—	32	—	ns
	Turn-off time	t_{off}			—	107	—	
Total gate charge		Q_g	V_{DD} = -10 V, I_D = -4.0 A, V_{GS} = -4.5 V		—	12.8	—	nC
Gate-source charge		Q_{gs1}			—	1.4	—	
Gate-drain charge		Q_{gd}			—	3.0	—	
Drain-source forward voltage		V_{DSF}	I_D = 4.0 A, V_{GS} = 0 V	(Note 3)	—	0.88	1.2	V

Note 3: Pulse test

Note 4: If a forward bias is applied between gate and source, this device enters V(BR)DSX mode. Note that the drain-source breakdown voltage is lowered in this mode.

Switching Time Test Circuit

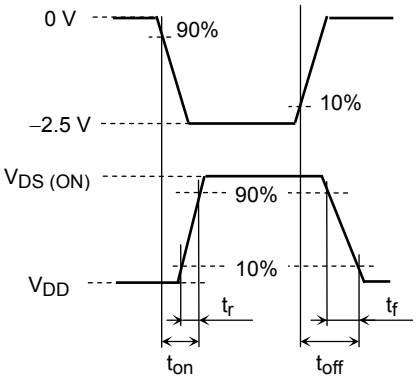
(a) Test Circuit



V_{DD} = -10 V
R_G = 4.7 Ω
Duty ≤ 1%
V_{IN}: t_r, t_f < 5 ns
Common Source
Ta = 25°C

(b) V_{IN}

(c) V_{OUT}



Notice on Usage

V_{th} can be expressed as the voltage between gate and source when the low operating current value is I_D = -1 mA for this product. For normal switching operation, $V_{GS\ (on)}$ requires a higher voltage than V_{th} and $V_{GS\ (off)}$ requires a lower voltage than V_{th}. (The relationship can be established as follows: $V_{GS\ (off)} < V_{th} < V_{GS\ (on)}$.)

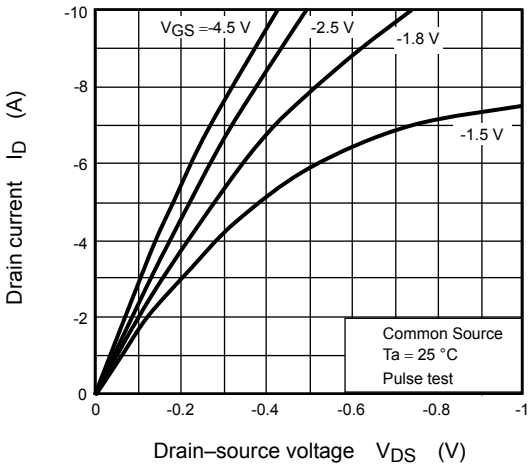
Take this into consideration when using the device.

Handling Precaution

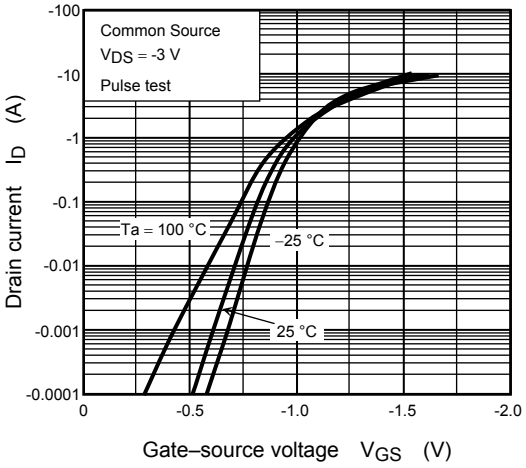
When handling individual devices that are not yet mounted on a circuit board, make sure that the environment is protected against electrostatic discharge. Operators should wear antistatic clothing, and containers and other objects that come into direct contact with devices should be made of antistatic materials.

Thermal resistance $R_{th\ (ch\text{-}a)}$ and power dissipation P_D vary depending on board material, board area, board thickness and pad area. When using this device, please take heat dissipation into consideration.

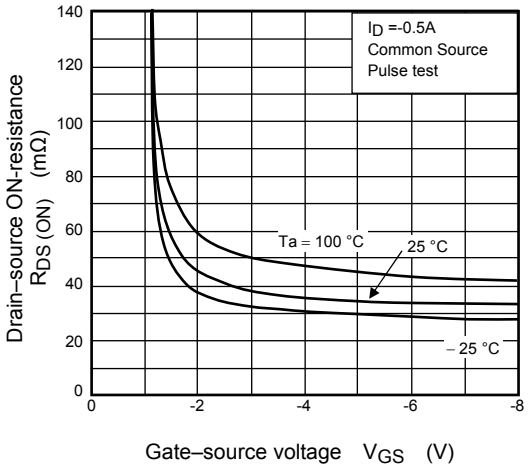
$I_D - V_{DS}$



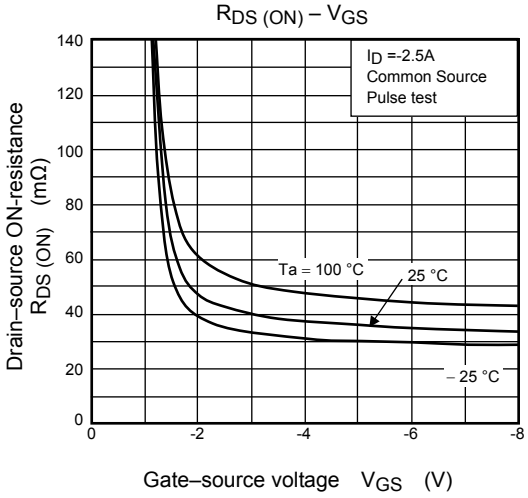
$I_D - V_{GS}$



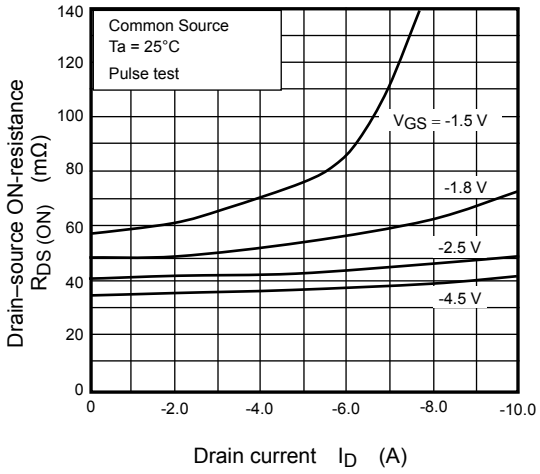
$R_{DS\ (ON)} - V_{GS}$



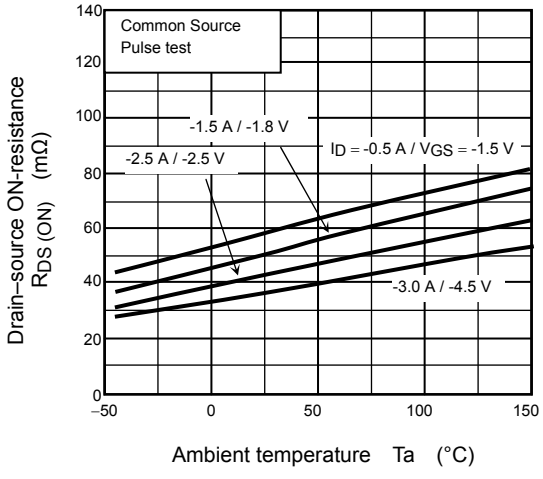
$R_{DS\ (ON)} - V_{GS}$



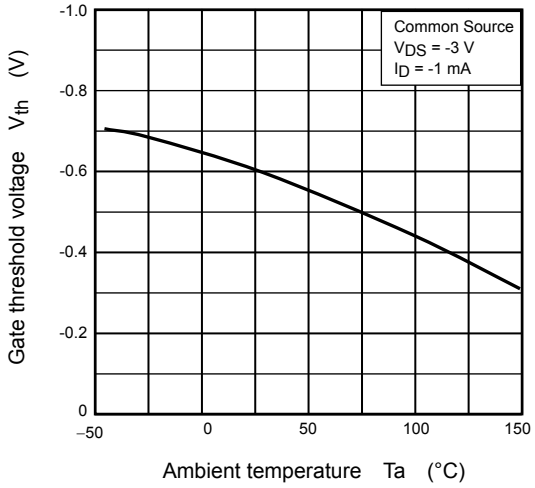
$R_{DS\ (ON)} - I_D$



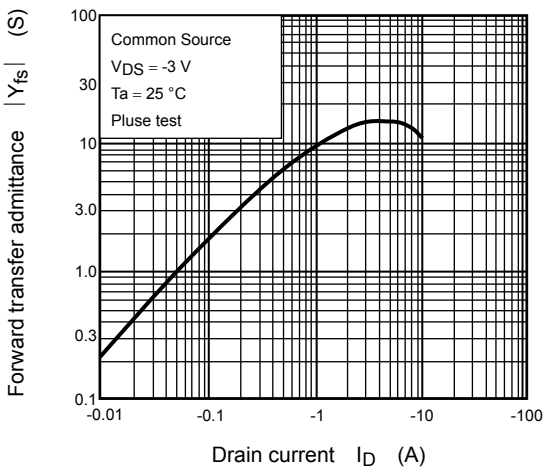
$R_{DS\ (ON)} - Ta$



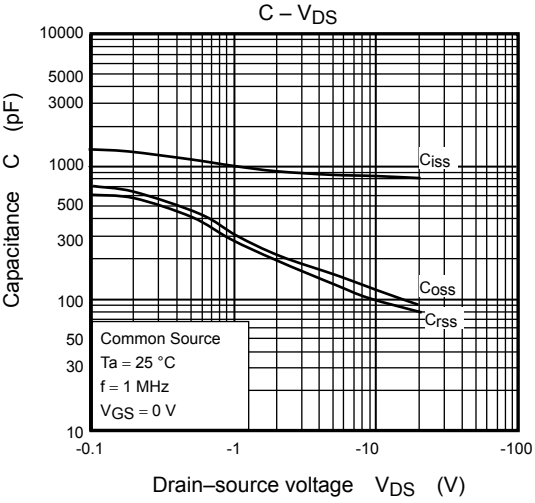
V_{th} – Ta



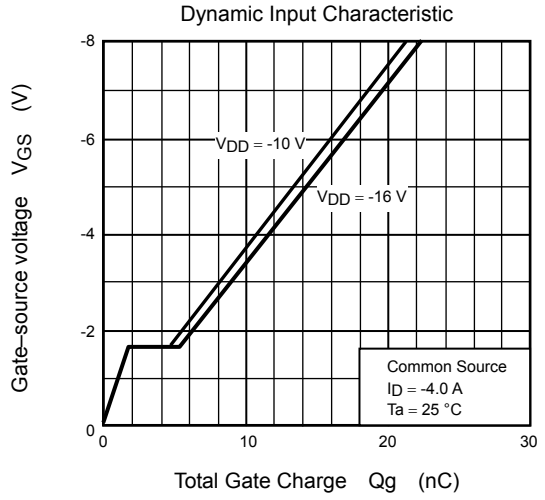
$|Y_{fs}|$ – I_D



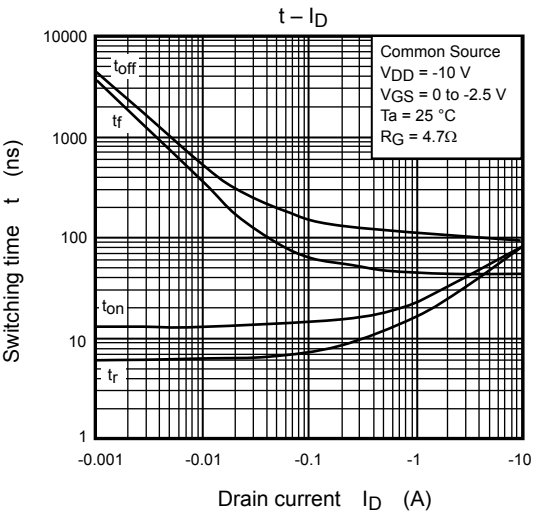
C – V_{DS}



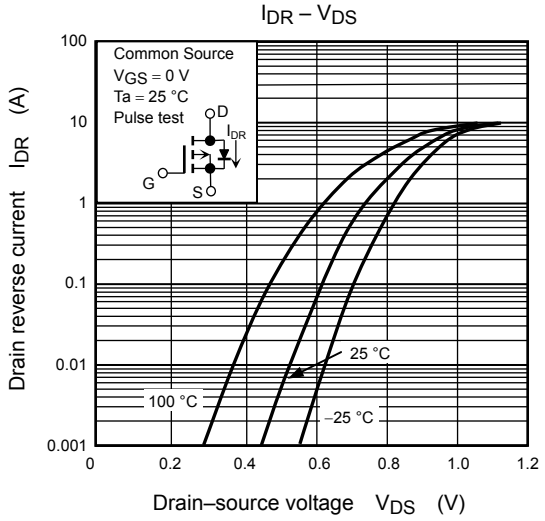
Dynamic Input Characteristic



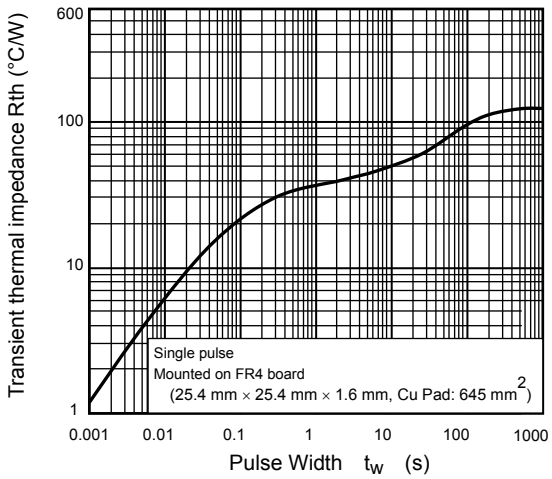
t – I_D



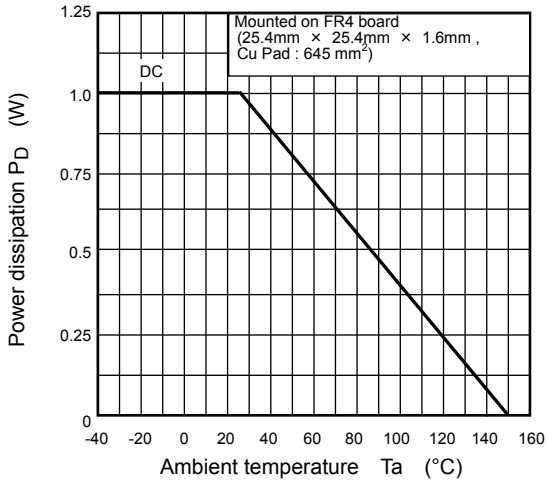
I_{DR} – V_{DS}



Rth – t_w


Transient thermal impedance Rth (°C/W)
600
100
10
1
0.001
0.01
0.1
1
10
100
1000
Pulse Width t_w (s)
Single pulse
Mounted on FR4 board
(25.4 mm × 25.4 mm × 1.6 mm, Cu Pad: 645 mm^2)

P_D – T_a


Power dissipation P_D (W)
1.25
1.0
0.75
0.5
0.25
0
-40
-20
0
20
40
60
80
100
120
140
160
Ambient temperature Ta (°C)
DC
Mounted on FR4 board
(25.4mm × 25.4mm × 1.6mm ,
Cu Pad : 645 mm^2)

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