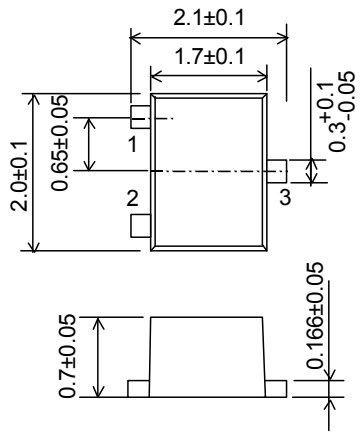
TOSHIBA Field Effect Transistor Silicon N Channel MOS Type

SSM3K116TU

High Speed Switching Applications

- 2.5V drive
- Low on-resistance: R_{on} = 135mΩ (max) (@V_{GS} = 2.5 V)
  R_{on} = 100mΩ (max) (@V_{GS} = 4.5 V)

Unit: mm



1: Gate
2: Source
3: Drain

UFM	
JEDEC	—
JEITA	—
TOSHIBA	2-2U1A

Weight: 6.6 mg (typ.)

Absolute Maximum Ratings (Ta = 25°C)

Characteristic		Symbol	Rating	Unit
Drain-Source voltage		V_{DS}	30	V
Gate-Source voltage		V_{GSS}	± 12	V
Drain current	DC	I_D	2.2	A
	Pulse	I_{DP}	4.4	
Drain power dissipation		$P_{D\ (Note\ 1)}$	800	mW
		$P_{D\ (Note\ 2)}$	500	
Channel temperature		T_{ch}	150	°C
Storage temperature range		T_{stg}	−55 to 150	°C

Note: Using continuously under heavy loads (e.g. the application of high temperature/current/voltage and the significant change in temperature, etc.) may cause this product to decrease in the reliability significantly even if the operating conditions (i.e. operating temperature/current/voltage, etc.) are within the absolute maximum ratings.
Please design the appropriate reliability upon reviewing the Toshiba Semiconductor Reliability Handbook (“Handling Precautions”/“Derating Concept and Methods”) and individual reliability data (i.e. reliability test report and estimated failure rate, etc).

Note 1: Mounted on ceramic board.
(25.4 mm × 25.4 mm × 0.8 mm, Cu Pad: 645 mm^2)

Note 2: Mounted on FR4 board.
(25.4 mm × 25.4 mm × 1.6 mm, Cu Pad: 645 mm^2)

Electrical Characteristics (Ta = 25°C)

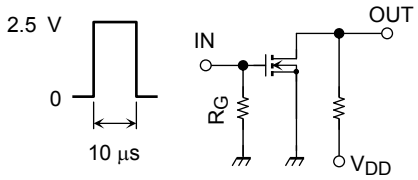
Characteristic		Symbol	Test Conditions	Min	Typ.	Max	Unit
Drain-Source breakdown voltage		$V_{(BR)\ DSS}$	I_D = 1 mA, V_{GS} = 0	30	—	—	V
		$V_{(BR)\ DSX}$	I_D = 1 mA, V_{GS} = −12 V	18	—	—	
Drain cut-off current		I_{DSS}	V_{DS} = 30 V, V_{GS} = 0	—	—	1	μA
Gate leakage current		I_{GSS}	V_{GS} = ±12V, V_{DS} = 0	—	—	±1	μA
Gate threshold voltage		V_{th}	V_{DS} = 3 V, I_D = 0.1 mA	0.5	—	1.1	V
Forward transfer admittance		$\|Y_{fs}\|$	V_{DS} = 3 V, I_D = 0.25 A (Note3)	1	2	—	S
Drain-Source on-resistance		$R_{DS\ (ON)}$	I_D = 0.5 A, V_{GS} = 4.5 V (Note3)	—	75	100	mΩ
			I_D = 0.25 A, V_{GS} = 2.5 V (Note3)	—	95	135	
Input capacitance		C_{iss}	V_{DS} = 10 V, V_{GS} = 0, f = 1 MHz	—	245	—	pF
Output capacitance		C_{oss}	V_{DS} = 10 V, V_{GS} = 0, f = 1 MHz	—	41	—	pF
Reverse transfer capacitance		C_{rss}	V_{DS} = 10 V, V_{GS} = 0, f = 1 MHz	—	33	—	pF
Switching time	Turn-on time	t_{on}	V_{DD} = 10 V, I_D = 0.25 A,	—	9	—	ns
	Turn-off time	t_{off}	V_{GS} = 0 to 2.5 V, R_G = 4.7 Ω	—	15	—	
Drain-Source forward voltage		V_{DSF}	I_D = −2.2A, V_{GS} = 0 V (Note3)	—	−0.83	-1.2	V

Note3: Pulse test

Start of commercial production
2005-06

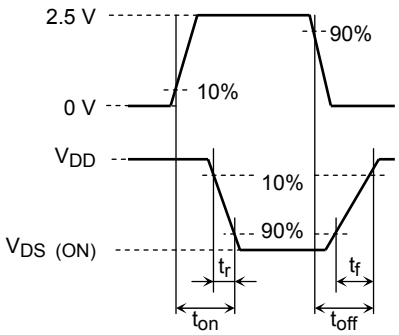
Switching Time Test Circuit

(a) Test Circuit



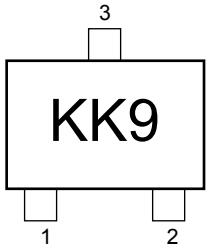
V_{DD} = 10 V
R_G = 4.7 Ω
Duty ≤ 1%
V_{IN}: t_r, t_f < 5 ns
Common Source
Ta = 25°C

(b) V_{IN}

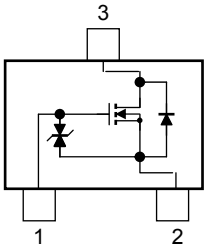


(c) V_{OUT}

Marking



Equivalent Circuit (top view)



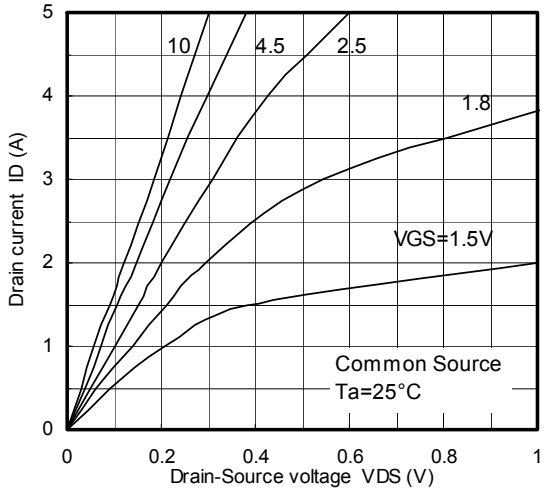
Precaution

V_{th} can be expressed as the voltage between gate and source when the low operating current value is I_D=0.1mA for this product. For normal switching operation, $V_{GS\ (on)}$ requires a higher voltage than V_{th}, and $V_{GS\ (off)}$ requires a lower voltage than V_{th}.
(The relationship can be established as follows: $V_{GS\ (off)} < V_{th} < V_{GS\ (on)}$)
Take this into consideration when using the device.

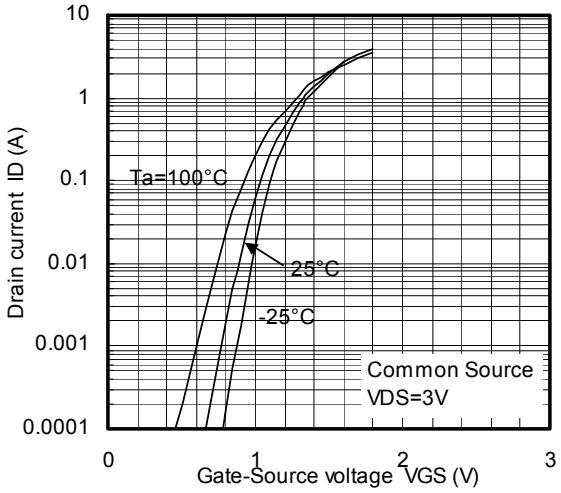
Handling Precaution

When handling individual devices which are not yet mounted on a circuit board, be sure that the environment is protected against electrostatic discharge. Operators should wear anti-static clothing, and containers and other objects that come into direct contact with devices should be made of anti-static materials.

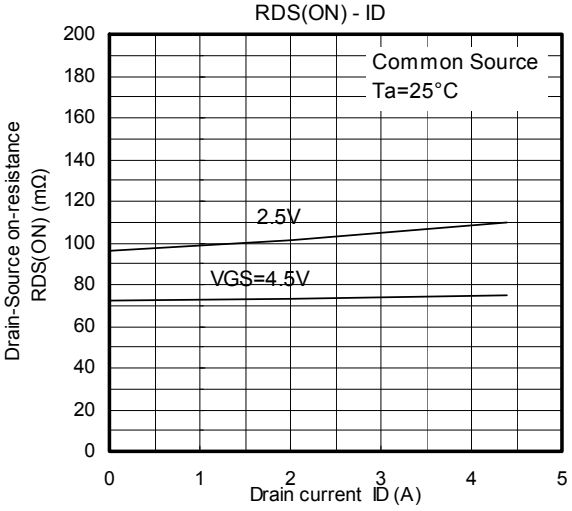
ID - VDS



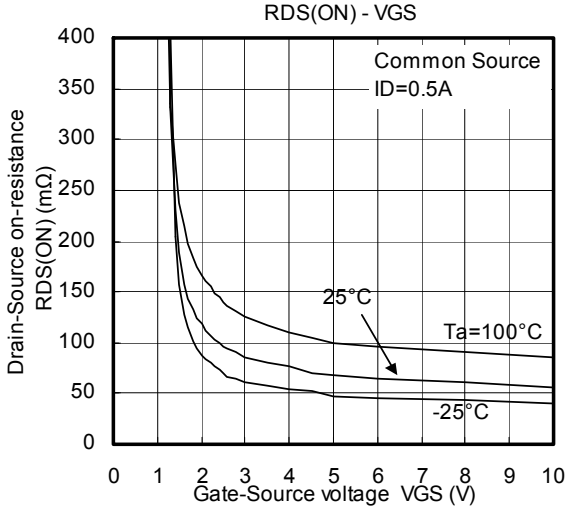
ID - VGS



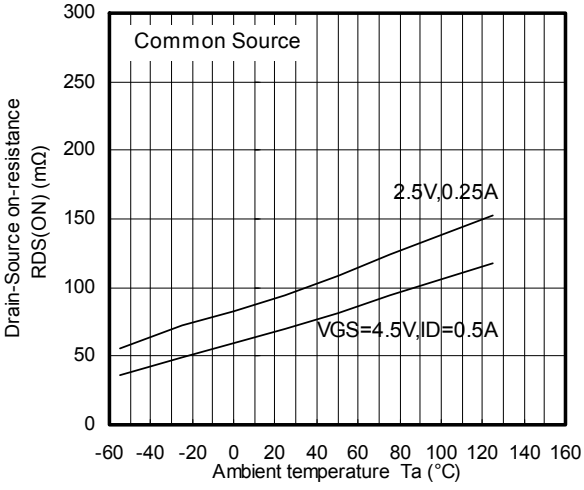
RDS(ON) - ID



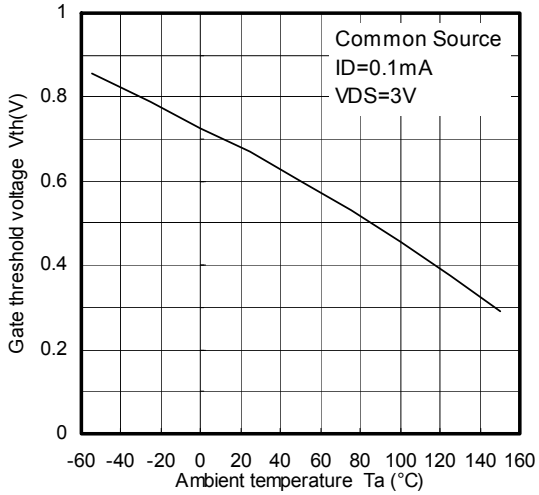
RDS(ON) - VGS

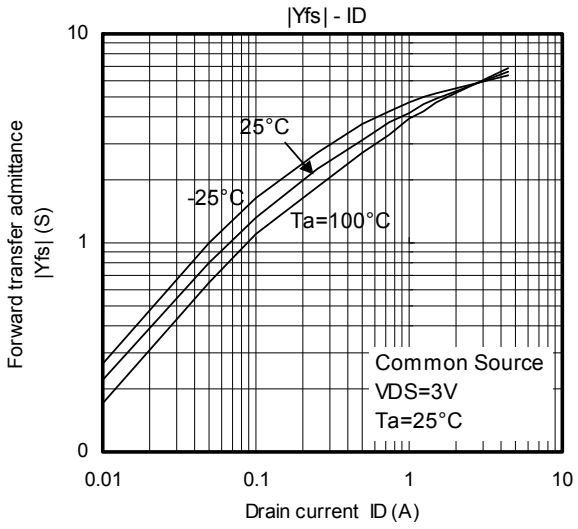


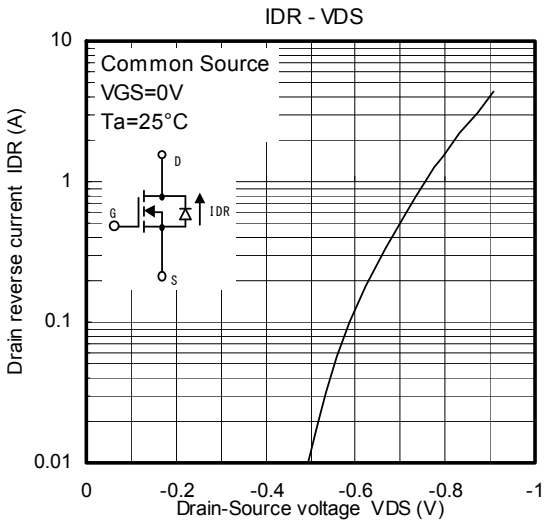
RDS(ON) - Ta

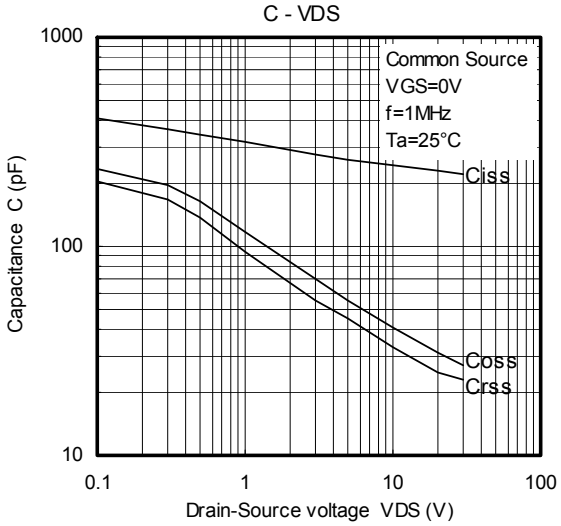


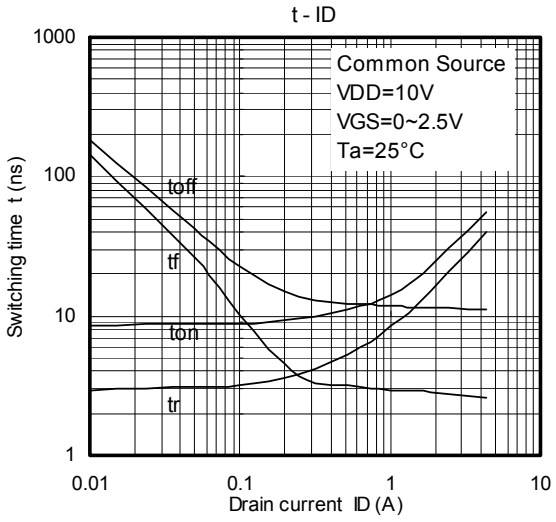
Vth - Ta

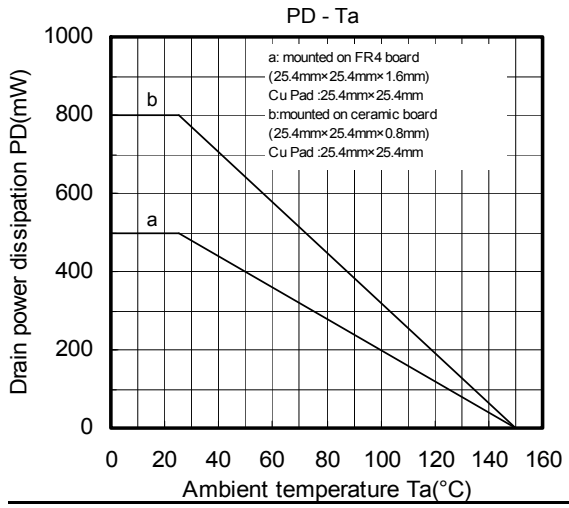


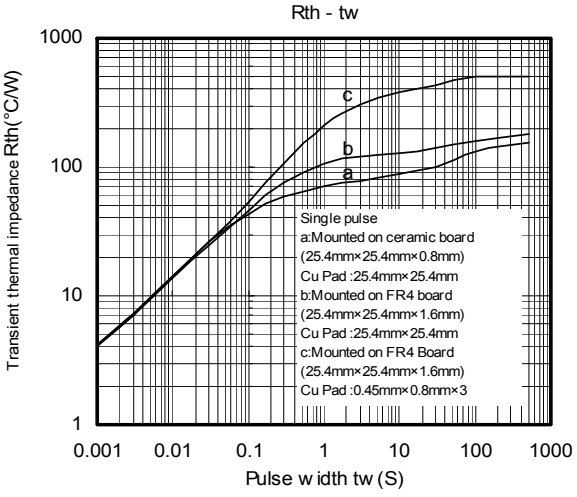

|Yfs| - ID
Forward transfer admittance |Yfs| (S)
Drain current ID (A)
25°C
-25°C
Ta=100°C
Common Source
VDS=3V
Ta=25°C
10
1
0
0.01
0.1
1
10


IDR - VDS
Drain reverse current IDR (A)
Drain-Source voltage VDS (V)
Common Source
VGS=0V
Ta=25°C
D
G
S
IDR
10
1
0.1
0.01
0
-0.2
-0.4
-0.6
-0.8
-1


C - VDS
Capacitance C (pF)
Drain-Source voltage VDS (V)
Common Source
VGS=0V
f=1MHz
Ta=25°C
Ciss
Coss
Crss
1000
100
10
0.1
1
10
100


t - ID
Switching time t (ns)
Drain current ID (A)
Common Source
VDD=10V
VGS=0~2.5V
Ta=25°C
toff
tf
ton
tr
1000
100
10
1
0.01
0.1
1
10


PD - Ta
Drain power dissipation PD(mW)
Ambient temperature Ta(°C)
a: mounted on FR4 board
(25.4mm×25.4mm×1.6mm)
Cu Pad :25.4mm×25.4mm
b:mounted on ceramic board
(25.4mm×25.4mm×0.8mm)
Cu Pad :25.4mm×25.4mm
b
a
1000
800
600
400
200
0
0
20
40
60
80
100
120
140
160


Rth - tw
Transient thermal impedance Rth(°C/W)
Pulse width tw (S)
c
b
a
Single pulse
a:Mounted on ceramic board
(25.4mm×25.4mm×0.8mm)
Cu Pad :25.4mm×25.4mm
b:Mounted on FR4 board
(25.4mm×25.4mm×1.6mm)
Cu Pad :25.4mm×25.4mm
c:Mounted on FR4 Board
(25.4mm×25.4mm×1.6mm)
Cu Pad :0.45mm×0.8mm×3
1000
100
10
1
0.001
0.01
0.1
1
10
100
1000

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