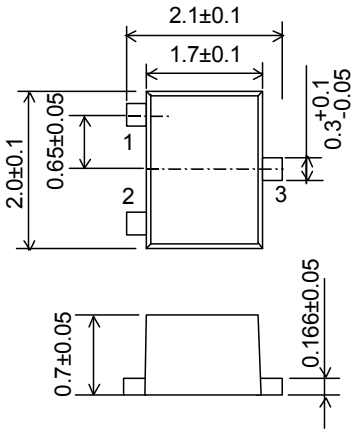
TOSHIBA Field-Effect Transistor Silicon P-Channel MOS Type (U-MOSⅥ)

SSM3J130TU

○ Power Management Switch Applications

- 1.5 V drive
- Low ON-resistance: $R_{DS(ON)}$ = 63.2 mΩ (max) (@V_{GS} = -1.5 V)
  $R_{DS(ON)}$ = 41.1 mΩ (max) (@V_{GS} = -1.8 V)
  $R_{DS(ON)}$ = 31.0 mΩ (max) (@V_{GS} = -2.5 V)
  $R_{DS(ON)}$ = 25.8 mΩ (max) (@V_{GS} = -4.5 V)

Unit: mm



UFM

JEDEC	―
JEITA	―
TOSHIBA	2-2U1A

Weight: 6.6 mg (typ.)

Absolute Maximum Ratings (Ta = 25°C)

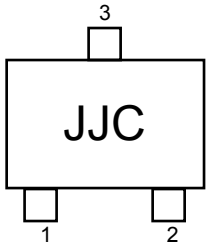
Characteristic		Symbol	Rating	Unit
Drain-Source voltage		V_{DSS}	-20	V
Gate-Source voltage		V_{GSS}	±8	V
Drain current	DC	I_D	-4.4	A
	Pulse	I_{DP}	-8.8	
Power dissipation		P_D (Note 1)	800	mW
		P_D (Note 2)	500	
Channel temperature		T_{ch}	150	°C
Storage temperature range		T_{stg}	-55 to 150	°C

Note: Using continuously under heavy loads (e.g. the application of high temperature/current/voltage and the significant change in temperature, etc.) may cause this product to decrease in the reliability significantly even if the operating conditions (i.e. operating temperature/current/voltage, etc.) are within the absolute maximum ratings.
Please design the appropriate reliability upon reviewing the Toshiba Semiconductor Reliability Handbook (“Handling Precautions”/“Derating Concept and Methods”) and individual reliability data (i.e. reliability test report and estimated failure rate, etc).

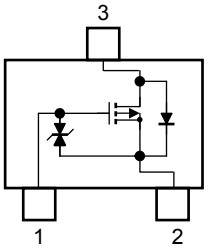
Note 1: Mounted on a ceramic board.
(25.4 mm × 25.4 mm × 0.8 mm, Cu Pad: 645 mm^2)

Note 2: Mounted on an FR4 board.
(25.4 mm × 25.4 mm × 1.6 mm, Cu Pad: 645 mm^2)

Marking



Equivalent Circuit (top view)



Start of commercial production
2009-01

Electrical Characteristics (Ta = 25°C)

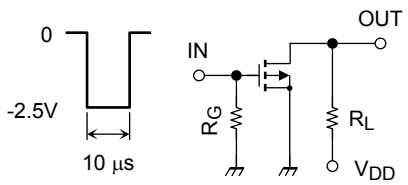
Characteristic		Symbol	Test Conditions		Min	Typ.	Max	Unit
Drain-Source breakdown voltage		$V_{(BR)\ DSS}$	I_D = -1 mA, V_{GS} = 0 V		-20	—	—	V
		$V_{(BR)\ DSX}$	I_D = -1 mA, V_{GS} = 5 V	(Note 4)	-15	—	—	
Drain cut-off current		I_{DSS}	V_{DS} = -20 V, V_{GS} = 0 V		—	—	-1	μA
Gate leakage current		I_{GSS}	V_{GS} = ±8 V, V_{DS} = 0 V		—	—	±1	μA
Gate threshold voltage		V_{th}	V_{DS} = -3 V, I_D = -1 mA		-0.3	—	-1.0	V
Forward transfer admittance		$\|Y_{fs}\|$	V_{DS} = -3 V, I_D = -2.0 A	(Note 3)	8.8	17.5	—	S
Drain–source ON-resistance		$R_{DS\ (ON)}$	I_D = -4.0 A, V_{GS} = -4.5 V	(Note 3)	—	20.9	25.8	mΩ
			I_D = -4.0 A, V_{GS} = -2.5 V	(Note 3)	—	24.2	31.0	
			I_D = -2.5 A, V_{GS} = -1.8 V	(Note 3)	—	28.8	41.1	
			I_D = -1.5 A, V_{GS} = -1.5 V	(Note 3)	—	32.4	63.2	
Input capacitance		C_{iss}	V_{DS} = -10 V, V_{GS} = 0 V f = 1 MHz		—	1800	—	pF
Output capacitance		C_{oss}			—	205	—	
Reverse transfer capacitance		C_{rss}			—	190	—	
Switching time	Turn-on time	t_{on}	V_{DD} = -10 V, I_D = -1.5 A V_{GS} = 0 to -2.5 V, R_G = 4.7 Ω		—	25	—	ns
	Turn-off time	t_{off}			—	133	—	
Total Gate Charge		Q_g	V_{DS} = -10 V, I_{DS} = - 4.4 A, V_{GS} = - 4.5 V		—	24.8	—	nC
Gate-Source Charge		Q_{gs}			—	18.0	—	
Gate-Drain Charge		Q_{gd}			—	6.8	—	
Drain-Source forward voltage		V_{DSF}	I_D = 4.4 A, V_{GS} = 0 V	(Note 3)	—	0.83	1.2	V

Note3: Pulse test

Note4: If a forward bias is applied between gate and source, this device enters V(BR)DSX mode. Note that the drain-source breakdown voltage is lowered in this mode.

Switching Time Test Circuit

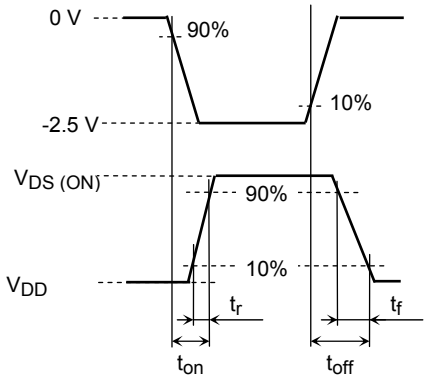
(a) Test Circuit



V_{DD} = -10 V
R_G = 4.7 Ω
Duty ≤ 1%
V_{IN}: t_r, t_f < 5 ns
Common Source
Ta = 25°C

(b) V_{IN}

(c) V_{OUT}



Usage Considerations

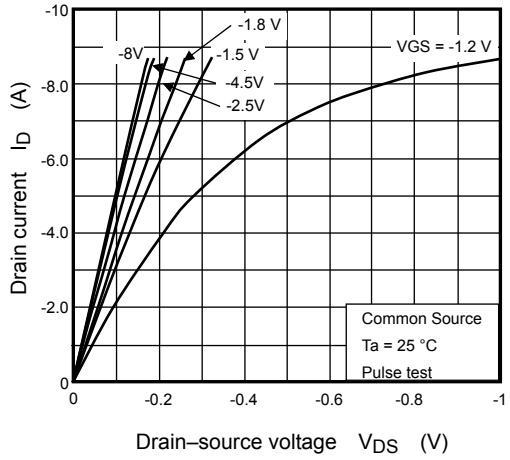
Let V_{th} be the voltage applied between gate and source that causes the drain current (I_D) to below −1 mA for the SSM3J130TU. Then, for normal switching operation, $V_{GS(on)}$ must be higher than V_{th}, and $V_{GS(off)}$ must be lower than V_{th}. This relationship can be expressed as: $V_{GS(off)} < V_{th} < V_{GS(on)}$.

Take this into consideration when using the device.

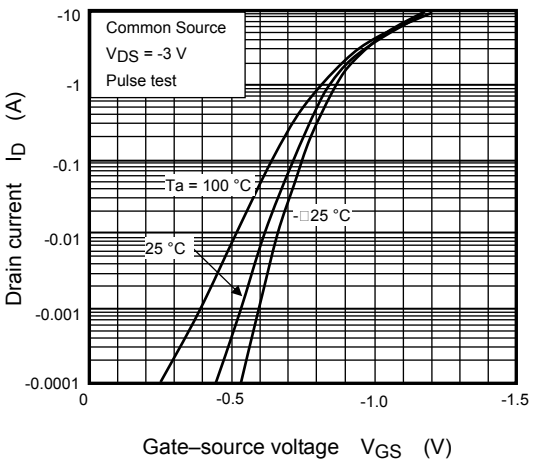
Handling Precaution

When handling individual devices that are not yet mounted on a circuit board, make sure that the environment is protected against electrostatic discharge. Operators should wear antistatic clothing, and containers and other objects that come into direct contact with devices should be made of antistatic materials.

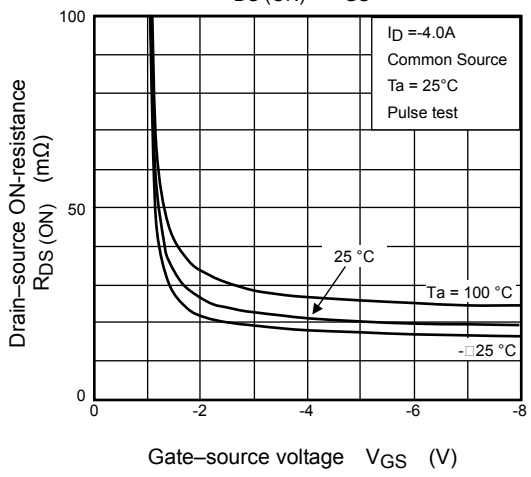
$I_D - V_{DS}$



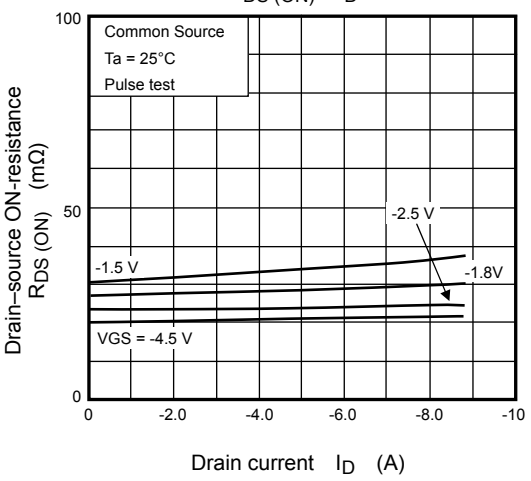
$I_D - V_{GS}$



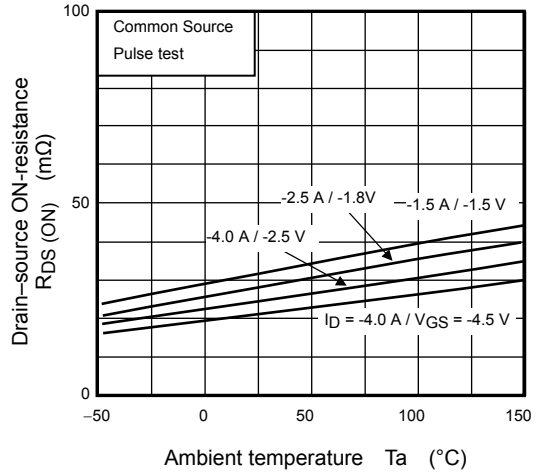
$R_{DS\ (ON)} - V_{GS}$



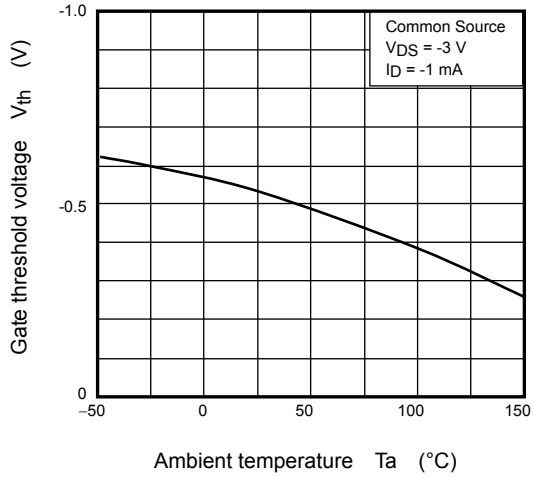
$R_{DS\ (ON)} - I_D$

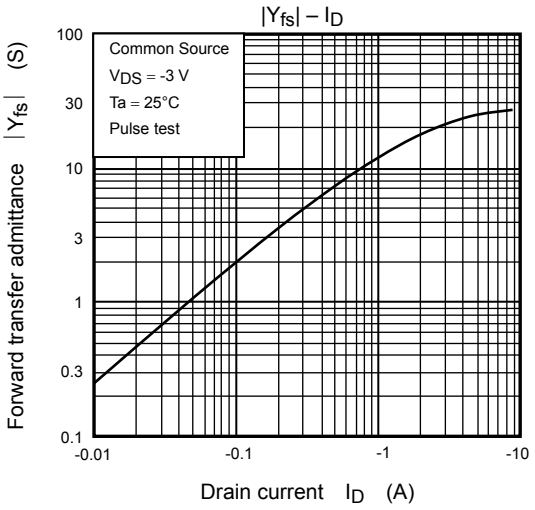


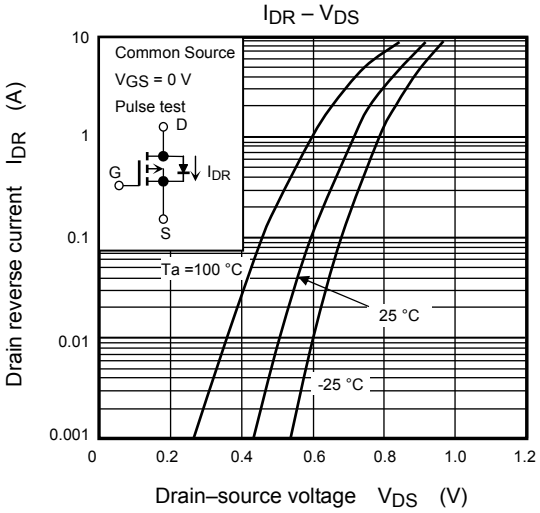
$R_{DS\ (ON)} - Ta$

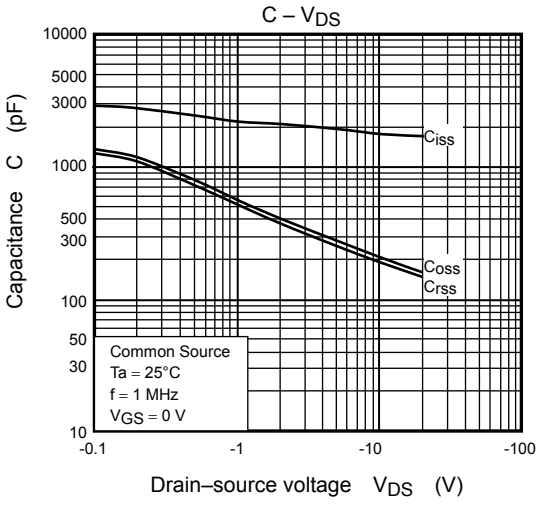


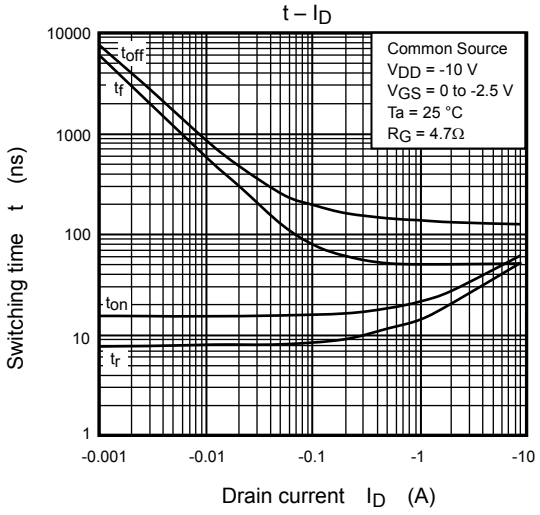
$V_{th} - Ta$

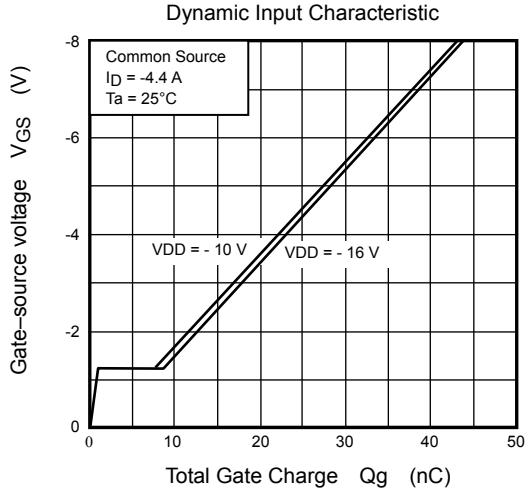



|Yfs| – ID
Common Source
VDS = -3 V
Ta = 25°C
Pulse test
Forward transfer admittance |Yfs| (S)
100
30
10
3
1
0.3
0.1
-0.01
-0.1
-1
-10
Drain current ID (A)

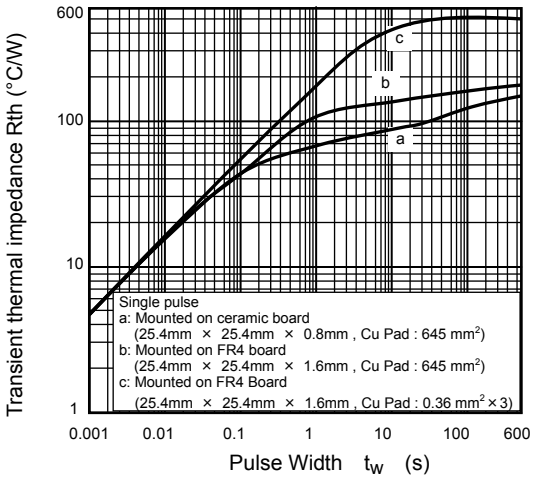

IDR – VDS
Common Source
VGS = 0 V
Pulse test
D
G
S
IDR
Ta =100 °C
25 °C
-25 °C
Drain reverse current IDR (A)
10
1
0.1
0.01
0.001
0
0.2
0.4
0.6
0.8
1.0
1.2
Drain–source voltage VDS (V)


C – VDS
Ciss
Coss
Crss
Common Source
Ta = 25°C
f = 1 MHz
VGS = 0 V
Capacitance C (pF)
10000
5000
3000
1000
500
300
100
50
30
10
-0.1
-1
-10
-100
Drain–source voltage VDS (V)

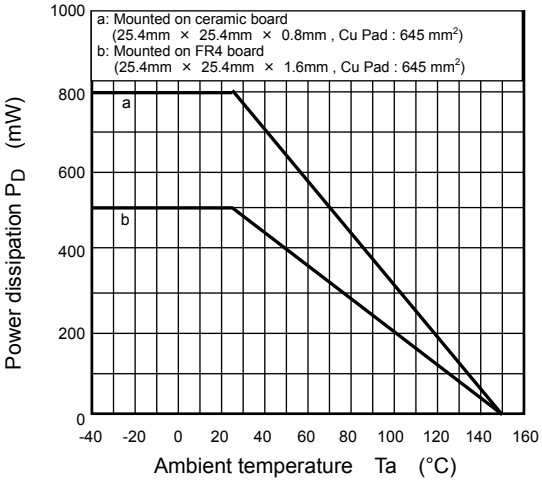

t – ID
toff
tf
ton
tr
Common Source
VDD = -10 V
VGS = 0 to -2.5 V
Ta = 25 °C
RG = 4.7Ω
Switching time t (ns)
10000
1000
100
10
1
-0.001
-0.01
-0.1
-1
-10
Drain current ID (A)


Dynamic Input Characteristic
Common Source
ID = -4.4 A
Ta = 25°C
VDD = - 10 V
VDD = - 16 V
Gate–source voltage VGS (V)
-8
-6
-4
-2
0
0
10
20
30
40
50
Total Gate Charge Qg (nC)

$R_{th} - t_w$


Transient thermal impedance Rth (°C/W)
600
100
10
1
0.001
0.01
0.1
1
10
100
600
Pulse Width tw (s)
c
b
a
Single pulse
a: Mounted on ceramic board
(25.4mm × 25.4mm × 0.8mm , Cu Pad : 645 mm²)
b: Mounted on FR4 board
(25.4mm × 25.4mm × 1.6mm , Cu Pad : 645 mm²)
c: Mounted on FR4 Board
(25.4mm × 25.4mm × 1.6mm , Cu Pad : 0.36 mm² × 3)

$P_D - T_a$


Power dissipation PD (mW)
1000
800
600
400
200
0
-40
-20
0
20
40
60
80
100
120
140
160
Ambient temperature Ta (°C)
a: Mounted on ceramic board
(25.4mm × 25.4mm × 0.8mm , Cu Pad : 645 mm²)
b: Mounted on FR4 board
(25.4mm × 25.4mm × 1.6mm , Cu Pad : 645 mm²)
a
b

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