MOSFETs Silicon N-channel MOS (U-MOSⅧ-H)

# TPH6R30ANL

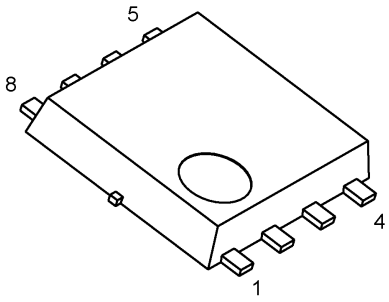
## 1. Applications

- High-Efficiency DC-DC Converters
- Switching Voltage Regulators
- Motor Drivers

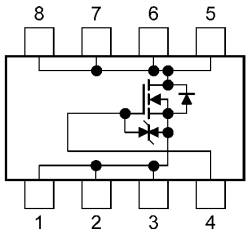
## 2. Features

(1) High-speed switching
(2) Small gate charge : $Q_{SW}$ = 14 nC (typ.)
(3) Small output charge : $Q_{oss}$ = 46 nC (typ.)
(4) Low drain-source on-resistance : $R_{DS(ON)}$ = 5.1 mΩ (typ.) ($V_{GS}$ = 10 V)
(5) Low leakage current : $I_{DSS}$ = 10 μA (max) ($V_{DS}$ = 100 V)
(6) Enhancement mode : $V_{th}$ = 1.5 to 2.5 V ($V_{DS}$ = 10 V, $I_D$ = 0.5 mA)

## 3. Packaging and Internal Circuit




SOP Advance




1, 2, 3: Source
4: Gate
5, 6, 7, 8: Drain

Start of commercial production
2016-09

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## 4. Absolute Maximum Ratings (Note) ($T_a$ = 25 °C unless otherwise specified)

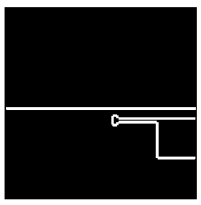
| Characteristics | | | Symbol | Rating | Unit |
|---|---|---|---|---|---|
| Drain-source voltage | | | $V_{DSS}$ | 100 | V |
| Gate-source voltage | | | $V_{GSS}$ | ±20 | |
| Drain current (DC) | ( $T_c$ = 25 °C ) | (Note 1) | $I_D$ | 45 | A |
| Drain current (DC) | ( Silicon limit ) | (Note 1), (Note 2) | $I_D$ | 66 | |
| Drain current (pulsed) | ( t = 100 μs ) | (Note 1) | $I_{DP}$ | 300 | |
| Power dissipation | ( $T_c$ = 25 °C ) | | $P_D$ | 54 | W |
| Power dissipation | | (Note 3) | $P_D$ | 2.5 | |
| Power dissipation | | (Note 4) | $P_D$ | 0.8 | |
| Single-pulse avalanche energy | | (Note 5) | $E_{AS}$ | 63 | mJ |
| Single-pulse avalanche current | | (Note 5) | $I_{AS}$ | 45 | A |
| Channel temperature | | | $T_{ch}$ | 150 | °C |
| Storage temperature | | | $T_{stg}$ | -55 to 150 | |

Note: Using continuously under heavy loads (e.g. the application of high temperature/current/voltage and the significant change in temperature, etc.) may cause this product to decrease in the reliability significantly even if the operating conditions (i.e. operating temperature/current/voltage, etc.) are within the absolute maximum ratings.
Please design the appropriate reliability upon reviewing the Toshiba Semiconductor Reliability Handbook ("Handling Precautions"/"Derating Concept and Methods") and individual reliability data (i.e. reliability test report and estimated failure rate, etc).

## 5. Thermal Characteristics

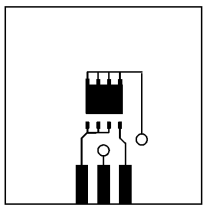
| Characteristics | | | Symbol | Max | Unit |
|---|---|---|---|---|---|
| Channel-to-case thermal resistance | ( $T_c$ = 25 °C ) | | $R_{th(ch-c)}$ | 2.31 | °C/W |
| Channel-to-ambient thermal resistance | ( $T_a$ = 25 °C ) | (Note 3) | $R_{th(ch-a)}$ | 50 | |
| Channel-to-ambient thermal resistance | ( $T_a$ = 25 °C ) | (Note 4) | $R_{th(ch-a)}$ | 156 | |

Note 1: Ensure that the channel temperature does not exceed 150 °C.
Note 2: Limited by silicon chip capability.
Note 3: Device mounted on a glass-epoxy board (a), Figure 5.1
Note 4: Device mounted on a glass-epoxy board (b), Figure 5.2
Note 5: $V_{DD}$ = 60 V, $T_{ch}$ = 25 °C (initial), L = 34 μH, $I_{AS}$ = 45 A



FR-4
25.4 × 25.4 × 1.6
(Unit: mm)
2 oz copper

Fig. 5.1 Device Mounted on a Glass-Epoxy Board (a)



FR-4
25.4 × 25.4 × 1.6
(Unit: mm)
2 oz copper

Fig. 5.2 Device Mounted on a Glass-Epoxy Board (b)

Note: This transistor is sensitive to electrostatic discharge and should be handled with care.

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# 6. Electrical Characteristics

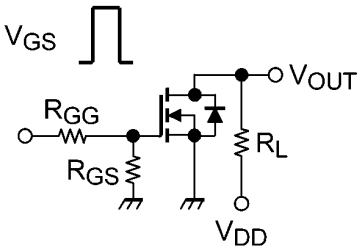
## 6.1. Static Characteristics ($T_a$ = 25 °C unless otherwise specified)

| Characteristics | Symbol | Test Condition | Min | Typ. | Max | Unit |
|---|---|---|---|---|---|---|
| Gate leakage current | $I_{GSS}$ | $V_{GS}$ = ±16 V, $V_{DS}$ = 0 V | — | — | ±10 | μA |
| Drain cut-off current | $I_{DSS}$ | $V_{DS}$ = 100 V, $V_{GS}$ = 0 V | — | — | 10 | |
| Drain-source breakdown voltage | $V_{(BR)DSS}$ | $I_D$ = 10 mA, $V_{GS}$ = 0 V | 100 | — | — | V |
| Drain-source breakdown voltage (Note 6) | $V_{(BR)DSX}$ | $I_D$ = 10 mA, $V_{GS}$ = -20 V | 65 | — | — | |
| Gate threshold voltage | $V_{th}$ | $V_{DS}$ = 10 V, $I_D$ = 0.5 mA | 1.5 | — | 2.5 | |
| Drain-source on-resistance | $R_{DS(ON)}$ | $V_{GS}$ = 4.5 V, $I_D$ = 15 A | — | 6.4 | 10.3 | mΩ |
| | | $V_{GS}$ = 10 V, $I_D$ = 22.5 A | — | 5.1 | 6.3 | |

Note 6: If a reverse bias is applied between gate and source, this device enters $V_{(BR)DSX}$ mode. Note that the drain-source breakdown voltage is lowered in this mode.

## 6.2. Dynamic Characteristics ($T_a$ = 25 °C unless otherwise specified)

| Characteristics | Symbol | Test Condition | Min | Typ. | Max | Unit |
|---|---|---|---|---|---|---|
| Input capacitance | $C_{iss}$ | $V_{DS}$ = 50 V, $V_{GS}$ = 0 V, f = 1 MHz | — | 3300 | 4300 | pF |
| Reverse transfer capacitance | $C_{rss}$ | | — | 27 | 56 | |
| Output capacitance | $C_{oss}$ | | — | 410 | — | |
| Gate resistance | $r_g$ | — | — | 2.1 | 3.2 | Ω |
| Switching time (rise time) | $t_r$ | See Figure 6.2.1 | — | 7 | — | ns |
| Switching time (turn-on time) | $t_{on}$ | | — | 18 | — | |
| Switching time (fall time) | $t_f$ | | — | 12 | — | |
| Switching time (turn-off time) | $t_{off}$ | | — | 58 | — | |




$V_{DD}$ ≈ 50 V
$V_{GS}$ = 0 V/ 10 V
$I_D$ = 22.5 A
$R_L$ = 2.2 Ω
$R_{GG}$ = 0 Ω
$R_{GS}$ = 4.7 Ω
Duty ≤ 1 %, $t_w$ = 10 μs

**Fig. 6.2.1 Switching Time Test Circuit**

## 6.3. Gate Charge Characteristics ($T_a$ = 25 °C unless otherwise specified)

| Characteristics | Symbol | Test Condition | Min | Typ. | Max | Unit |
|---|---|---|---|---|---|---|
| Total gate charge (gate-source plus gate-drain) | $Q_g$ | $V_{DD}$ ≈ 50 V, $V_{GS}$ = 10 V, $I_D$ = 22.5 A | — | 55 | — | nC |
| | | $V_{DD}$ ≈ 50 V, $V_{GS}$ = 4.5 V, $I_D$ = 22.5 A | — | 27 | — | |
| Gate-source charge 1 | $Q_{gs1}$ | $V_{DD}$ ≈ 50 V, $V_{GS}$ = 10 V, $I_D$ = 22.5 A | — | 16 | — | |
| Gate-drain charge | $Q_{gd}$ | | — | 7 | — | |
| Gate switch charge | $Q_{SW}$ | | — | 14 | — | |
| Output charge | $Q_{oss}$ | $V_{DS}$ = 50 V, $V_{GS}$ = 0 V, f = 1 MHz | — | 46 | — | |

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### 6.4. Source-Drain Characteristics ($T_a$ = 25 °C unless otherwise specified)

| Characteristics | Symbol | Test Condition | Min | Typ. | Max | Unit |
|---|---|---|---|---|---|---|
| Reverse drain current (pulsed) (Note 7) | $I_{DRP}$ | (t = 100 μs) | — | — | 300 | A |
| Diode forward voltage | $V_{DSF}$ | $I_{DR}$ = 45 A, $V_{GS}$ = 0 V | — | — | -1.2 | V |
| Reverse recovery time | $t_{rr}$ | $V_R$ = 50 V, $I_{DR}$ = 11.3 A, $V_{GS}$ = 0 V, $-dI_{DR}/dt$ = 100 A/μs | — | 48 | — | ns |
| Reverse recovery charge | $Q_{rr}$ | | — | 61 | — | nC |

Note 7: Ensure that the channel temperature does not exceed 150 °C.

## 7. Marking

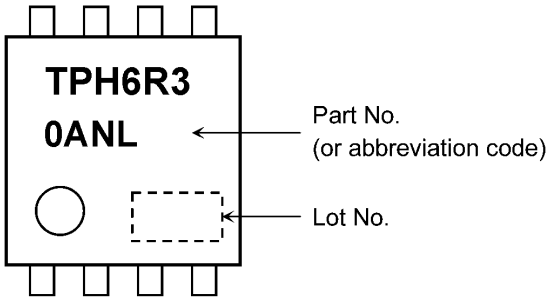



Fig. 7.1 Marking

## 8. Characteristics Curves (Note)

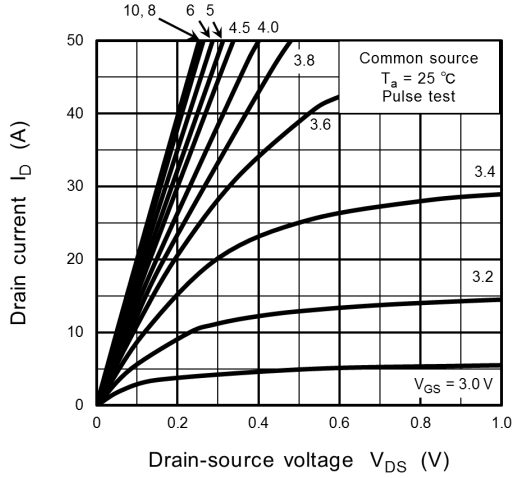



Fig. 8.1 $I_D$ - $V_{DS}$

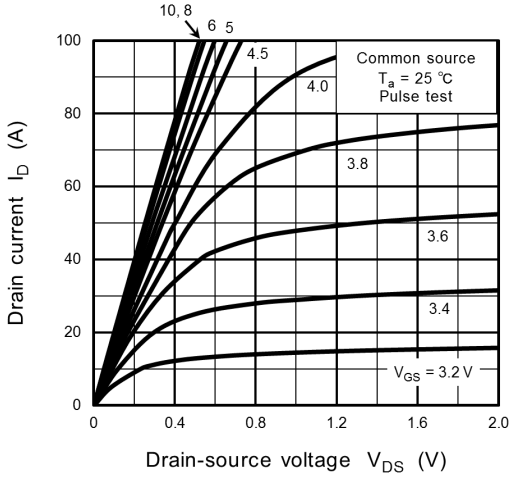



Fig. 8.2 $I_D$ - $V_{DS}$

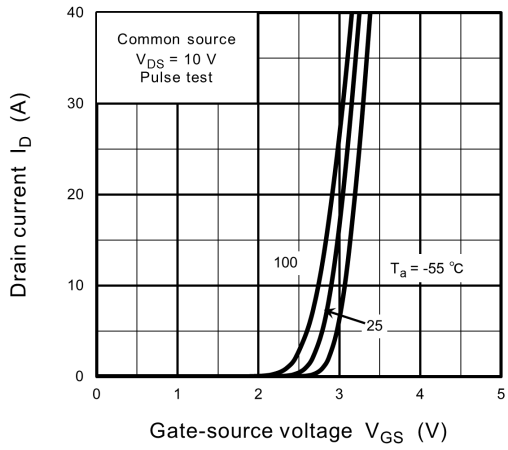



Fig. 8.3 $I_D$ - $V_{GS}$

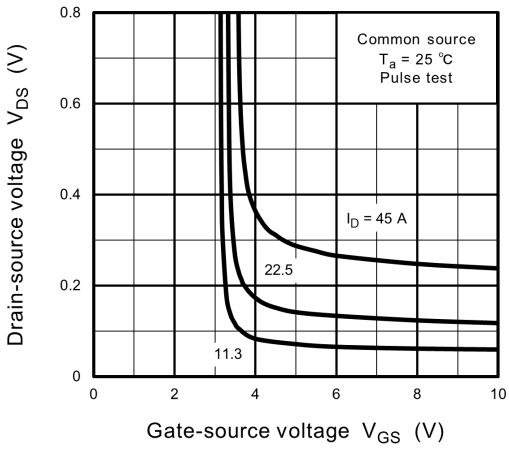



Fig. 8.4 $V_{DS}$ - $V_{GS}$

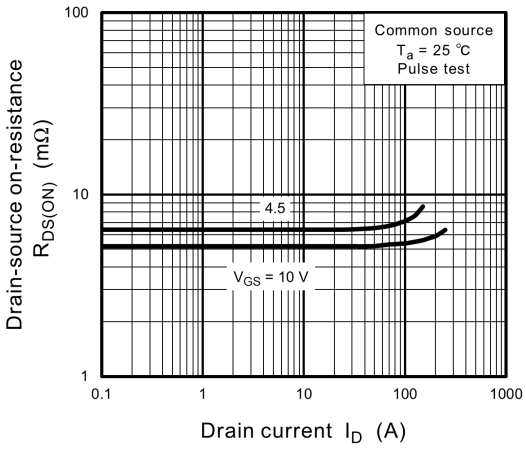



Fig. 8.5 $R_{DS(ON)}$ - $I_D$

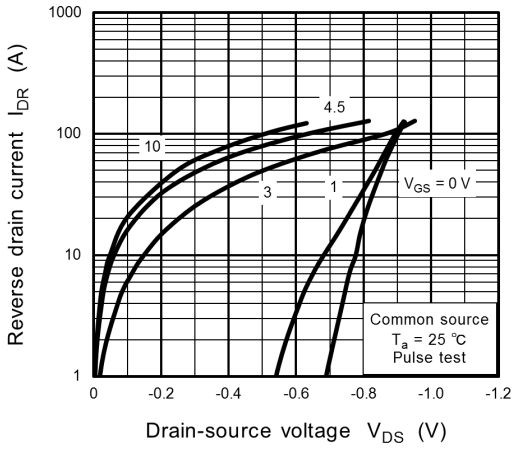



Fig. 8.6 $I_{DR}$ - $V_{DS}$

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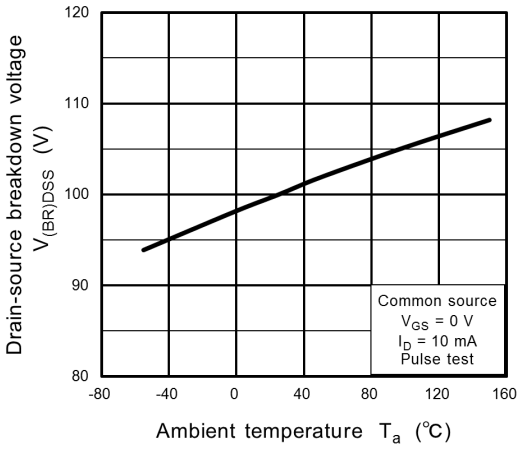



**Fig. 8.7 $V_{(BR)DSS}$ - $T_a$**

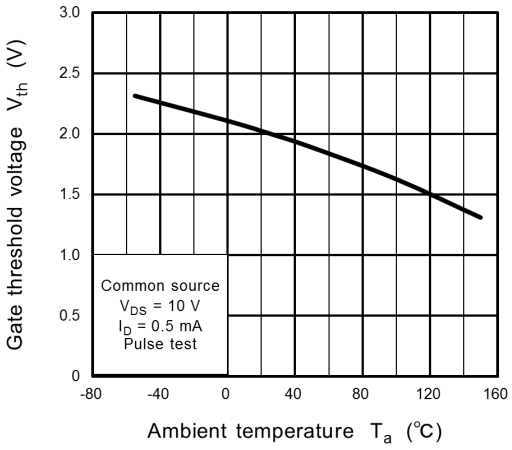



**Fig. 8.8 $V_{th}$ - $T_a$**

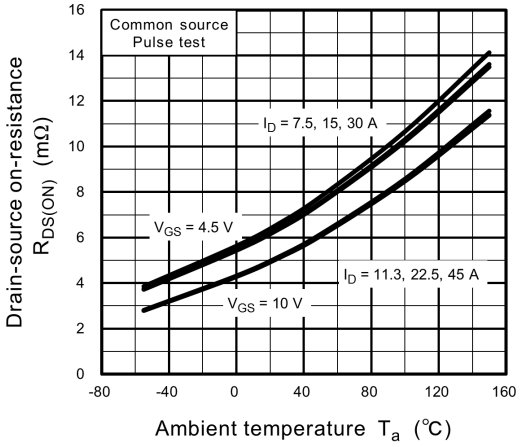



**Fig. 8.9 $R_{DS(ON)}$ - $T_a$**

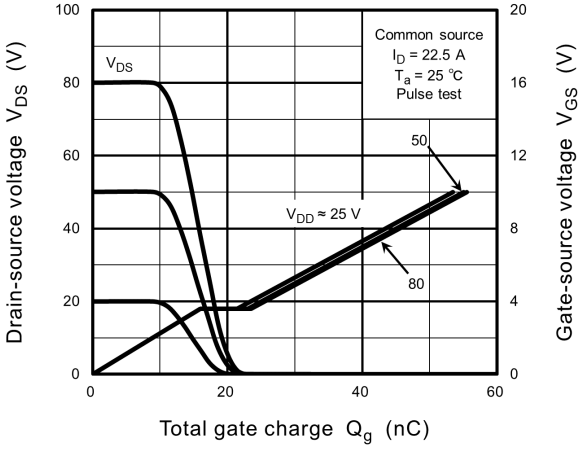



**Fig. 8.10 Dynamic Input/Output Characteristics**

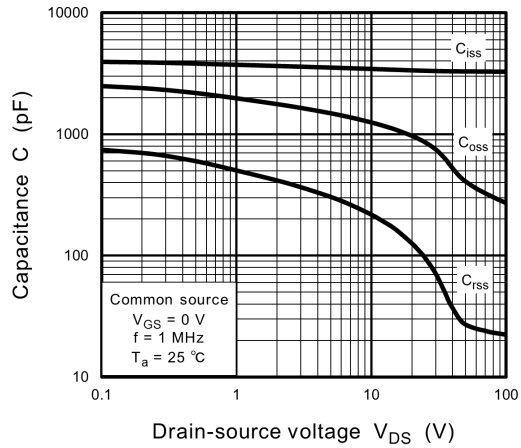



**Fig. 8.11 Capacitance - $V_{DS}$**

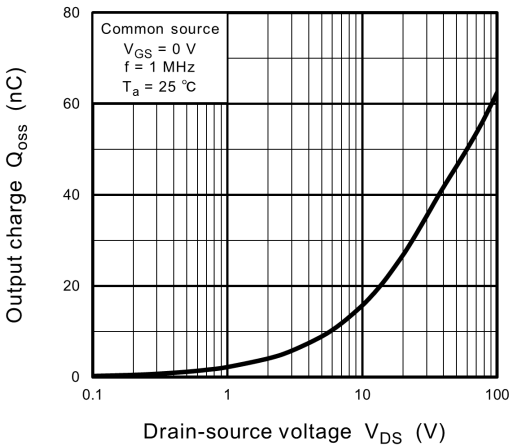



**Fig. 8.12 $Q_{oss}$ - $V_{DS}$**

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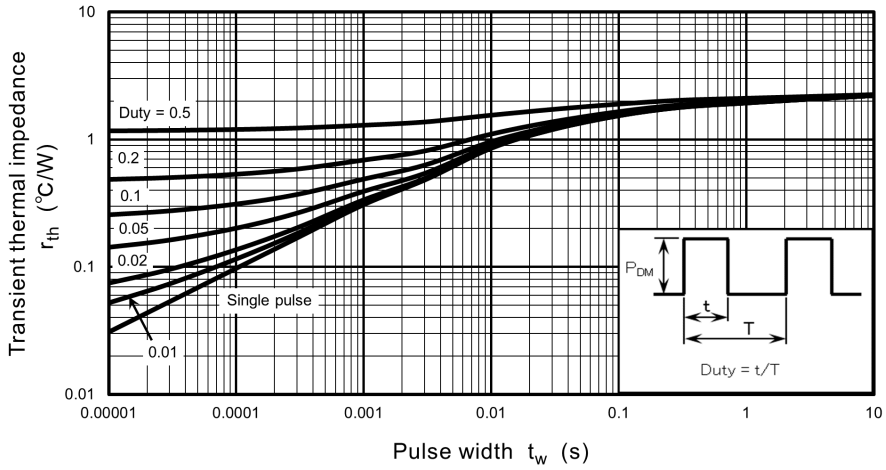



**Fig. 8.13 $r_{th}$ - $t_w$**
**(Guaranteed Maximum)**

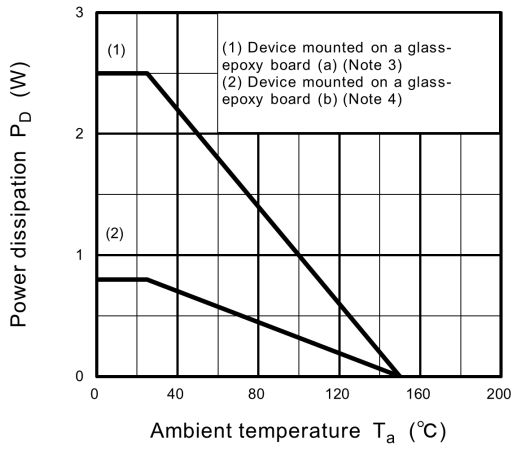



**Fig. 8.14 $P_D$ - $T_a$**
**(Guaranteed Maximum)**

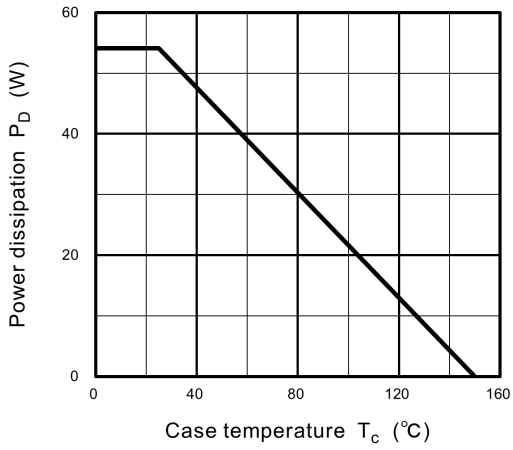



**Fig. 8.15 $P_D$ - $T_c$**
**(Guaranteed Maximum)**

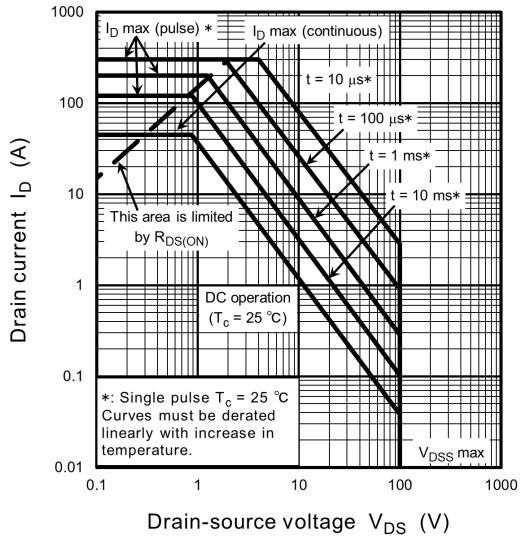


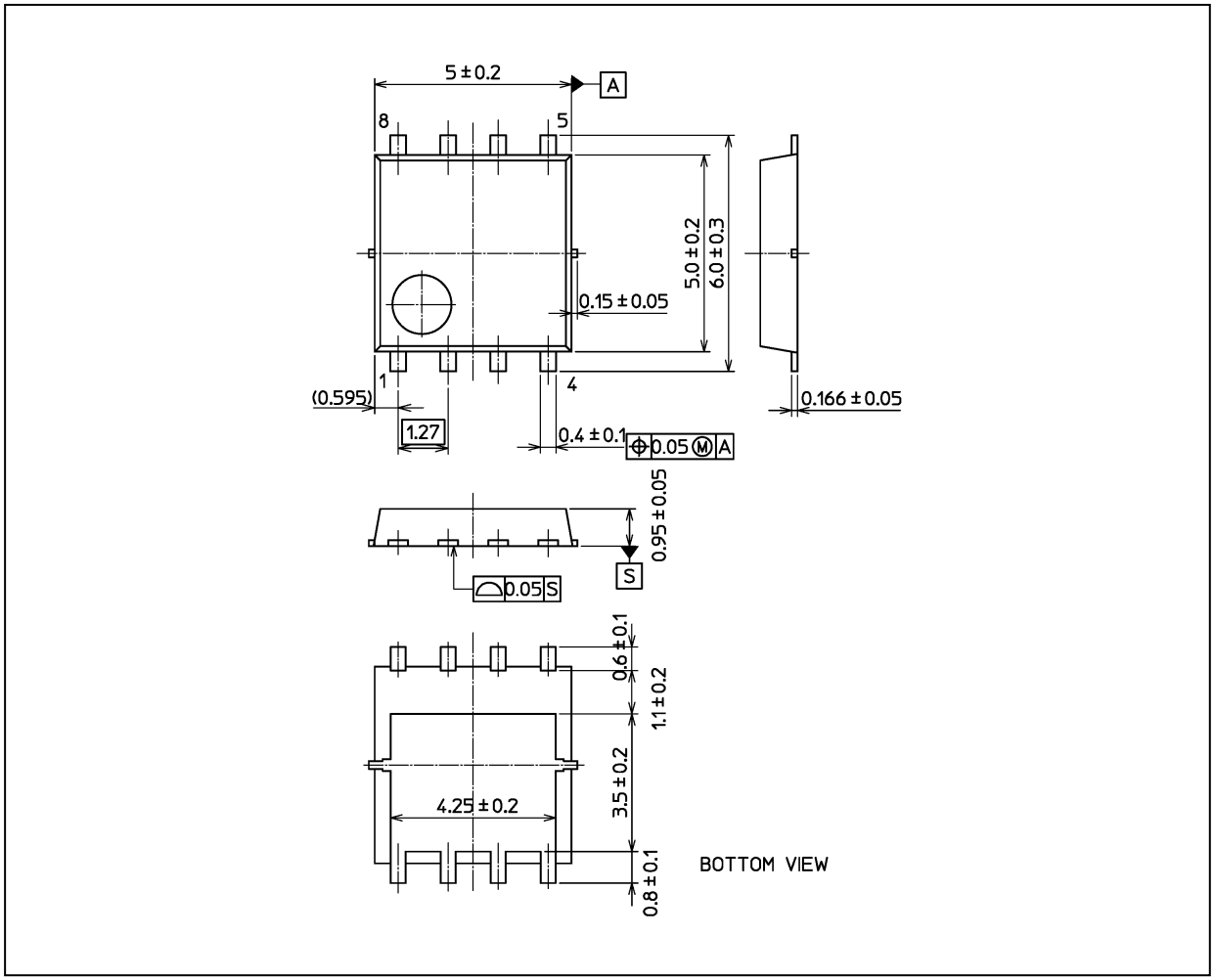

**Fig. 8.16 Safe Operating Area**
**(Guaranteed Maximum)**

Note: The above characteristics curves are presented for reference only and not guaranteed by production test, unless otherwise noted.

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## Package Dimensions

Unit: mm




Weight: 0.079 g (typ.)

| Package Name(s) |
|---|
| TOSHIBA: 2-5Q1S |
| Nickname: SOP Advance |

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