MOSFETs Silicon P-Channel MOS

SSM3J35CTC

1. Applications

- Analog Switches

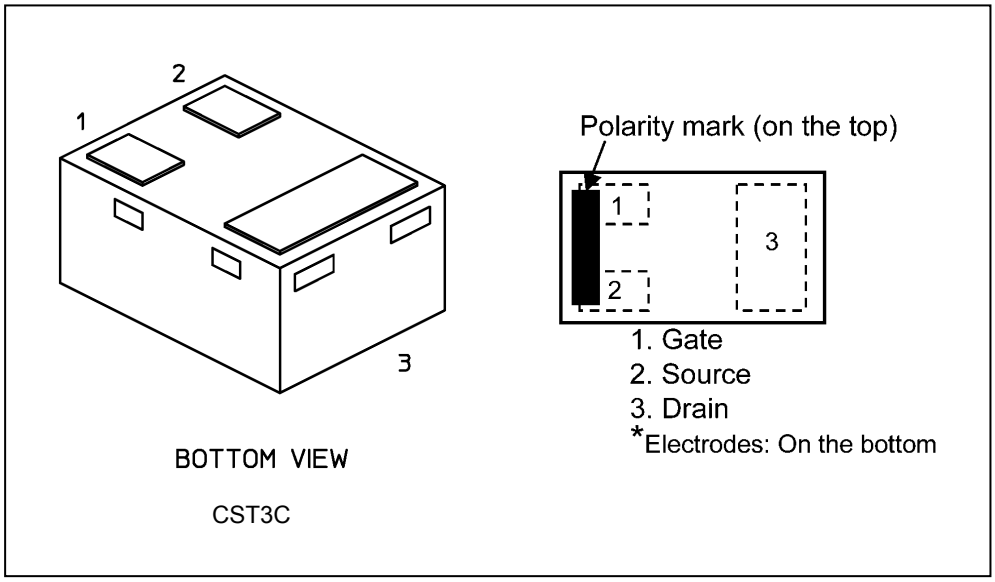
2. Features

(1) 1.2 V drive

(2) Low drain-source on-resistance

: $R_{DS(ON)}$ = 3.2 Ω (typ.) ($@V_{GS}$ = -1.2 V)
$R_{DS(ON)}$ = 2.3 Ω (typ.) ($@V_{GS}$ = -1.5 V)
$R_{DS(ON)}$ = 2.0 Ω (typ.) ($@V_{GS}$ = -1.8 V)
$R_{DS(ON)}$ = 1.5 Ω (typ.) ($@V_{GS}$ = -2.5 V)
$R_{DS(ON)}$ = 1.1 Ω (typ.) ($@V_{GS}$ = -4.5 V)

3. Packaging and Pin Assignment



Start of commercial production
2016-01

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4. Absolute Maximum Ratings (Note) (Unless otherwise specified, T_a = 25 °C)

Characteristics		Symbol	Rating	Unit
Drain-source voltage		V_{DSS}	-20	V
Gate-source voltage		V_{GSS}	±10	
Drain current (DC)	(Note 1)	I_D	-250	mA
Drain current (pulsed)	(Note 1)	I_{DP}	-600	
Power dissipation	(Note 2)	P_D	500	mW
Channel temperature		T_{ch}	150	°C
Storage temperature		T_{stg}	-55 to 150	

Note: Using continuously under heavy loads (e.g. the application of high temperature/current/voltage and the significant change in temperature, etc.) may cause this product to decrease in the reliability significantly even if the operating conditions (i.e. operating temperature/current/voltage, etc.) are within the absolute maximum ratings.
Please design the appropriate reliability upon reviewing the Toshiba Semiconductor Reliability Handbook ("Handling Precautions"/"Derating Concept and Methods") and individual reliability data (i.e. reliability test report and estimated failure rate, etc).

Note 1: Ensure that the channel temperature does not exceed 150 °C.

Note 2: Device mounted on a 25.4 mm × 25.4 mm × 1.6 mm FR4 glass epoxy board (Cu pad: 645 mm^2)

Note: This transistor is sensitive to electrostatic discharge and should be handled with care.

Note: The MOSFETs in this device are sensitive to electrostatic discharge. When handling this device, the worktables, operators, soldering irons and other objects should be protected against anti-static discharge.

Note: The channel-to-ambient thermal resistance, $R_{th(ch-a)}$, and the drain power dissipation, P_D, vary according to the board material, board area, board thickness and pad area. When using this device, be sure to take heat dissipation fully into account.

5. Electrostatic Discharge Test (T_a=25°C)

Apply voltage	Failure	Test conditions
±2000 V	0/10 pcs	C = 100 pF, R = 1.5 kΩ (JEITA ED-4701)

Note: Conducted Electrostatic Discharge Test based on JEITA ED-4701 standard, and confirmed above result.

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6. Electrical Characteristics

6.1. Static Characteristics (Unless otherwise specified, T_a = 25 °C)

Characteristics		Symbol	Test Condition	Min	Typ.	Max	Unit
Gate leakage current		I_{GSS}	V_{DS} = 0 V, V_{GS} = ±10 V	—	—	±1	μA
Drain cut-off current		I_{DSS}	V_{DS} = -20 V, V_{GS} = 0 V	—	—	-1	
Drain-source breakdown voltage		$V_{(BR)DSS}$	I_D = -1 mA, V_{GS} = 0 V	-20	—	—	V
Drain-source breakdown voltage	(Note 1)	$V_{(BR)DSX}$	I_D = -1 mA, V_{GS} = 10 V	-10	—	—	
Gate threshold voltage	(Note 2)	V_{th}	V_{DS} = -10 V, I_D = -100 μA	-0.3	—	-1	
Drain-source on-resistance	(Note 3)	$R_{DS(ON)}$	I_D = -10 mA, V_{GS} = -1.2 V	—	3.2	20	Ω
			I_D = -20 mA, V_{GS} = -1.5 V	—	2.3	4.0	
			I_D = -50 mA, V_{GS} = -1.8 V	—	2.0	2.9	
			I_D = -150 mA, V_{GS} = -2.5 V	—	1.5	2.1	
			I_D = -150 mA, V_{GS} = -4.5 V	—	1.1	1.4	
Forward transfer admittance	(Note 3)	$\|Y_{fs}\|$	V_{DS} = -10 V, I_D = -100 mA	—	430	—	mS

Note 1: If a reverse bias is applied between gate and source, this device enters $V_{(BR)DSX}$ mode. Note that the drain-source breakdown voltage is lowered in this mode.

Note 2: Let V_{th} be the voltage applied between gate and source that causes the drain current (I_D) to below (-100 μA for this device). Then, for normal switching operation, $V_{GS(ON)}$ must be higher than V_{th}, and $V_{GS(OFF)}$ must be lower than V_{th}. This relationship can be expressed as: $V_{GS(OFF)} < V_{th} < V_{GS(ON)}$.
Take this into consideration when using the device.

Note 3: Pulse measurement.

6.2. Dynamic Characteristics (Unless otherwise specified, T_a = 25 °C)

Characteristics	Symbol	Test Condition	Min	Typ.	Max	Unit
Input capacitance	C_{iss}	V_{DS} = -10 V, V_{GS} = 0 V, f = 1 MHz	—	21	42	pF
Reverse transfer capacitance	C_{rss}		—	2	—	
Output capacitance	C_{oss}		—	6	—	
Switching time (rise time)	t_r	V_{DD} = -10 V, I_D = -50 mA, V_{GS} = 0 to -4.5 V, R_G = 10 Ω Duty ≤ 1 %, V_{IN}: t_r, t_f < 5 ns, Common source, See Chapter 6.3.	—	42	—	ns
Switching time (turn-on delay time)	$t_{d(on)}$		—	17	—	
Switching time (fall time)	t_f		—	145	—	
Switching time (turn-off delay time)	$t_{d(off)}$		—	420	—	

6.3. Switching Time Test Circuit

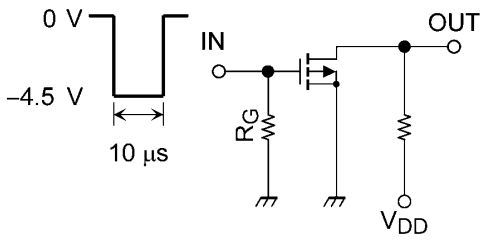


Fig. 6.3.1 Switching Time Test Circuit

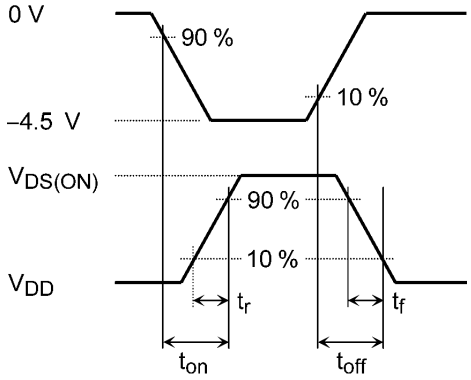


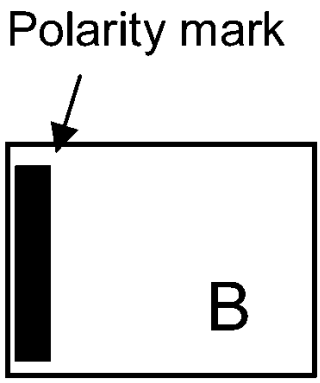
Fig. 6.3.2 Input Waveform/Output Waveform

6.4. Source-Drain Characteristics (Unless otherwise specified, T_a = 25 °C)

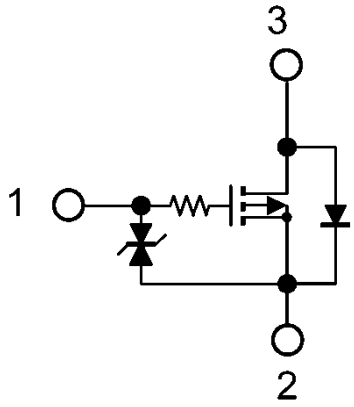
Characteristics		Symbol	Test Condition	Min	Typ.	Max	Unit
Diode forward voltage	(Note 1)	V_{DSF}	I_D = 100 mA, V_{GS} = 0 V	—	0.83	1.2	V

Note 1: Pulse measurement.

7. Marking



8. Equivalent Circuit



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9. Characteristics Curves (Note)

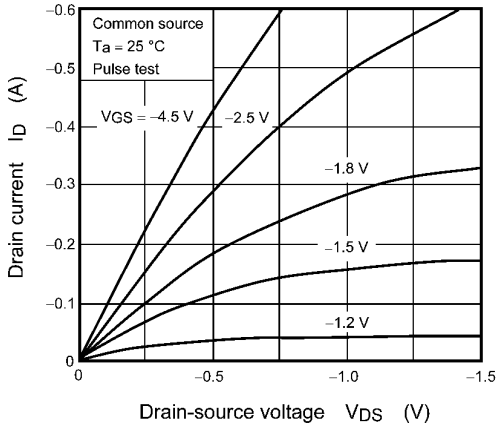


Fig. 9.1 I_D - V_{DS}

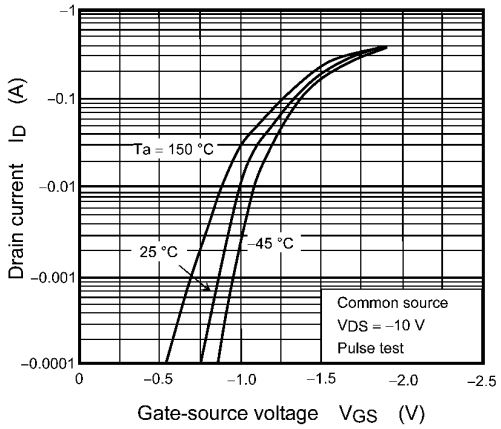


Fig. 9.2 I_D - V_{GS}

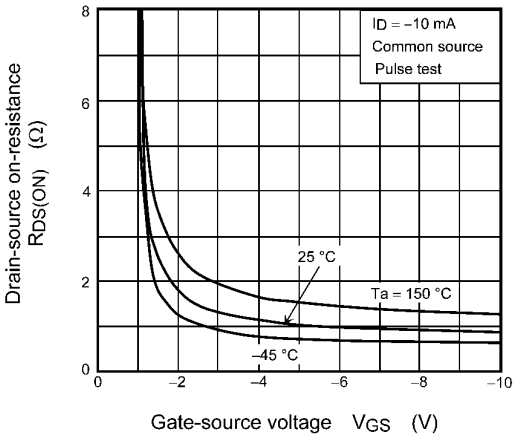


Fig. 9.3 $R_{DS(ON)}$ - V_{GS}

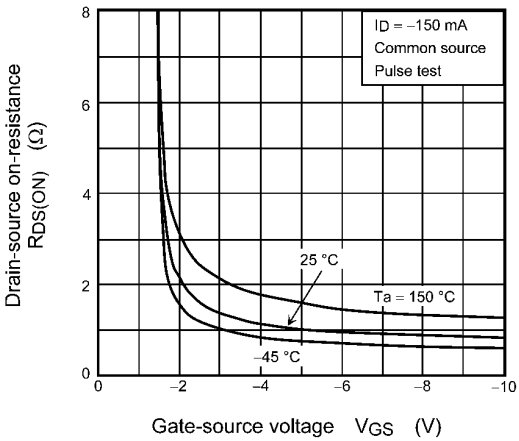


Fig. 9.4 $R_{DS(ON)}$ - V_{GS}

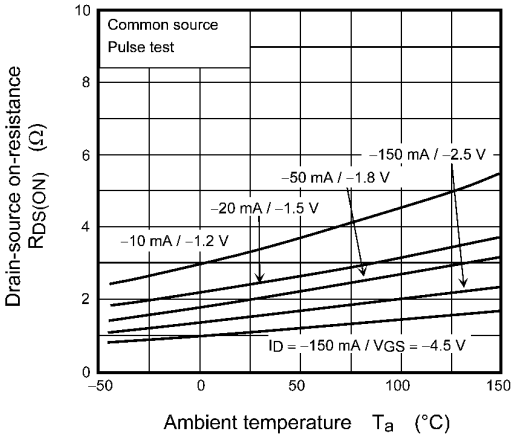


Fig. 9.5 $R_{DS(ON)}$ - T_a

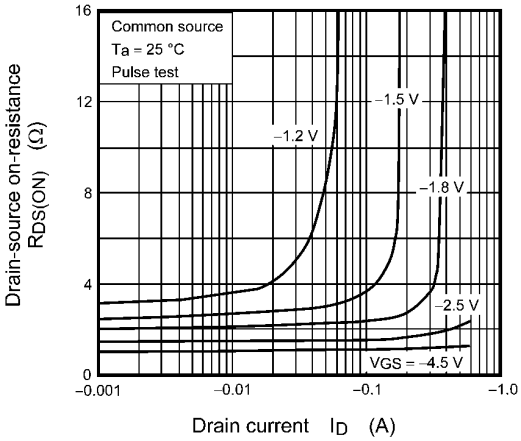


Fig. 9.6 $R_{DS(ON)}$ - I_D

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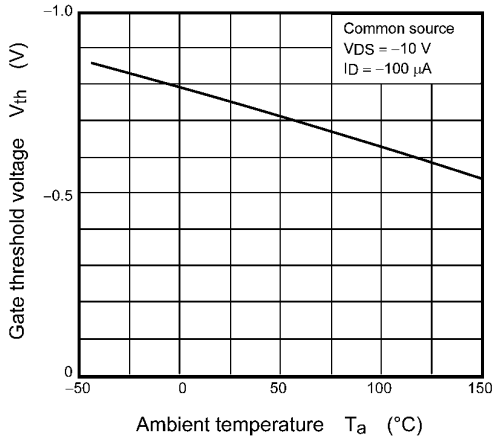


Fig. 9.7 V_{th} - T_a

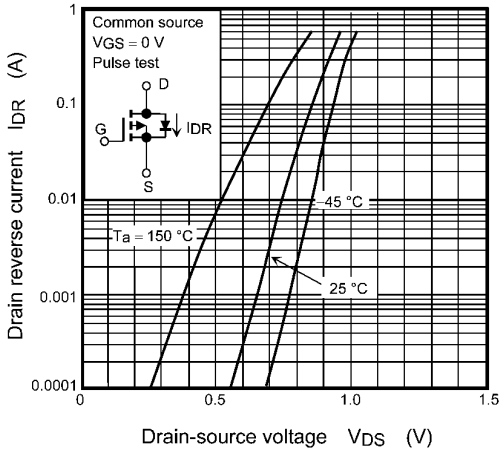


Fig. 9.8 I_{DR} - V_{DS}

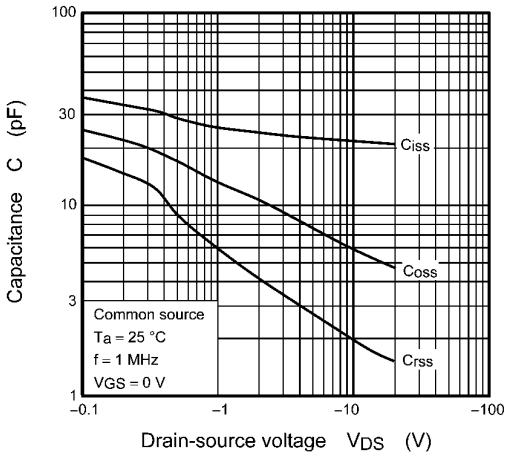


Fig. 9.9 C - V_{DS}

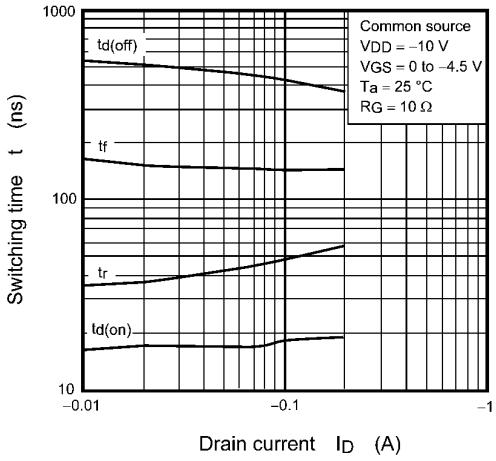


Fig. 9.10 t - I_D

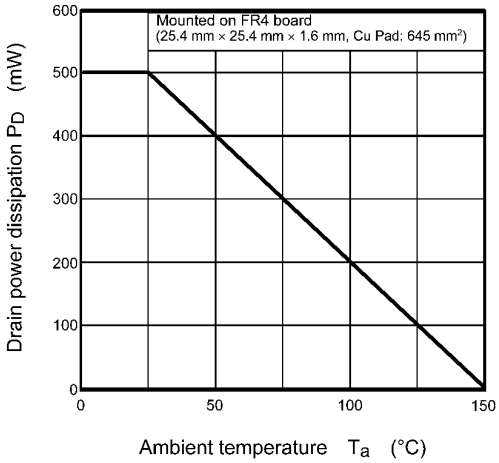


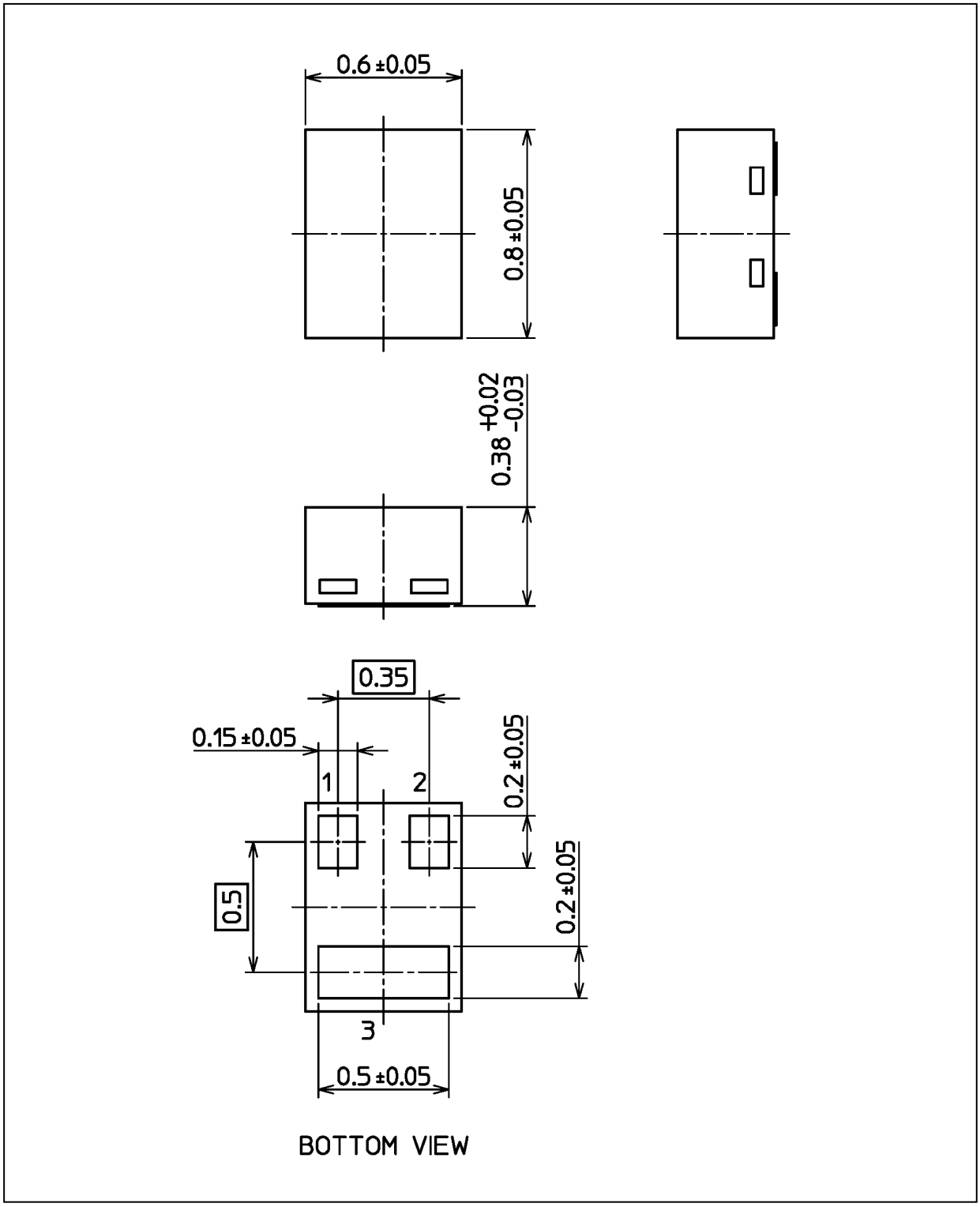
Fig. 9.11 P_D - T_a

Note: The above characteristics curves are presented for reference only and not guaranteed by production test, unless otherwise noted.

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Package Dimensions

Unit: mm



Weight: 0.55 mg (typ.)

Package Name(s)
Nickname: CST3C

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