MOSFETs Silicon N-Channel MOS

SSM3K35AFS

1. Applications

- High-Speed Switching
- Analog Switches

2. Features

(1) 1.2 V drive

(2) Low drain-source on-resistance

: $R_{DS(ON)}$ = 9.0 Ω (max) (@V_{GS} = 1.2 V, I_D = 10 mA)

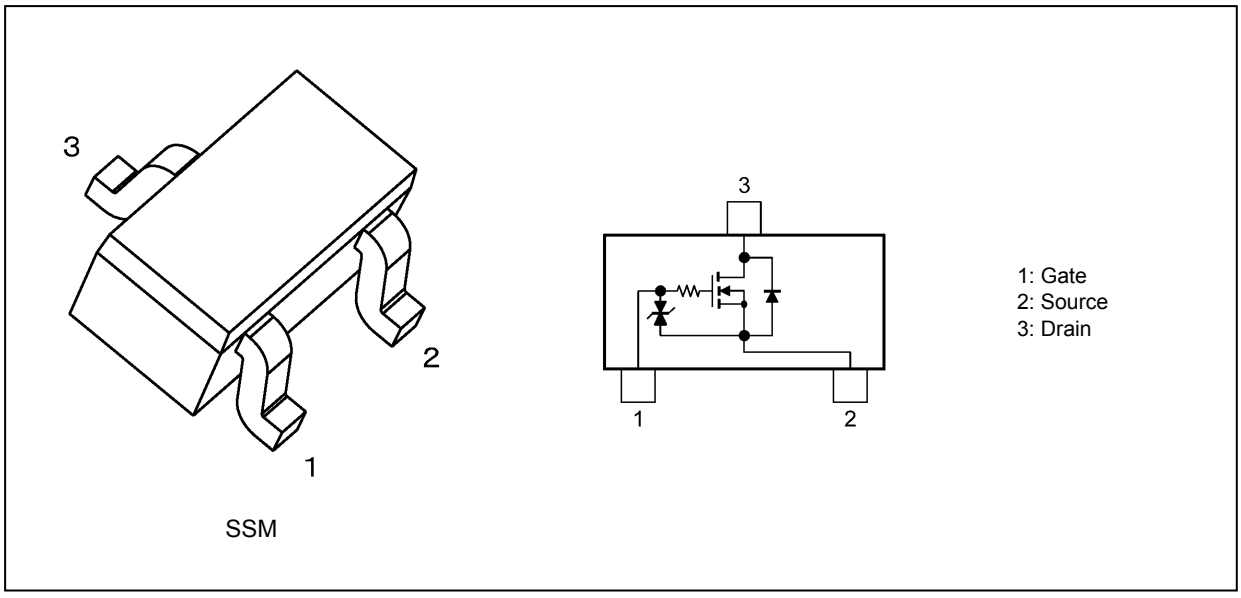
$R_{DS(ON)}$ = 3.1 Ω (max) (@V_{GS} = 1.5 V, I_D = 20 mA)

$R_{DS(ON)}$ = 2.4 Ω (max) (@V_{GS} = 1.8 V, I_D = 150 mA)

$R_{DS(ON)}$ = 1.6 Ω (max) (@V_{GS} = 2.5 V, I_D = 150 mA)

$R_{DS(ON)}$ = 1.1 Ω (max) (@V_{GS} = 4.5 V, I_D = 150 mA)

3. Packaging and Pin Assignment



Start of commercial production
2016-10

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4. Absolute Maximum Ratings (Note) (Unless otherwise specified, T_a = 25 °C)

Characteristics		Symbol	Rating	Unit
Drain-source voltage		V_{DSS}	20	V
Gate-source voltage		V_{GSS}	±10	
Drain current	(Note 1)	I_D	250	mA
Drain current (pulsed)	(Note 1)	I_{DP}	600	
Power dissipation	(Note 2)	P_D	150	mW
Power dissipation	(Note 3)		500	
Channel temperature		T_{ch}	150	°C
Storage temperature		T_{stg}	-55 to 150	°C

Note: Using continuously under heavy loads (e.g. the application of high temperature/current/voltage and the significant change in temperature, etc.) may cause this product to decrease in the reliability significantly even if the operating conditions (i.e. operating temperature/current/voltage, etc.) are within the absolute maximum ratings.
Please design the appropriate reliability upon reviewing the Toshiba Semiconductor Reliability Handbook ("Handling Precautions"/"Derating Concept and Methods") and individual reliability data (i.e. reliability test report and estimated failure rate, etc).

Note 1: Ensure that the channel temperature does not exceed 150 °C.

Note 2: Mounted on an FR4 board (25.4 mm × 25.4 mm × 1.6 mm, Cu pad: 0.36 mm^2 × 3)

Note 3: Mounted on an FR4 board (25.4 mm × 25.4 mm × 1.6 mm, Cu pad: 645 mm^2)

Note: The MOSFETs in this device are sensitive to electrostatic discharge. When handling this device, the worktables, operators, soldering irons and other objects should be protected against anti-static discharge.

Note: The channel-to-ambient thermal resistance, $R_{th(ch-a)}$, and the drain power dissipation, P_D, vary according to the board material, board area, board thickness and pad area. When using this device, be sure to take heat dissipation fully into account.

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5. Electrical Characteristics

5.1. Static Characteristics (Unless otherwise specified, T_a = 25 °C)

Characteristics		Symbol	Test Condition	Min	Typ.	Max	Unit
Gate leakage current		I_{GSS}	V_{GS} = ±10 V, V_{DS} = 0 V	—	—	±1	μA
Drain cut-off current		I_{DSS}	V_{DS} = 20 V, V_{GS} = 0 V	—	—	1	
Drain-source breakdown voltage		$V_{(BR)DSS}$	I_D = 1 mA, V_{GS} = 0 V	20	—	—	V
Gate threshold voltage	(Note 1)	V_{th}	V_{DS} = 10 V, I_D = 100 μA	0.35	—	1.0	V
Drain-source on-resistance	(Note 2)	$R_{DS(ON)}$	I_D = 150 mA, V_{GS} = 4.5 V	—	0.75	1.1	Ω
			I_D = 150 mA, V_{GS} = 2.5 V	—	1.1	1.6	
			I_D = 150 mA, V_{GS} = 1.8 V	—	1.4	2.4	
			I_D = 20 mA, V_{GS} = 1.5 V	—	1.7	3.1	
			I_D = 10 mA, V_{GS} = 1.2 V	—	2.4	9.0	
			I_D = 150 mA, V_{GS} = 4.5 V, T_j = 125 °C	—	1.25	2.5	
Forward transfer admittance	(Note 2)	$\|Y_{fs}\|$	V_{DS} = 10 V, I_D = 150 mA	—	0.5	—	S
Reverse drain current (pulsed)	(Note 2)	I_{DRP}	—	—	—	600	mA

Note 1: Let V_{th} be the voltage applied between gate and source that causes the drain current (I_D) to below (100 μA for this device). Then, for normal switching operation, $V_{GS(ON)}$ must be higher than V_{th}, and $V_{GS(OFF)}$ must be lower than V_{th}. This relationship can be expressed as: $V_{GS(OFF)} < V_{th} < V_{GS(ON)}$.
Take this into consideration when using the device.

Note 2: Pulse measurement.

5.2. Dynamic Characteristics (Unless otherwise specified, T_a = 25 °C)

Characteristics	Symbol	Test Condition	Min	Typ.	Max	Unit
Input capacitance	C_{iss}	V_{DS} = 10 V, V_{GS} = 0 V, f = 1 MHz	—	18	36	pF
Reverse transfer capacitance	C_{rss}		—	5	10	
Output capacitance	C_{oss}		—	6	12	
Switching time (turn-on delay time)	$t_{d(on)}$	V_{DD} = 10 V, I_D = 75 mA, V_{GS} = 0 to 4.5 V, R_G = 10 Ω	—	2	—	ns
Switching time (rise time)	t_r		—	2	—	
Switching time (turn-off delay time)	$t_{d(off)}$		—	6.5	—	
Switching time (fall time)	t_f		—	5.5	—	

5.3. Switching Time Test Circuit

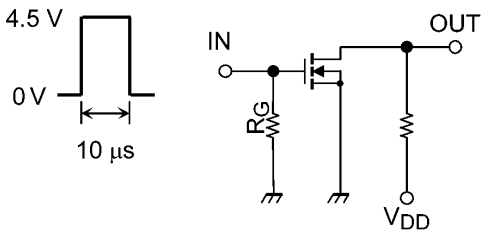


Fig. 5.3.1 Switching Time Test Circuit

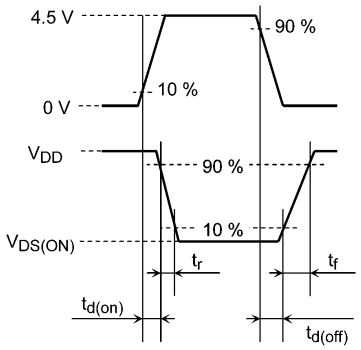


Fig. 5.3.2 Input Waveform/Output Waveform

5.4. Gate Charge Characteristics (Unless otherwise specified, T_a = 25 °C)

Characteristics	Symbol	Test Condition	Min	Typ.	Max	Unit
Total gate charge (gate-source plus gate-drain)	Q_g	V_{DD} = 10 V, I_D = 200 mA, V_{GS} = 4.5 V	—	0.34	—	nC
Gate-source charge 1	Q_{gs1}		—	0.09	—	
Gate-drain charge	Q_{gd}		—	0.16	—	

5.5. Source-Drain Characteristics (Unless otherwise specified, T_a = 25 °C)

Characteristics	Symbol	Test Condition	Min	Typ.	Max	Unit
Diode forward voltage (Note 1)	V_{DSF}	I_D = -150 mA, V_{GS} = 0 V	—	-0.8	-1.2	V

Note 1: Pulse measurement.

6. Marking

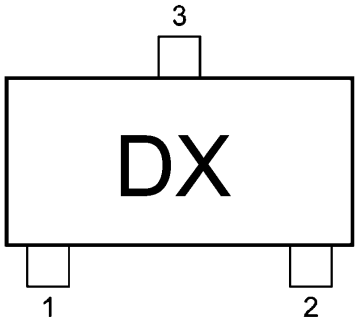


Fig. 6.1 Marking

7. Characteristics Curves (Note)

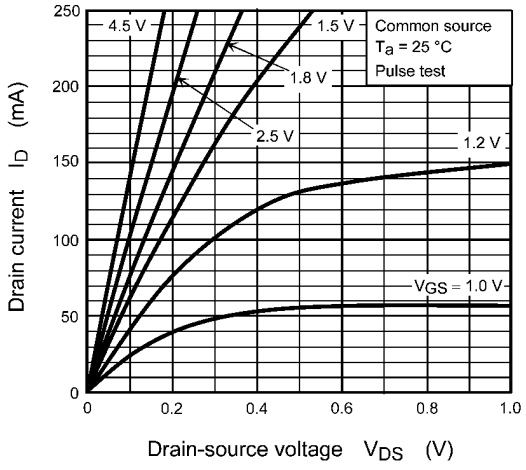


Fig. 7.1 I_D - V_{DS}

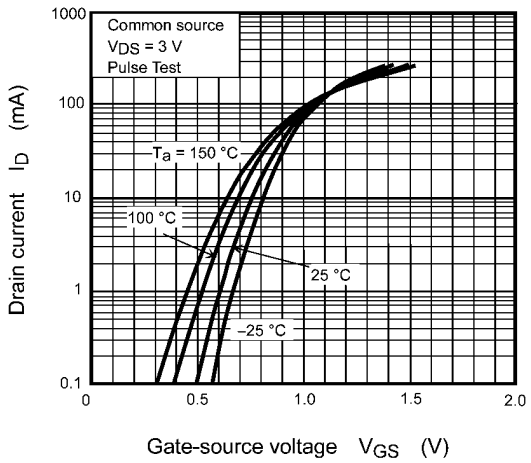


Fig. 7.2 I_D - V_{GS}

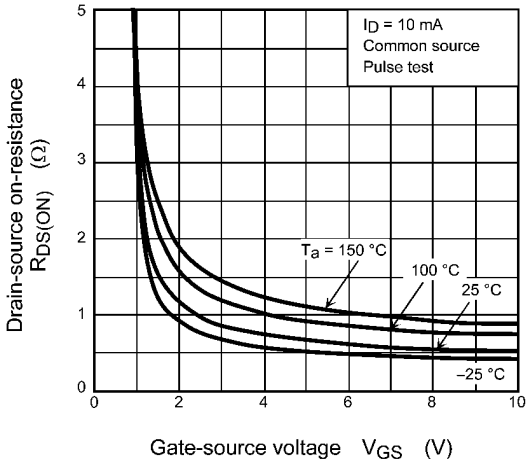


Fig. 7.3 $R_{DS(ON)}$ - V_{GS}

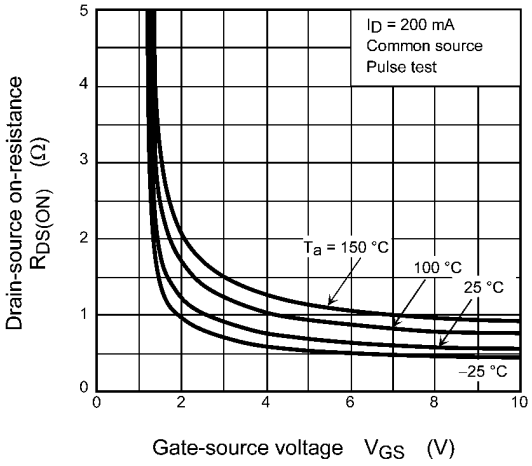


Fig. 7.4 $R_{DS(ON)}$ - V_{GS}

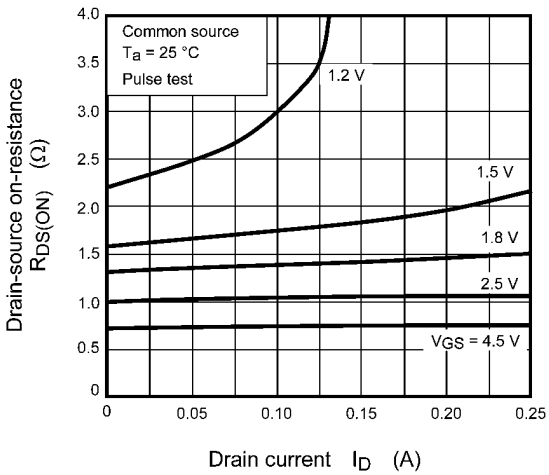


Fig. 7.5 $R_{DS(ON)}$ - I_D

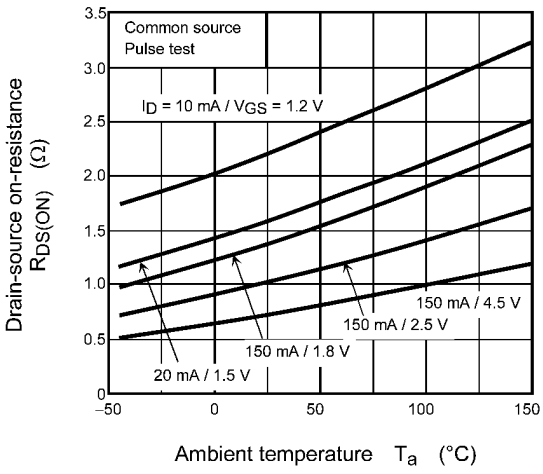


Fig. 7.6 $R_{DS(ON)}$ - T_a

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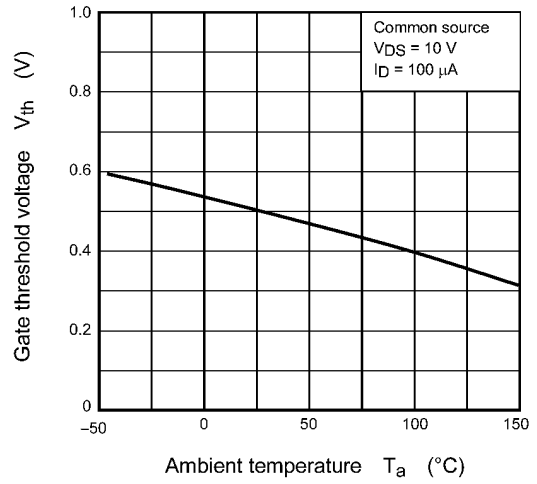


Fig. 7.7 V_{th} - T_a

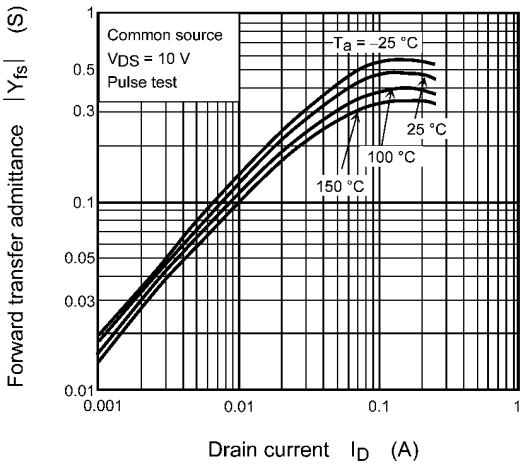


Fig. 7.8 $|Y_{fs}|$ - I_D

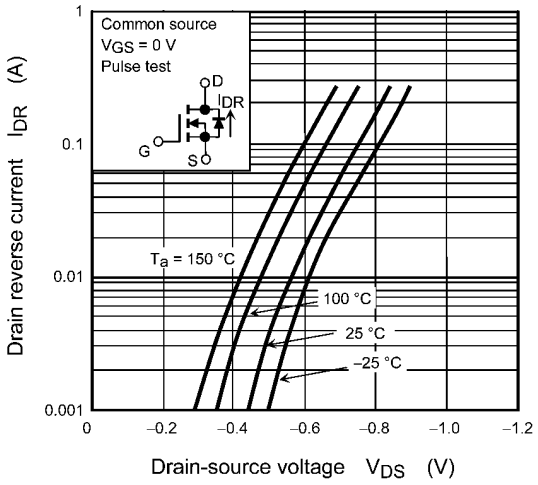


Fig. 7.9 I_{DR} - V_{DS}

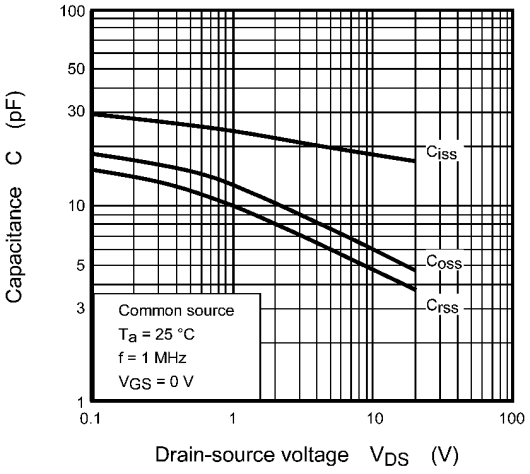


Fig. 7.10 C - V_{DS}

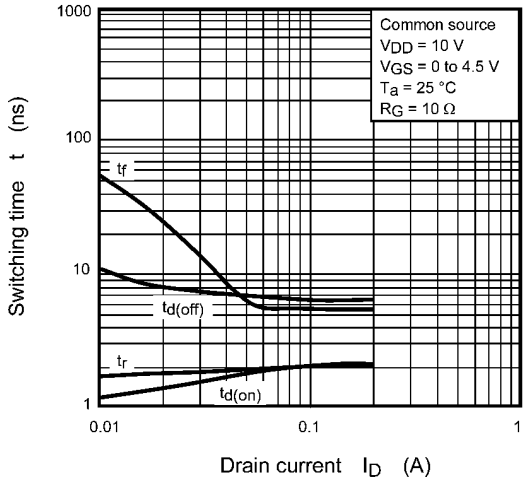


Fig. 7.11 t - I_D

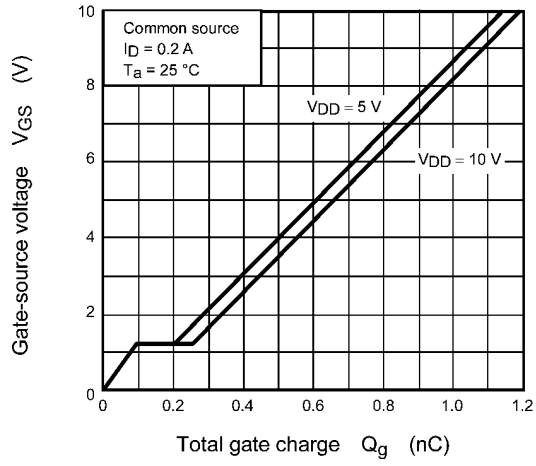


Fig. 7.12 Dynamic Input Characteristics

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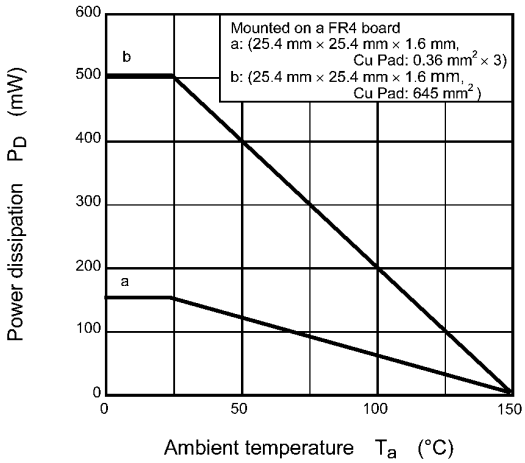
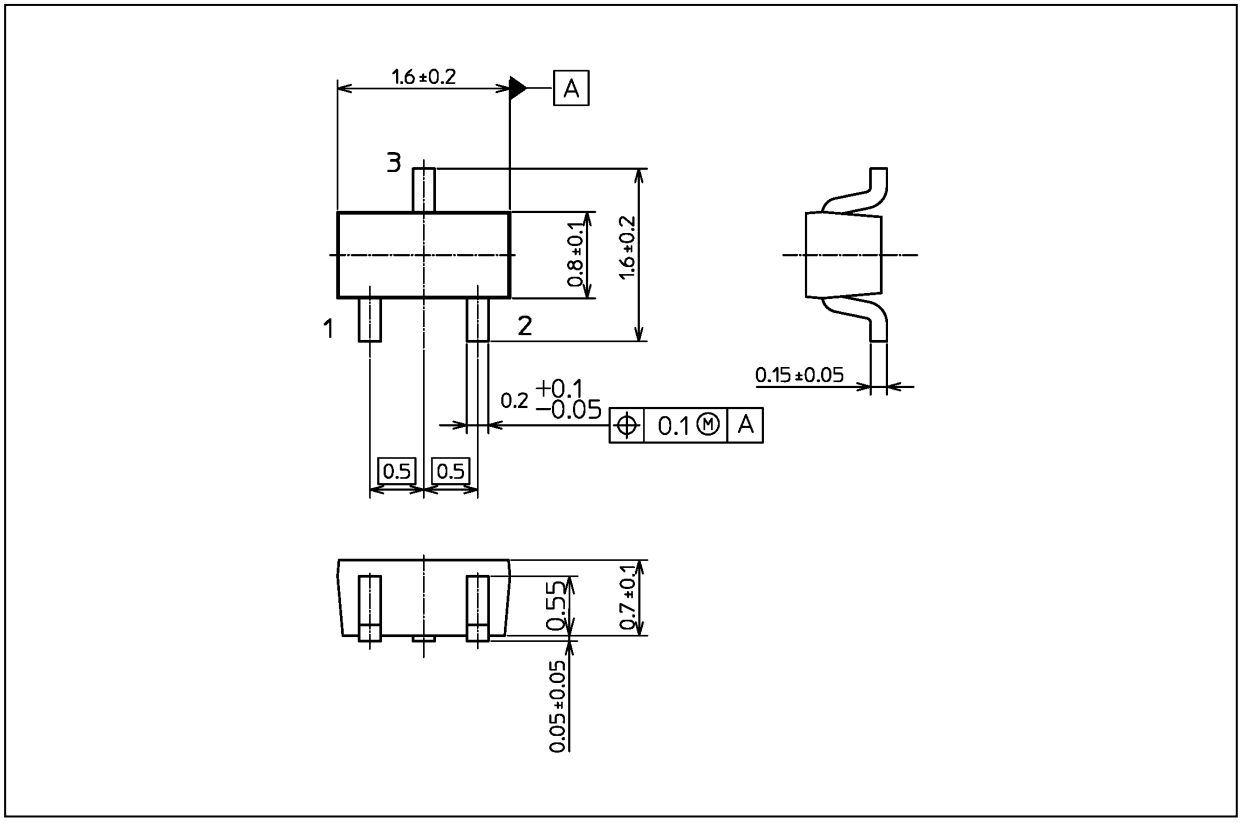


Fig. 7.13 P_D - T_a

Note: The above characteristics curves are presented for reference only and not guaranteed by production test, unless otherwise noted.

Package Dimensions

Unit: mm



Weight: 2.4 mg (typ.)

Package Name(s)
JEDEC: SOT-416
Nickname: SSM

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