MOSFETs Silicon N-channel MOS (U-MOSⅧ-H)

TK40A10N1

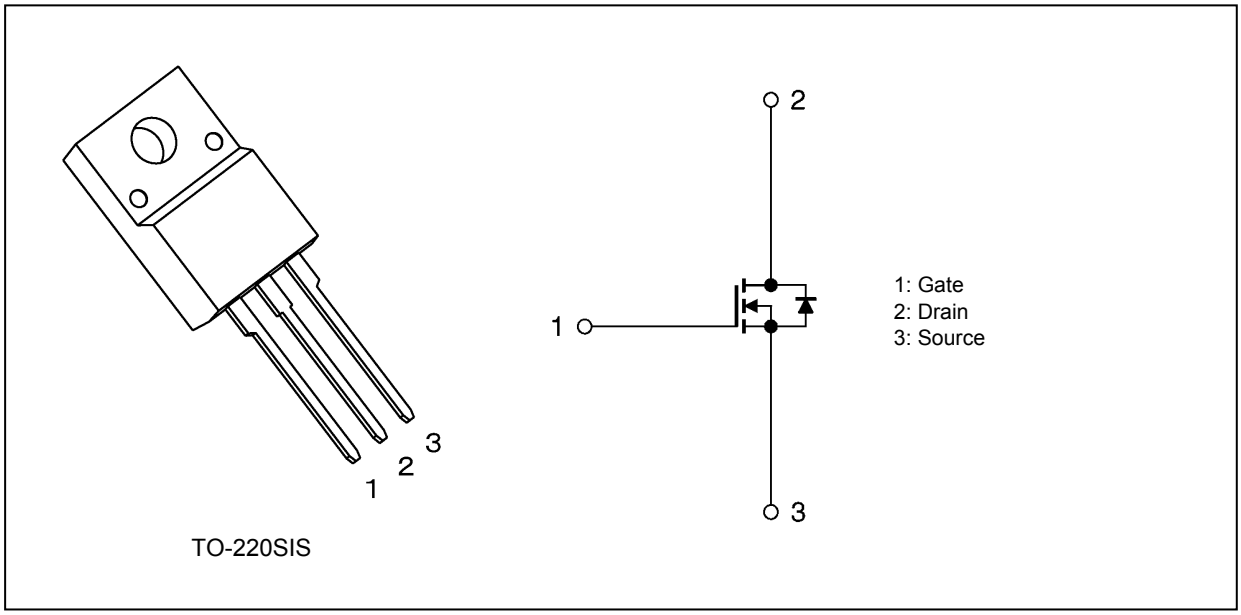
1. Applications

- Switching Voltage Regulators

2. Features

(1) Low drain-source on-resistance: $R_{DS(ON)}$ = 6.8 mΩ (typ.) (V_{GS} = 10 V)
(2) Low leakage current: I_{DSS} = 10 μA (max) (V_{DS} = 100 V)
(3) Enhancement mode: V_{th} = 2.0 to 4.0 V (V_{DS} = 10 V, I_D = 0.5 mA)

3. Packaging and Internal Circuit



4. Absolute Maximum Ratings (Note) (T_a = 25°C unless otherwise specified)

Characteristics			Symbol	Rating	Unit
Drain-source voltage			V_{DSS}	100	V
Gate-source voltage			V_{GSS}	±20	
Drain current (DC)	(Silicon limit)	(Note 1,2)	I_D	90	A
Drain current (DC)	(T_c = 25°C)	(Note 1)	I_D	40	
Drain current (pulsed)	(t = 1 ms)	(Note 1)	I_{DP}	171	
Power dissipation	(T_c = 25°C)		P_D	35	W
Single-pulse avalanche energy		(Note 3)	E_{AS}	74	mJ
Avalanche current			I_{AR}	40	A
Channel temperature			T_{ch}	150	°C
Storage temperature			T_{stg}	-55 to 150	

Note: Using continuously under heavy loads (e.g. the application of high temperature/current/voltage and the significant change in temperature, etc.) may cause this product to decrease in the reliability significantly even if the operating conditions (i.e. operating temperature/current/voltage, etc.) are within the absolute maximum ratings.
Please design the appropriate reliability upon reviewing the Toshiba Semiconductor Reliability Handbook ("Handling Precautions"/"Derating Concept and Methods") and individual reliability data (i.e. reliability test report and estimated failure rate, etc).

Start of commercial production
2011-09

5. Thermal Characteristics

Characteristics	Symbol	Max	Unit
Channel-to-case thermal resistance	$R_{th(ch-c)}$	3.57	°C/W
Channel-to-ambient thermal resistance	$R_{th(ch-a)}$	62.5	

Note 1: Ensure that the channel temperature does not exceed 150°C.
Note 2: Limited by silicon chip capability.
Note 3: V_{DD} = 80 V, T_{ch} = 25°C (initial), L = 35.9 μH, I_{AR} = 40 A

Note: This transistor is sensitive to electrostatic discharge and should be handled with care.

6. Electrical Characteristics

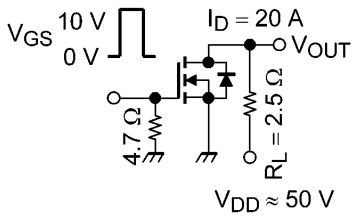
6.1. Static Characteristics (T_a = 25°C unless otherwise specified)

Characteristics	Symbol	Test Condition	Min	Typ.	Max	Unit
Gate leakage current	I_{GSS}	V_{GS} = ±20 V, V_{DS} = 0 V	—	—	±0.1	μA
Drain cut-off current	I_{DSS}	V_{DS} = 100 V, V_{GS} = 0 V	—	—	10	
Drain-source breakdown voltage	$V_{(BR)DSS}$	I_D = 10 mA, V_{GS} = 0 V	100	—	—	V
Drain-source breakdown voltage (Note 4)	$V_{(BR)DSX}$	I_D = 10 mA, V_{GS} = -20 V	65	—	—	
Gate threshold voltage	V_{th}	V_{DS} = 10 V, I_D = 0.5 mA	2.0	—	4.0	
Drain-source on-resistance	$R_{DS(ON)}$	V_{GS} = 10 V, I_D = 20 A	—	6.8	8.2	mΩ

Note 4: If a reverse bias is applied between gate and source, this device enters $V_{(BR)DSX}$ mode. Note that the drain-source breakdown voltage is lowered in this mode.

6.2. Dynamic Characteristics (T_a = 25°C unless otherwise specified)

Characteristics	Symbol	Test Condition	Min	Typ.	Max	Unit
Input capacitance	C_{iss}	V_{DS} = 50 V, V_{GS} = 0 V, f = 1 MHz	—	3000	—	pF
Reverse transfer capacitance	C_{rss}		—	29	—	
Output capacitance	C_{oss}		—	520	—	
Gate resistance	r_g	—	—	2.8	—	Ω
Switching time (rise time)	t_r	See Figure 6.2.1	—	14	—	ns
Switching time (turn-on time)	t_{on}		—	35	—	
Switching time (fall time)	t_f		—	21	—	
Switching time (turn-off time)	t_{off}		—	57	—	



Duty ≤ 1%, t_w = 10 μs

Fig. 6.2.1 Switching Time Test Circuit

6.3. Gate Charge Characteristics (T_a = 25°C unless otherwise specified)

Characteristics	Symbol	Test Condition	Min	Typ.	Max	Unit
Total gate charge (gate-source plus gate-drain)	Q_g	V_{DD} ≈ 80 V, V_{GS} = 10 V, I_D = 40 A	—	49	—	nC
Gate-source charge 1	Q_{gs1}		—	18	—	
Gate-drain charge	Q_{gd}		—	14	—	
Gate switch charge	Q_{SW}		—	21	—	

6.4. Source-Drain Characteristics (T_a = 25°C unless otherwise specified)

Characteristics		Symbol	Test Condition	Min	Typ.	Max	Unit
Reverse drain current (DC)	(Note 5)	I_{DR}	—	—	—	40	A
Reverse drain current (pulsed)	(Note 5)	I_{DRP}	—	—	—	171	
Diode forward voltage		V_{DSF}	I_{DR} = 40 A, V_{GS} = 0 V	—	—	-1.2	V
Reverse recovery time	(Note 6)	t_{rr}	I_{DR} = 40 A, V_{GS} = 0 V $-dI_{DR}/dt$ = 100 A/μs	—	67	—	ns
Reverse recovery charge	(Note 6)	Q_{rr}		—	130	—	nC

Note 5: Ensure that the channel temperature does not exceed 150°C.
Note 6: Ensure that V_{DS} peak does not exceed V_{DSS}.

7. Marking (Note)

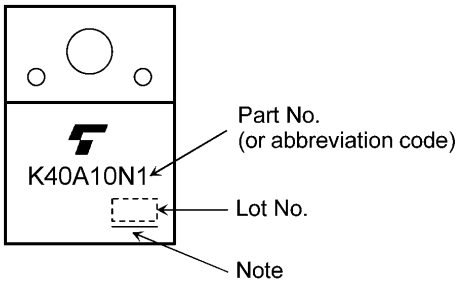


Fig. 7.1 Marking

Note: A line under a Lot No. identifies the indication of product Labels.
Not underlined: [[Pb]]/INCLUDES > MCV
Underlined: [[G]]/RoHS COMPATIBLE or [[G]]/RoHS [[Pb]]
Please contact your TOSHIBA sales representative for details as to environmental matters such as the RoHS compatibility of Product.
The RoHS is the Directive 2011/65/EU of the European Parliament and of the Council of 8 June 2011 on the restriction of the use of certain hazardous substances in electrical and electronic equipment.

8. Characteristics Curves (Note)

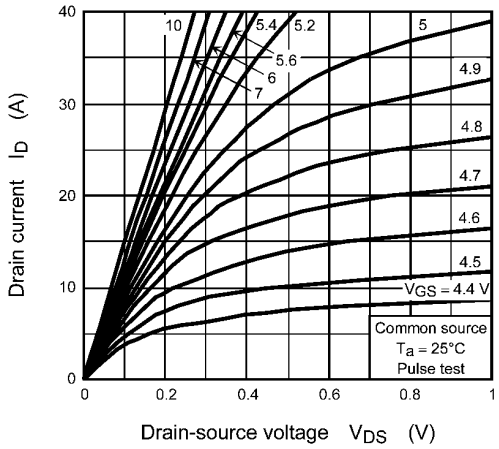


Fig. 8.1 I_D - V_{DS}

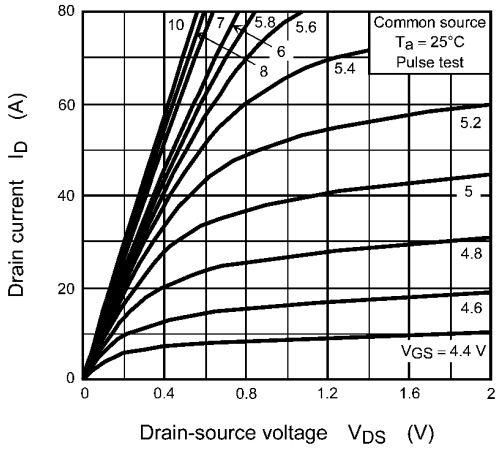


Fig. 8.2 I_D - V_{DS}

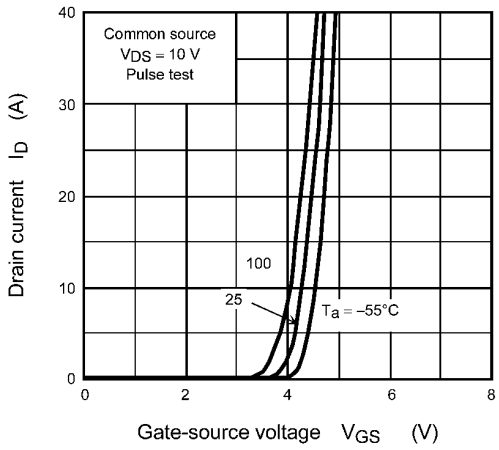


Fig. 8.3 I_D - V_{GS}

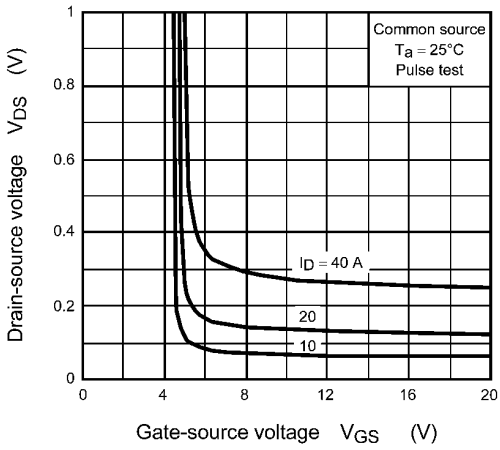


Fig. 8.4 V_{DS} - V_{GS}

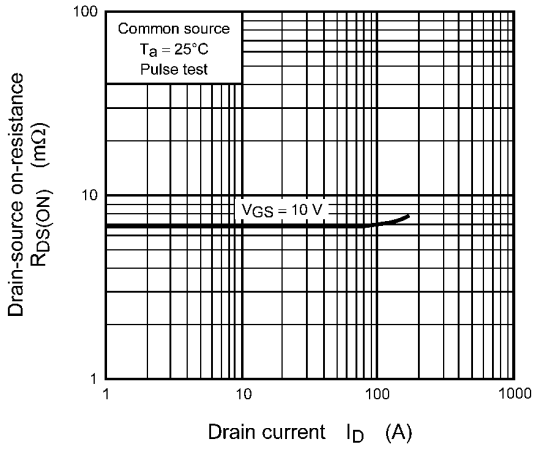


Fig. 8.5 $R_{DS(ON)}$ - I_D

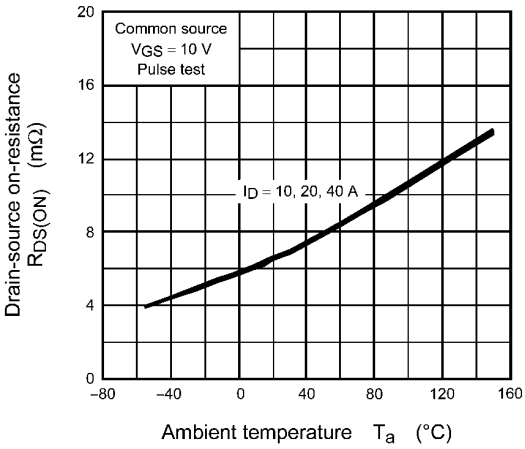


Fig. 8.6 $R_{DS(ON)}$ - T_a

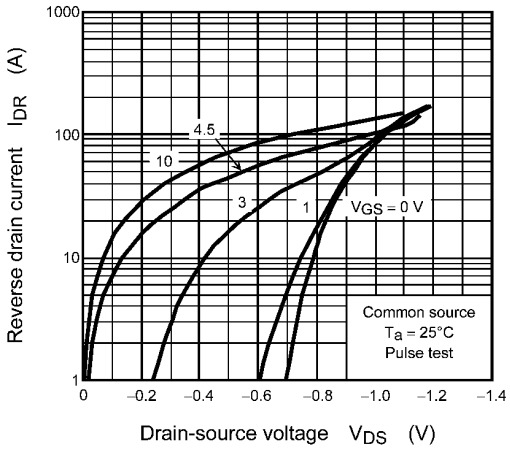


Fig. 8.7 I_{DR} - V_{DS}

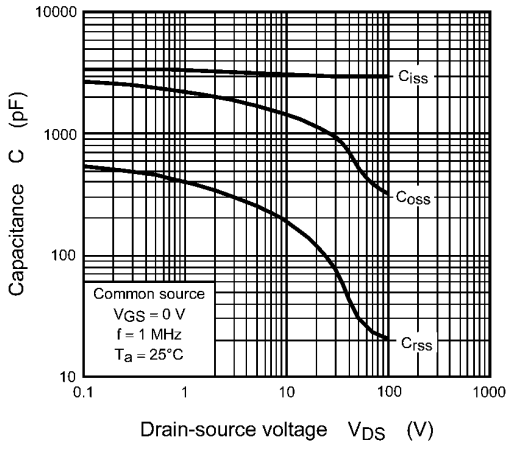


Fig. 8.8 Capacitance - V_{DS}

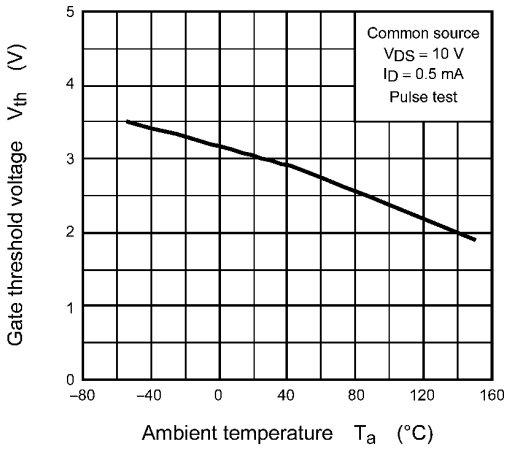


Fig. 8.9 V_{th} - T_a

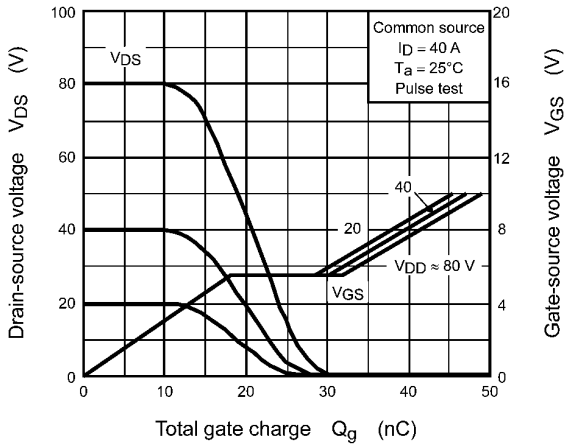


Fig. 8.10 Dynamic Input/Output Characteristics

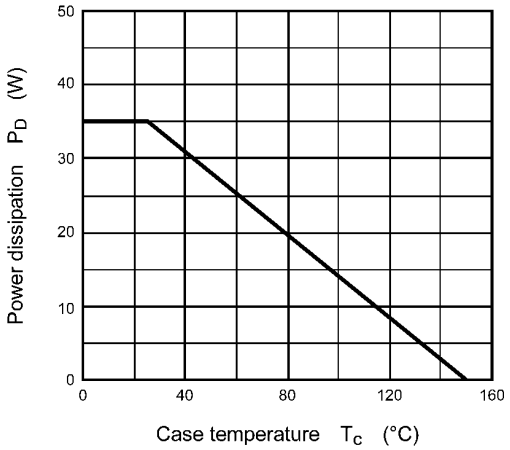


Fig. 8.11 P_D - T_c
(Guaranteed Maximum)

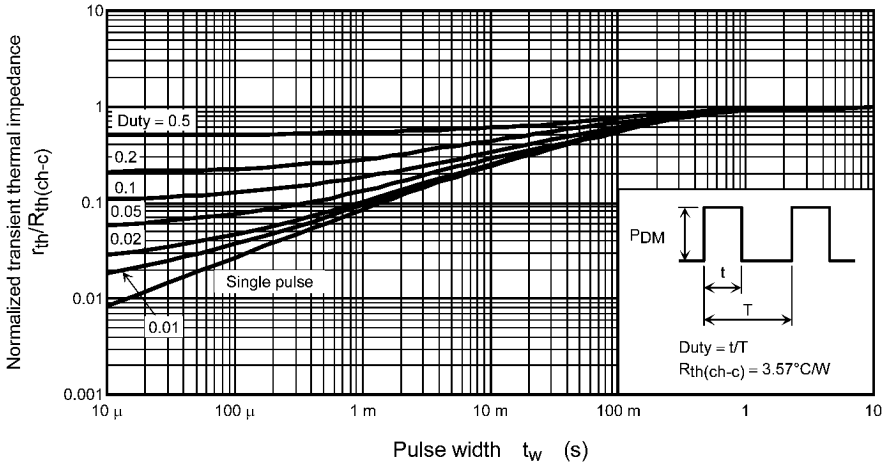


Fig. 8.12 $r_{th}/R_{th(ch-c)}$ - t_w (Guaranteed Maximum)

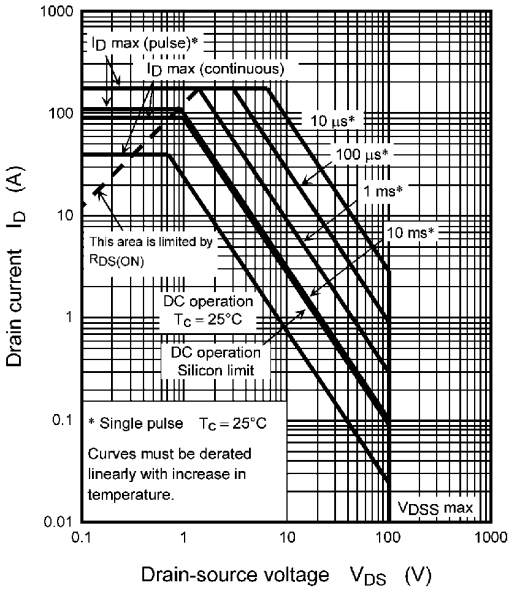


Fig. 8.13 Safe Operating Area (Guaranteed Maximum)

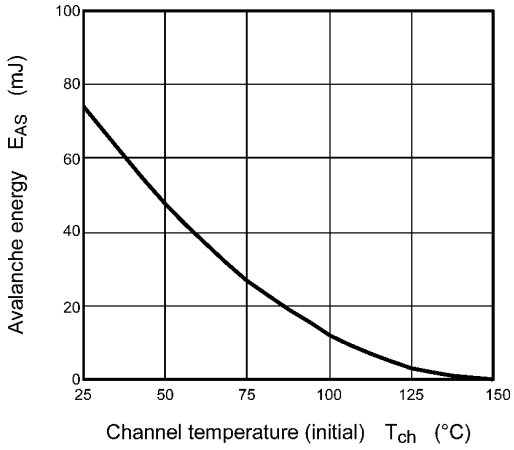
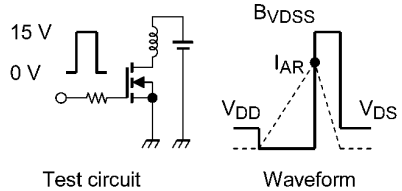


Fig. 8.14 E_{AS} - T_{ch} (Guaranteed Maximum)



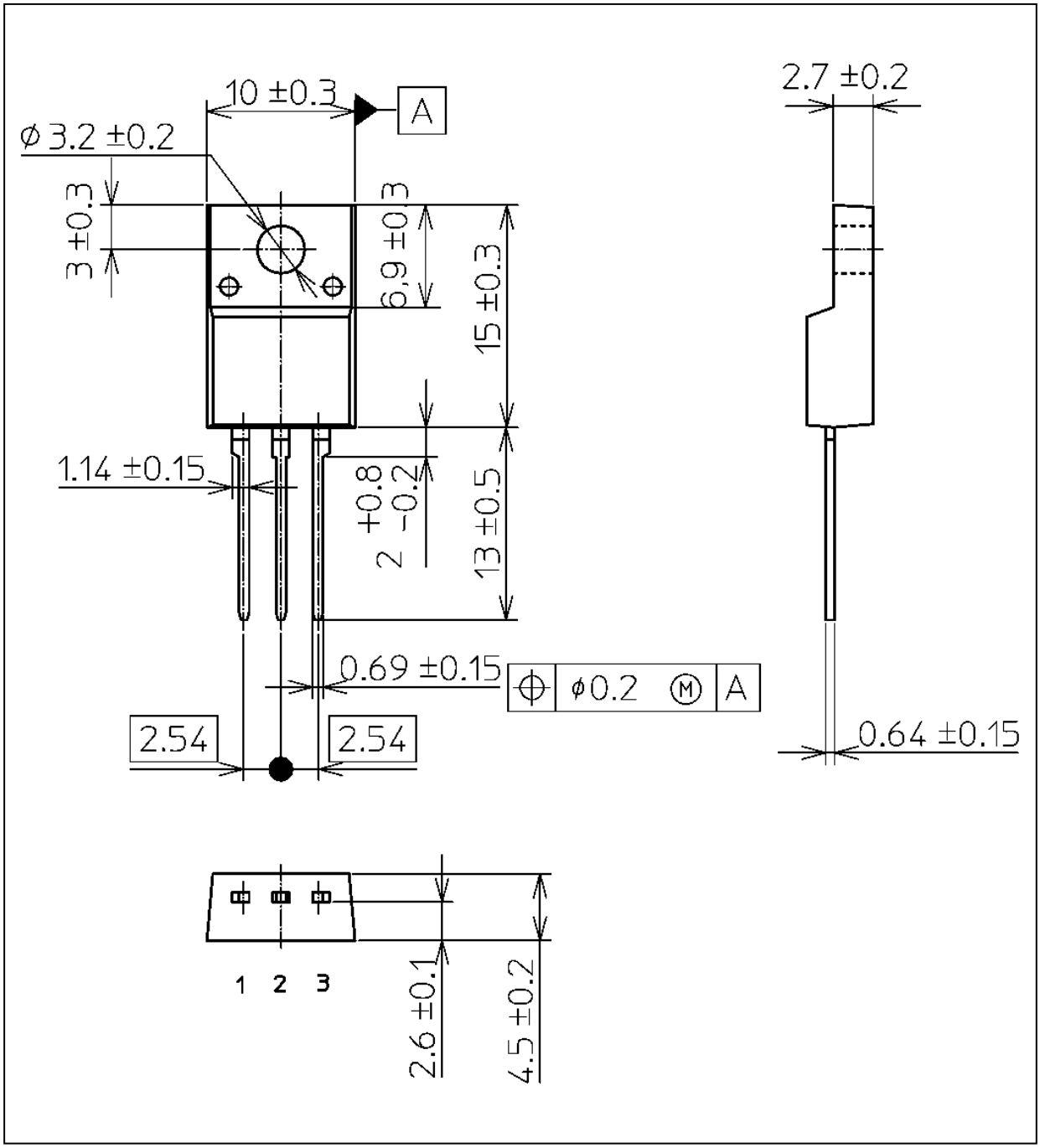
V_{DD} = 80 V, I_{AR} = 40 A $E_{AS} = \frac{1}{2} \cdot L \cdot I_{AR}^2 \cdot \left(\frac{B_{VDSS}}{B_{VDSS} - V_{DD}} \right)$

Fig. 8.15 Test Circuit/Waveform

Note: The above characteristics curves are presented for reference only and not guaranteed by production test, unless otherwise noted.

Package Dimensions

Unit: mm



Weight: 1.7 g (typ.)

Package Name(s)
JEITA: SC-67
TOSHIBA: 2-10U1S
Nickname: TO-220SIS

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