MOSFETs Silicon N-channel MOS (U-MOSⅧ-H)

SSM3K36TU

1. Applications

- High-Speed Switching

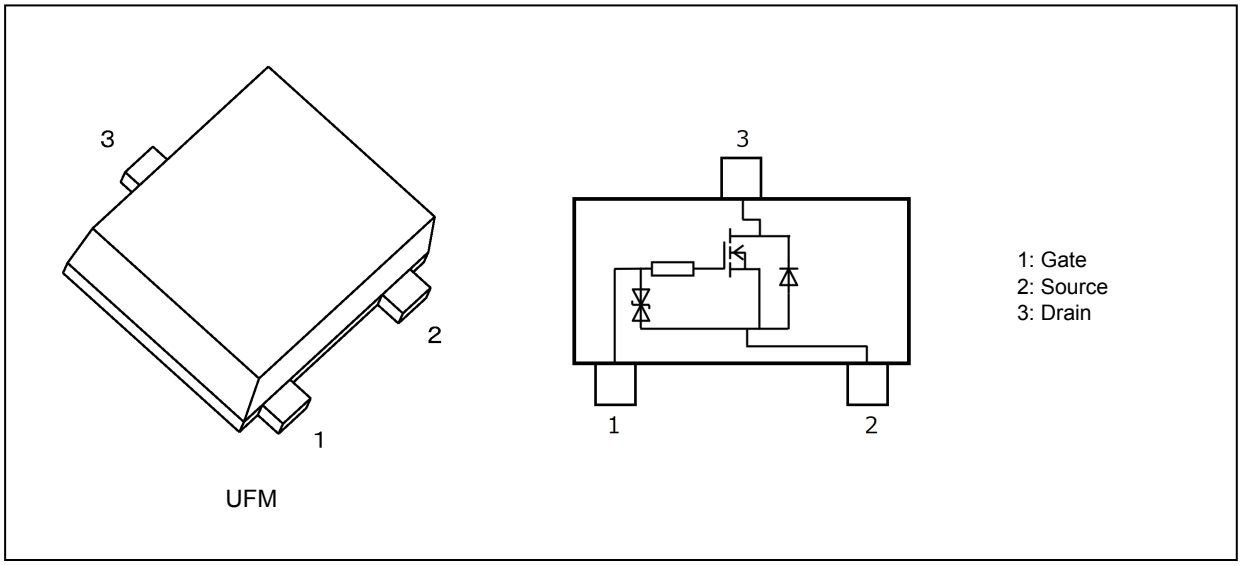
2. Features

(1) 1.5-V drive

(2) Low drain-source on-resistance

: $R_{DS(ON)}$ = 1.52 Ω (max) (@V_{GS} = 1.5 V)
$R_{DS(ON)}$ = 1.14 Ω (max) (@V_{GS} = 1.8 V)
$R_{DS(ON)}$ = 0.85 Ω (max) (@V_{GS} = 2.5 V)
$R_{DS(ON)}$ = 0.66 Ω (max) (@V_{GS} = 4.5 V)
$R_{DS(ON)}$ = 0.63 Ω (max) (@V_{GS} = 5.0 V)

3. Packaging and Internal Circuit



UFM

Start of commercial production
2008-02

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4. Absolute Maximum Ratings (Note) (Unless otherwise specified, T_a = 25 °C)

Characteristics		Symbol	Rating	Unit
Drain-source voltage		V_{DSS}	20	V
Gate-source voltage		V_{GSS}	±10	V
Drain current (DC)		I_D	500	mA
Drain current (pulsed)		I_{DP}	1000	
Power dissipation	(Note 1)	P_D	500	mW
			800	
Channel temperature		T_{ch}	150	°C
Storage temperature		T_{stg}	-55 to 150	°C

Note: Using continuously under heavy loads (e.g. the application of high temperature/current/voltage and the significant change in temperature, etc.) may cause this product to decrease in the reliability significantly even if the operating conditions (i.e. operating temperature/current/voltage, etc.) are within the absolute maximum ratings.
Please design the appropriate reliability upon reviewing the Toshiba Semiconductor Reliability Handbook ("Handling Precautions"/"Derating Concept and Methods") and individual reliability data (i.e. reliability test report and estimated failure rate, etc).

Note 1: Device mounted on a 25.4 mm × 25.4 mm × 1.6 mm FR4 glass epoxy board (Cu pad: 645 mm^2)

Note 2: Device mounted on a 25.4 mm × 25.4 mm × 0.8 mm ceramic board (Cu pad: 645 mm^2)

Note: This transistor is sensitive to electrostatic discharge and should be handled with care.

Note: The MOSFETs in this device are sensitive to electrostatic discharge. When handling this device, the worktables, operators, soldering irons and other objects should be protected against anti-static discharge.

Note: The channel-to-ambient thermal resistance, $R_{th(ch-a)}$, and the drain power dissipation, P_D, vary according to the board material, board area, board thickness and pad area. When using this device, be sure to take heat dissipation fully into account.

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5. Electrical Characteristics

5.1. Static Characteristics (Unless otherwise specified, T_a = 25 °C)

Characteristics		Symbol	Test Condition	Min	Typ.	Max	Unit
Gate leakage current		I_{GSS}	V_{DS} = 0 V, V_{GS} = ±10 V	—	—	±1	μA
Drain cut-off current		I_{DSS}	V_{DS} = 20 V, V_{GS} = 0 V	—	—	1	μA
Drain-source breakdown voltage		$V_{(BR)DSS}$	I_D = 1 mA, V_{GS} = 0 V	20	—	—	V
Drain-source breakdown voltage	(Note 1)	$V_{(BR)DSX}$	I_D = 1 mA, V_{GS} = -10 V	12	—	—	
Gate threshold voltage	(Note 2)	V_{th}	V_{DS} = 3 V, I_D = 1 mA	0.35	—	1.0	V
Forward transfer admittance	(Note 3)	$\|Y_{fs}\|$	V_{DS} = 3 V, I_D = 200 mA	420	840	—	mS
Drain-source on-resistance	(Note 3)	$R_{DS(ON)}$	I_D = 200 mA, V_{GS} = 5.0 V	—	0.46	0.63	Ω
			I_D = 200 mA, V_{GS} = 4.5 V	—	0.51	0.66	
			I_D = 200 mA, V_{GS} = 2.5 V	—	0.66	0.85	
			I_D = 100 mA, V_{GS} = 1.8 V	—	0.81	1.14	
			I_D = 50 mA, V_{GS} = 1.5 V	—	0.95	1.52	

Note 1: If a reverse bias is applied between gate and source, this device enters $V_{(BR)DSX}$ mode. Note that the drain-source breakdown voltage is lowered in this mode.

Note 2: Let V_{th} be the voltage applied between gate and source that causes the drain current (I_D) to below (1 mA for this device). Then, for normal switching operation, $V_{GS(ON)}$ must be higher than V_{th}, and $V_{GS(OFF)}$ must be lower than V_{th}. This relationship can be expressed as: $V_{GS(OFF)} < V_{th} < V_{GS(ON)}$.
Take this into consideration when using the device.

Note 3: Pulse measurement.

5.2. Dynamic Characteristics (Unless otherwise specified, T_a = 25 °C)

Characteristics	Symbol	Test Condition	Min	Typ.	Max	Unit
Input capacitance	C_{iss}	V_{DS} = 10 V, V_{GS} = 0 V, f = 1 MHz	—	46	—	pF
Reverse transfer capacitance	C_{rss}		—	7.3	—	
Output capacitance	C_{oss}		—	10.8	—	
Switching time (turn-on time)	t_{on}	V_{DD} = 10 V, I_D = 200 mA, V_{GS} = 0 to 2.5 V, R_{GS} = 50 Ω Duty ≤ 1 %, Input: t_r, t_f < 5 ns, Common source, See Chapter 5.3.	—	30	—	ns
Switching time (turn-off time)	t_{off}		—	75	—	

5.3. Switching Time Test Circuit

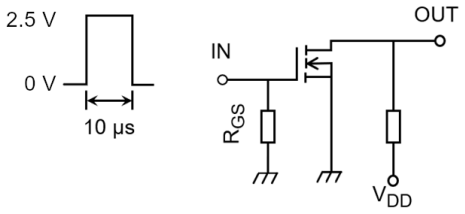


Fig. 5.3.1 Switching Time Test Circuit

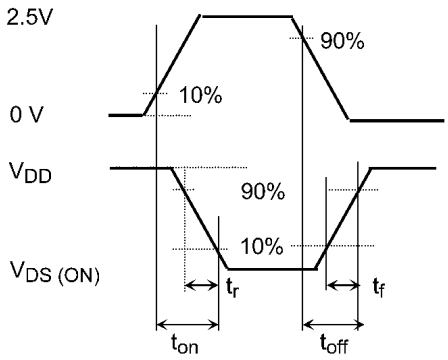


Fig. 5.3.2 Input Waveform/Output Waveform

5.4. Gate Charge Characteristics (Unless otherwise specified, T_a = 25 °C)

Characteristics	Symbol	Test Condition	Min	Typ.	Max	Unit
Total gate charge (gate-source plus gate-drain)	Q_g	V_{DD} = 10 V, I_D = 0.5 A, V_{GS} = 4.0 V	—	1.23	—	nC
Gate-source charge	Q_{gs}		—	0.60	—	
Gate-drain charge	Q_{gd}		—	0.63	—	

5.5. Source-Drain Characteristics (Unless otherwise specified, T_a = 25 °C)

Characteristics	Symbol	Test Condition	Min	Typ.	Max	Unit
Diode forward voltage (Note 1)	V_{DSF}	I_{DR} = 0.5 A, V_{GS} = 0 V	—	0.88	1.2	V

Note 1: Pulse measurement.

6. Marking

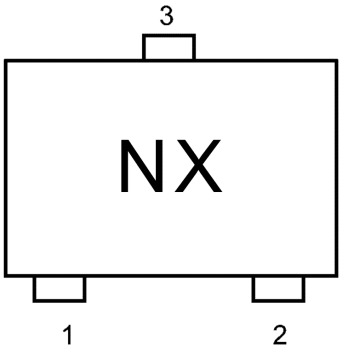


Fig. 6.1 Marking

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7. Characteristics Curves (Note)

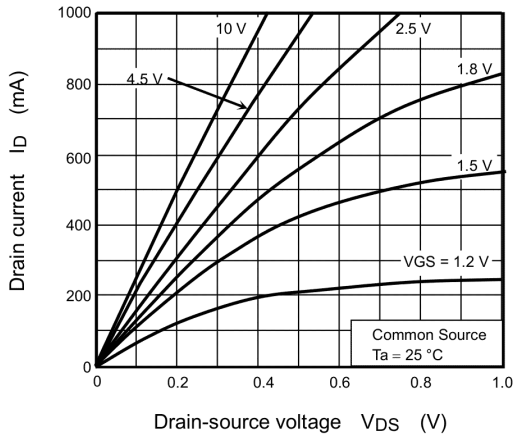


Fig. 7.1 I_D - V_{DS}

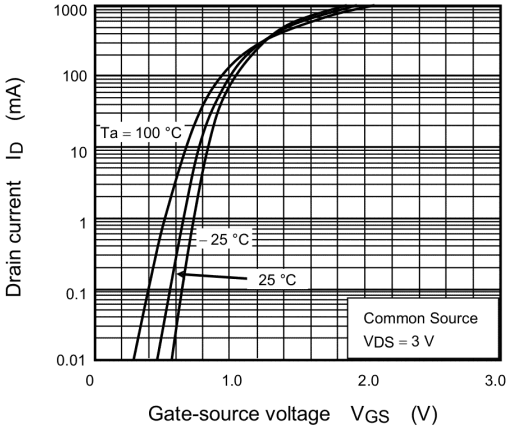


Fig. 7.2 I_D - V_{GS}

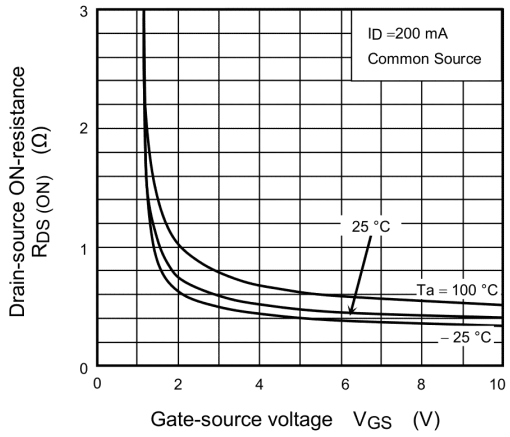


Fig. 7.3 $R_{DS(ON)}$ - V_{GS}

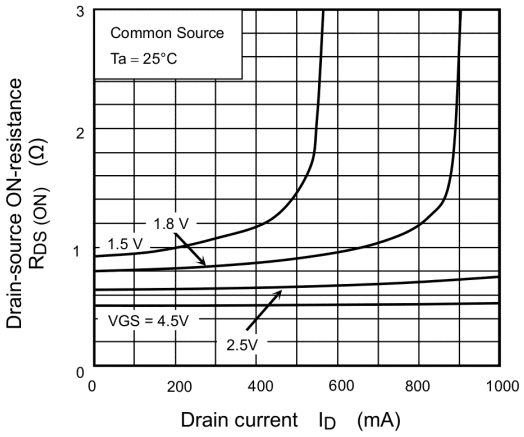


Fig. 7.4 $R_{DS(ON)}$ - I_D

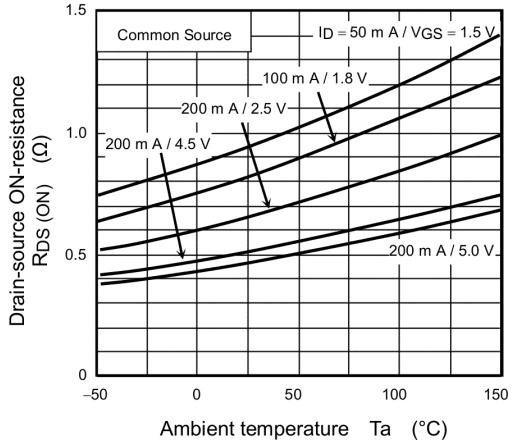


Fig. 7.5 $R_{DS(ON)}$ - T_a

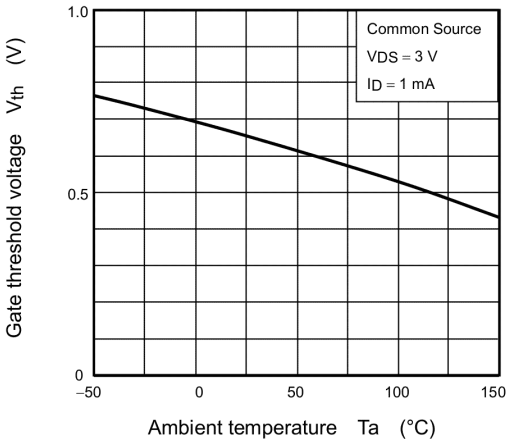


Fig. 7.6 V_{th} - T_a

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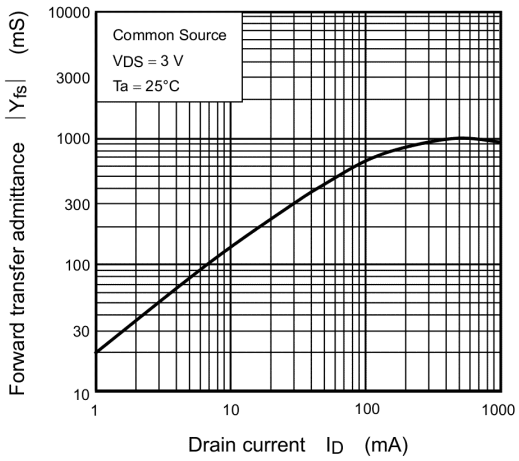


Fig. 7.7 $|Y_{fs}|$ - I_D

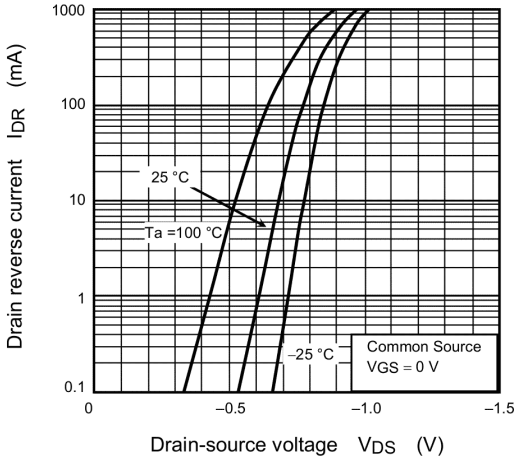


Fig. 7.8 I_{DR} - V_{DS}

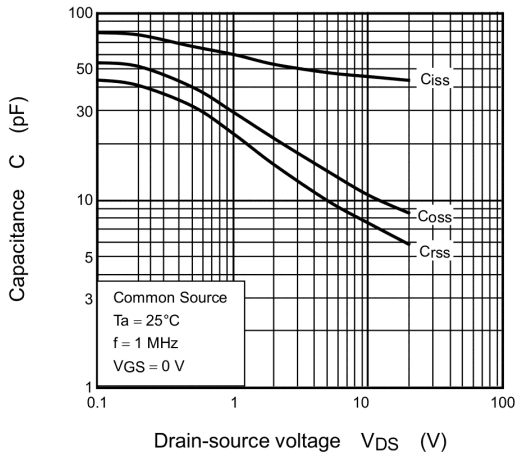


Fig. 7.9 C - V_{DS}

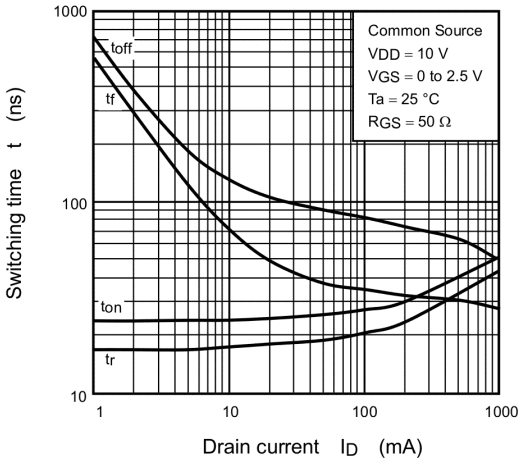


Fig. 7.10 t - I_D

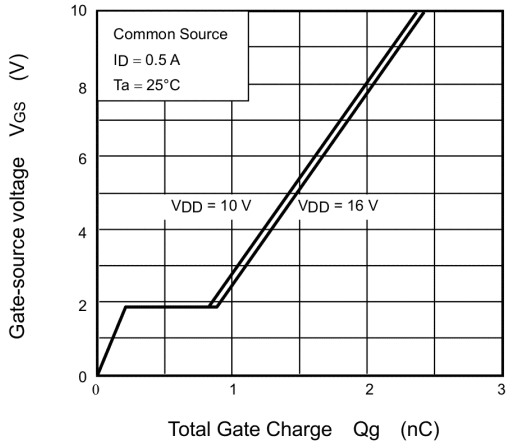


Fig. 7.11 Dynamic Input Characteristics

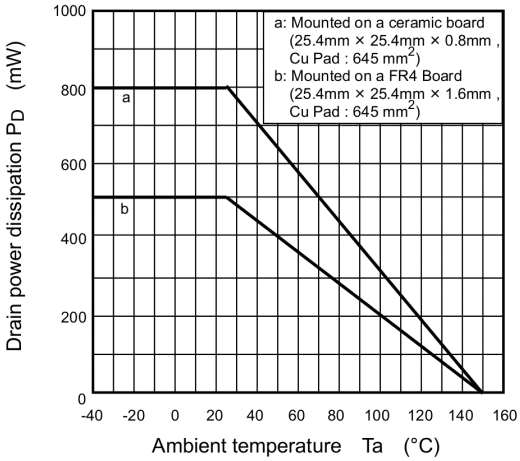


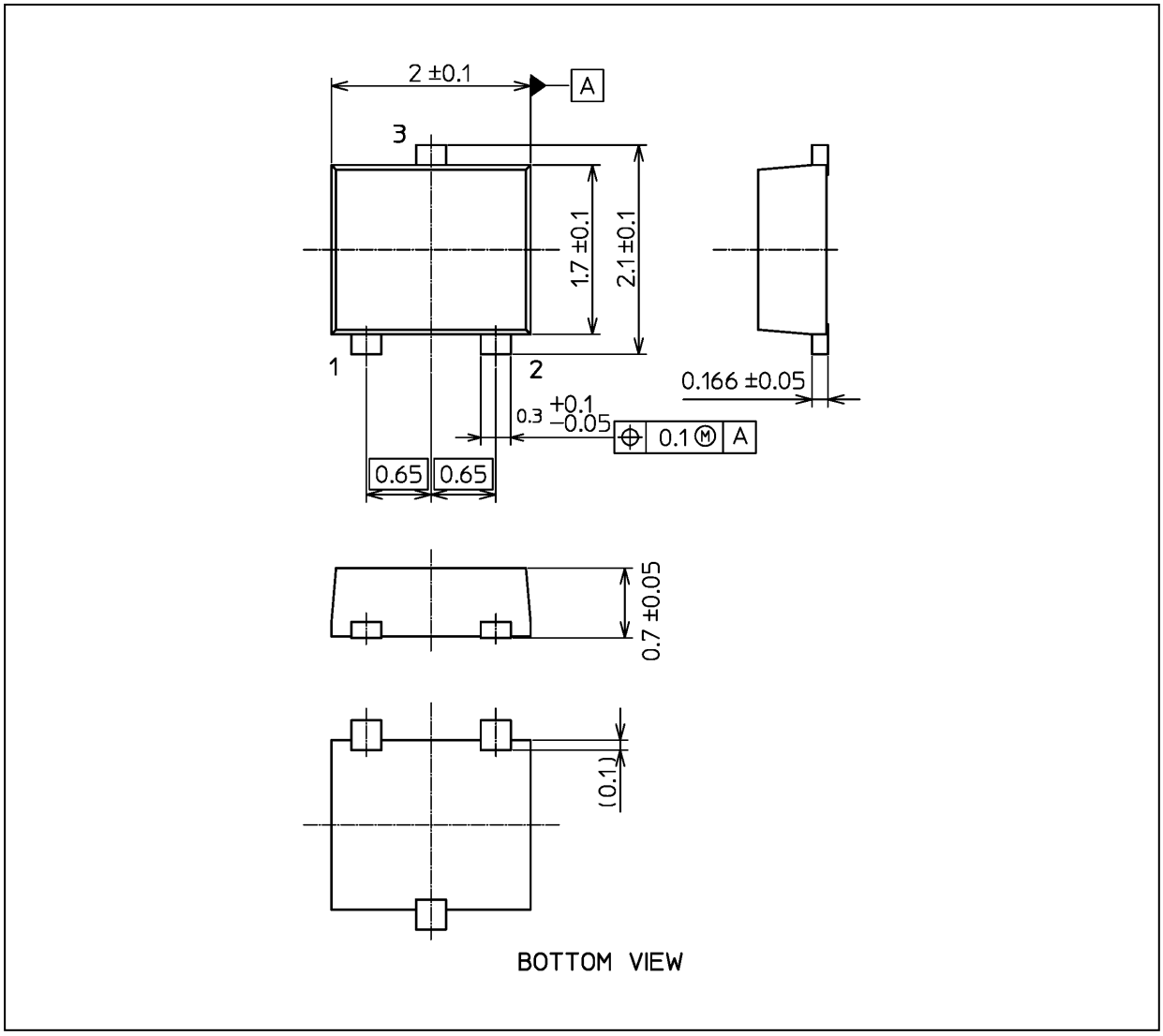
Fig. 7.12 P_D - T_a

Note: The above characteristics curves are presented for reference only and not guaranteed by production test, unless otherwise noted.

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Package Dimensions

Unit: mm



Weight: 6.6 mg (typ.)

Package Name(s)
Nickname: UFM

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