TOSHIBA Field Effect Transistor Silicon N Channel MOS Type

SSM5N15FU

1. Applications

- High Speed Switching Applications
- Analog Switch Applications

2. Features

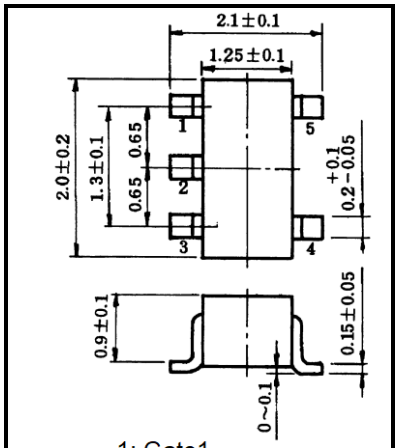
- Small package
- Low ON resistance: R_{DS} (ON) = 4.0 Ω (max) (@VGS = 4 V)
- : R_{DS} (ON) = 7.0 Ω (max) (@VGS = 2.5 V)

3. Absolute Maximum Ratings (Ta = 25°C)

(Q1, Q2 Common) (Note)

Characteristics		Symbol	Rating	Unit
Drain-Source voltage		V_{DS}	30	V
Gate-Source voltage		V_{GSS}	±20	V
Drain current	DC	I_D	100	mA
	Pulse	I_{DP}	200	
Drain power dissipation (Ta = 25°C)		P_D (Note1)	200	mW
Channel temperature		T_{ch}	150	°C
Storage temperature range		T_{stg}	-55 to 150	°C

Unit: mm



1: Gate1
2: Source
3: Gate2
4: Drain2
5: Drain1

USV

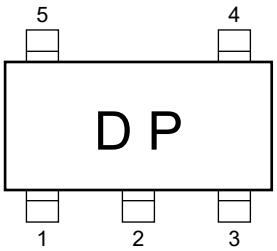
JEDEC	—
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TOSHIBA	2-2L1B

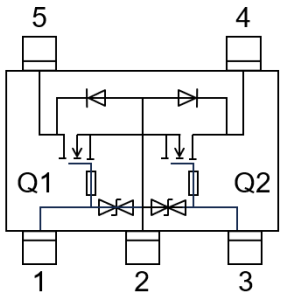
Weight: 6 mg (typ.)

Note: Using continuously under heavy loads (e.g. the application of high temperature/current/voltage and the significant change in temperature, etc.) may cause this product to decrease in the reliability significantly even if the operating conditions (i.e. operating temperature/current/voltage, etc.) are within the absolute maximum ratings. Please design the appropriate reliability upon reviewing the Toshiba Semiconductor Reliability Handbook ("Handling Precautions"/"Derating Concept and Methods") and individual reliability data (i.e. reliability test report and estimated failure rate, etc).

Note1: Total rating

4. Marking, Equivalent Circuit (top view)





5. Handling Precaution

When handling individual devices (which are not yet mounting on a circuit board), be sure that the environment is protected against electrostatic electricity. Operators should wear anti-static clothing, and containers and other objects that come into direct contact with devices should be made of anti-static materials.

Start of commercial production
2001-02

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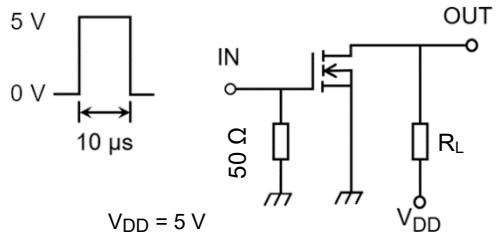
6. Electrical Characteristics

6.1. Electrical Characteristics (Ta = 25°C) (Q1, Q2 common)

Characteristic		Symbol	Test Condition	Min	Typ	Max	Unit
Gate leakage current		I_{GSS}	V_{GS} = ±16 V, V_{DS} = 0 V	-	-	±1	μA
Drain-Source breakdown voltage		$V_{(BR)\ DSS}$	I_D = 0.1 mA, V_{GS} = 0 V	30	-	-	V
Drain cut-off current		I_{DSS}	V_{DS} = 30 V, V_{GS} = 0 V	-	-	1	μA
Gate threshold voltage		V_{th}	V_{DS} = 3 V, I_D = 0.1 mA	0.8	-	1.5	V
Forward transfer admittance		$\|Y_{fs}\|$	V_{DS} = 3 V, I_D = 10 mA	25	-	-	mS
Drain-Source ON resistance		$R_{DS\ (ON)}$	I_D = 10 mA, V_{GS} = 4 V	-	2.2	4.0	Ω
			I_D = 10 mA, V_{GS} = 2.5 V	-	4.0	7.0	
Input capacitance		C_{iss}	V_{DS} = 3 V, V_{GS} = 0 V, f = 1 MHz	-	7.8	-	pF
Reverse transfer capacitance		C_{rss}		-	3.6	-	pF
Output capacitance		C_{oss}		-	8.8	-	pF
Switching time	Turn-on time	t_{on}	V_{DD} = 5 V, I_D = 10 mA, V_{GS} = 0 to 5 V See 6.2	-	50	-	ns
	Turn-off time	t_{off}		-	180	-	

6.2. Switching Time Test Circuit (Q1, Q2 common)

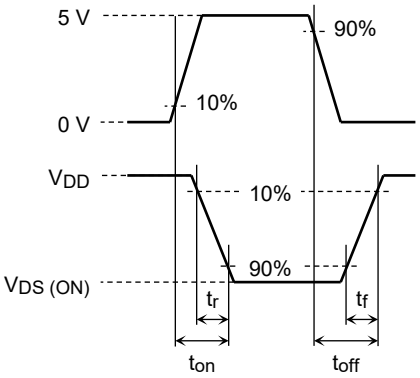
(a) Test circuit



V_{DD} = 5 V
Duty ≤ 1 %
V_{IN}: t_r, t_f < 5 ns
(Z_{out} = 50 Ω)
Common Source
Ta = 25°C

(b) V_{IN}

(c) V_{OUT}



6.3. Precaution

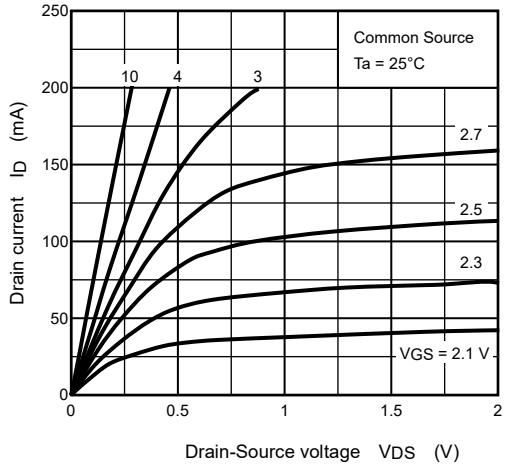
V_{th} can be expressed as voltage between gate and source when low operating current value is I_D = 100 μA for this product. For normal switching operation, $V_{GS\ (on)}$ requires higher voltage than V_{th} and $V_{GS\ (off)}$ requires lower voltage than V_{th}. (Relationship can be established as follows: $V_{GS\ (off)} < V_{th} < V_{GS\ (on)}$)

Please take this into consideration for using the device.

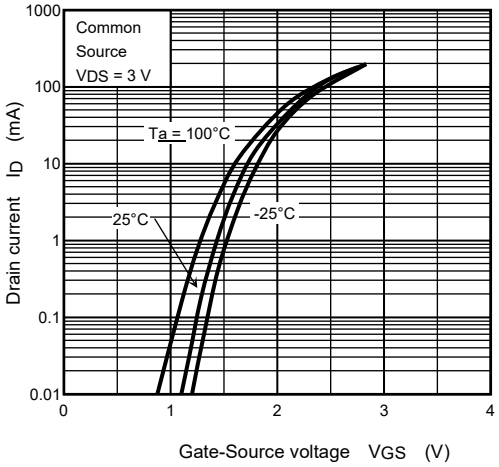
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7. Characteristic Chart(Q1, Q2 common) (Note)

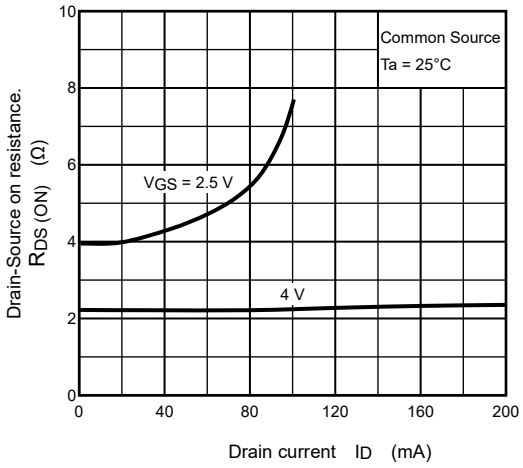
I_D – V_{DS}



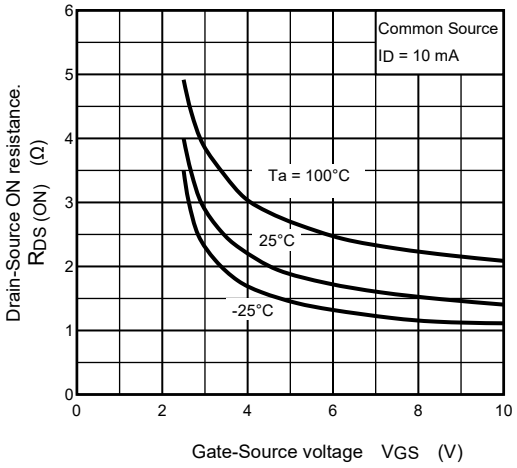
I_D – V_{GS}



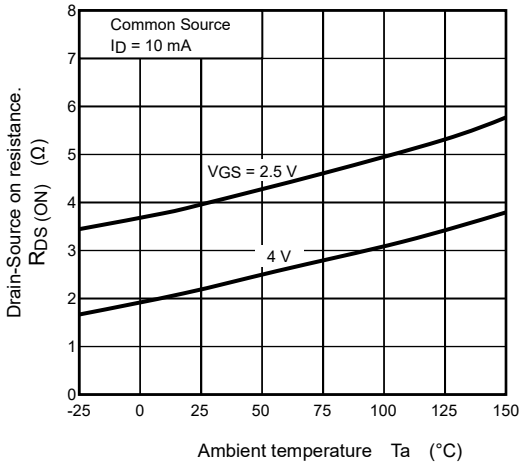
$R_{DS\ (ON)}$ – I_D



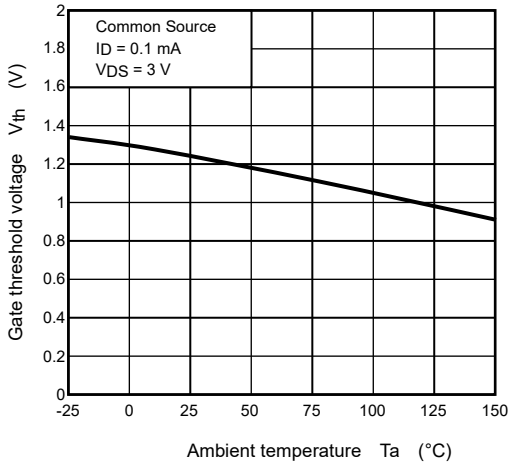
$R_{DS\ (ON)}$ – V_{GS}



$R_{DS\ (ON)}$ – Ta

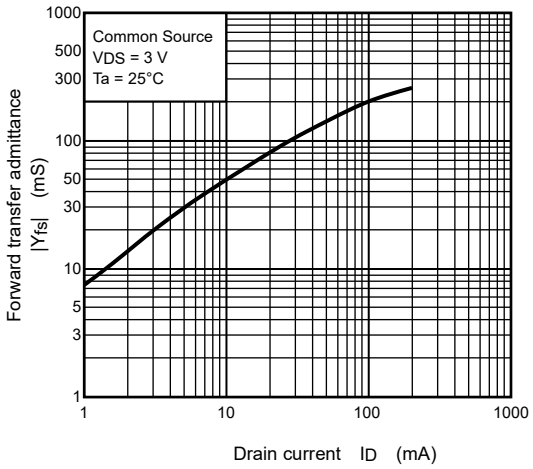


V_{th} – Ta

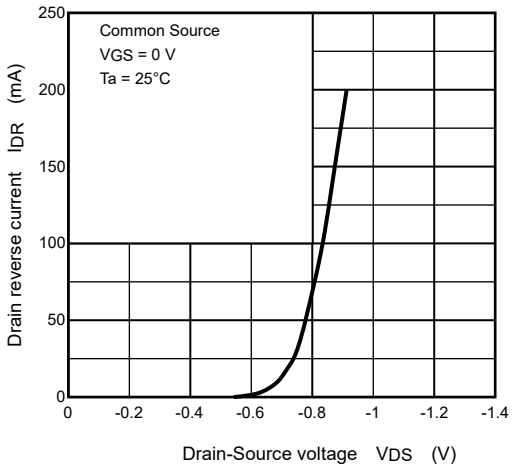


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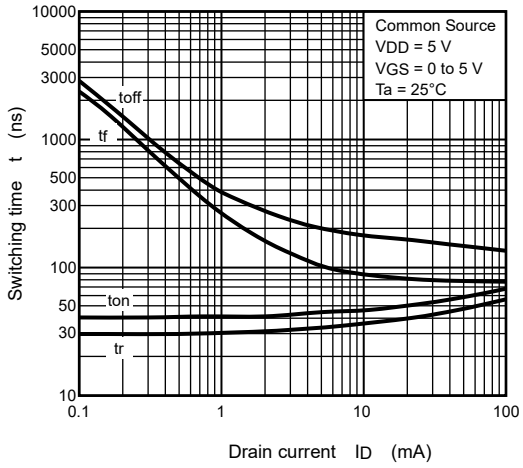
$|Y_{fs}| - I_D$



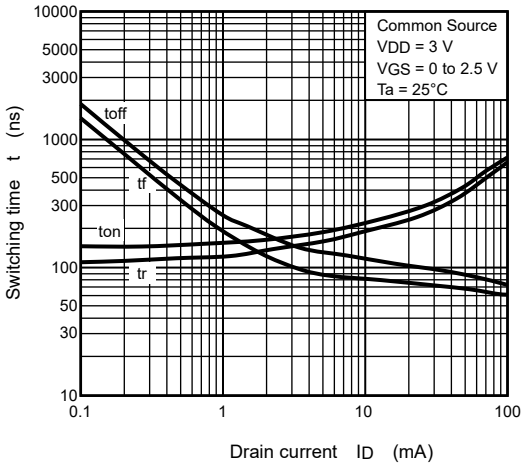
$I_{DR} - V_{DS}$



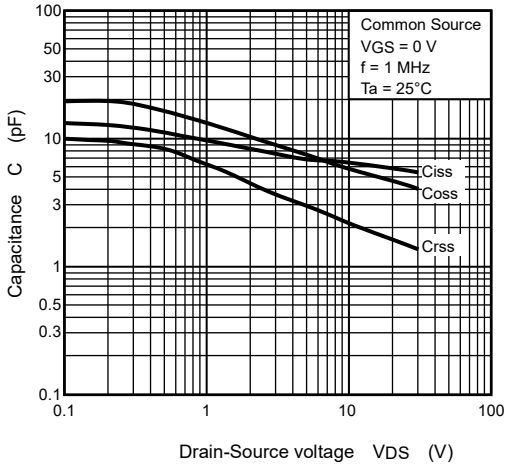
$t - I_D$



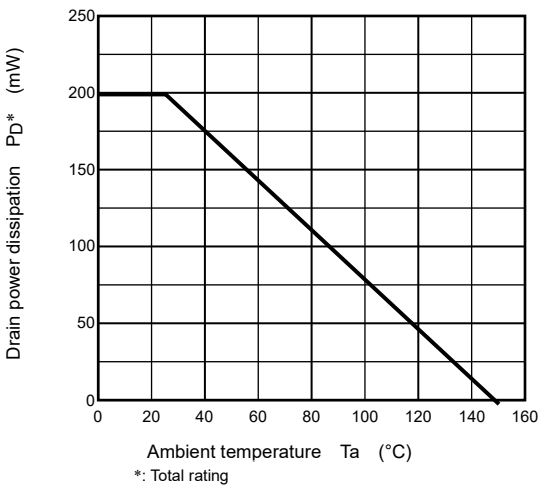
$t - I_D$



$C - V_{DS}$



$P_D^* - Ta$



*: Total rating

Note: The above characteristics curves are presented for reference only and not guaranteed by production test, unless otherwise noted.

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