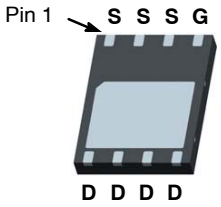
MOSFET – N-Channel, UltraFET Trench

80 V, 22 A, 16.5 mΩ

FDMS3572

V_{DS}	$R_{DS(on)}$ MAX	I_D MAX
80 V	16.5 mΩ @ 10 V	22 A
	24 mΩ @ 6 V	



Bottom View

WDFN8 5×6, 1.27P
(Power 56)
CASE 506DP

General Description

UltraFET devices combine characteristics that enable benchmark efficiency in power conversion applications. Optimized for $R_{DS(on)}$, low ESR, low total and Miller gate charge, these devices are ideal for high frequency DC to DC converters.

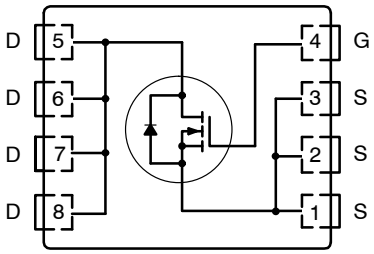
Features

- Max $R_{DS(on)}$ = 16.5 mΩ at V_{GS} = 10 V, I_D = 8.8 A
- Max $R_{DS(on)}$ = 24 mΩ at V_{GS} = 6 V, I_D = 8.4 A
- Typ Qg = 28 nC at V_{GS} = 10 V
- Low Miller Charge
- Optimized Efficiency at High Frequencies
- Pb−Free, Halide Free and RoHS Compliant

Applications

- DC – DC Conversion

ELECTRICAL CONNECTION



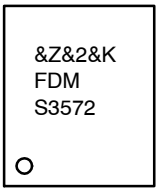
N-CHANNEL MOSFET

MAXIMUM RATINGS (T_A = 25°C unless otherwise noted)

Symbol	Parameter	Value	Unit
V_{DS}	Drain to Source Voltage	80	V
V_{GS}	Gate to Source Voltage	±20	V
I_D	Drain Current: – Continuous (Package limited) T_C = 25°C – Continuous (Silicon limited) T_C = 25°C – Continuous T_A = 25°C (Note 1a) – Pulsed	 22 48 8.8 50	A
P_D	Power Dissipation: T_C = 25°C T_A = 25°C (Note 1a)	 78 2.5	W
T_J, T_{STG}	Operating and Storage Junction Temperature Range	−55 to +150	°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

MARKING DIAGRAM



&Z	= Assembly Plant Code
&2	= 2−Digit Date Code (Year and Week)
&K	= 2−Digit Lot Run Code
FDMS3572	= Specific Device Code

THERMAL CHARACTERISTICS

Symbol	Parameter	Value	Unit
$R_{\theta JC}$	Thermal Resistance, Junction to Case	1.6	°C/W
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient (Note 1a)	50	

ORDERING INFORMATION

Device	Package	Shipping†
FDMS3572	WDFN8 5×6, 1.27P (Power 56) (Pb−Free, Halide Free)	3000 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specification Brochure, BRD8011/D.

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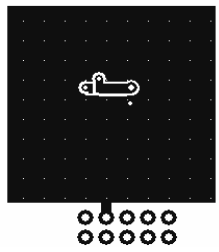
ELECTRICAL CHARACTERISTICS (T_J = 25°C unless otherwise noted)

Symbol	Parameter	Test Condition	Min	Typ	Max	Unit
OFF CHARACTERISTICS						
BV_{DSS}	Drain to Source Breakdown Voltage	I_D = 250 μA, V_{GS} = 0 V	80	–	–	V
$\frac{\Delta BV_{DSS}}{\Delta T_J}$	Breakdown Voltage Temperature Coefficient	I_D = 250 μA, Referenced to 25°C	–	76	–	mV/°C
I_{DSS}	Zero Gate Voltage Drain Current	V_{DS} = 64 V, V_{GS} = 0 V	–	–	1	μA
I_{GSS}	Gate to Source Leakage Current	V_{GS} = ±20 V, V_{DS} = 0 V	–	–	±100	nA
ON CHARACTERISTICS (Note 2)						
$V_{GS(th)}$	Gate to Source Threshold Voltage	V_{GS} = V_{DS}, I_D = 250 μA	2	3.2	4	V
$\frac{\Delta V_{GS(th)}}{\Delta T_J}$	Gate to Source Threshold Voltage Temperature Coefficient	I_D = 250 μA, Referenced to 25°C	–	−11	–	mV/°C
$R_{DS(on)}$	Drain to Source On Resistance	V_{GS} = 10 V, I_D = 8.8 A	–	13.5	16.5	mΩ
		V_{GS} = 6 V, I_D = 8.4 A	–	18.3	24	
		V_{GS} = 10 V, I_D = 8.8 A, T_J = 125°C	–	22.2	29	
g_{FS}	Forward Transconductance	V_{DS} = 10 V, I_D = 8.8 A	–	23	–	S
DYNAMIC CHARACTERISTICS						
C_{iss}	Input Capacitance	V_{DS} = 40 V, V_{GS} = 0 V, f = 1 MHz	–	1870	2490	pF
C_{oss}	Output Capacitance		–	275	365	pF
C_{rss}	Reverse Transfer Capacitance		–	78	120	pF
R_g	Gate Resistance	f = 1 MHz	–	1.3	–	Ω
SWITCHING CHARACTERISTICS						
$t_{d(on)}$	Turn-On Delay Time	V_{DD} = 40 V, I_D = 8.8 A, V_{GS} = 10 V, R_{GEN} = 6 Ω	–	11	20	ns
t_r	Rise Time		–	13	24	ns
$t_{d(off)}$	Turn-Off Delay Time		–	24	39	ns
t_f	Fall Time		–	12	22	ns
$Q_{g(TOT)}$	Total Gate Charge at 10 V	V_{GS} = 0 V to 10 V, V_{DD} = 40 V, I_D = 8.8 A	–	28	40	nC
Q_{gs}	Gate to Source Gate Charge	V_{DD} = 40 V, I_D = 8.8 A	–	9	–	nC
Q_{gd}	Gate to Drain “Miller” Charge	V_{DD} = 40 V, I_D = 8.8 A	–	8	–	nC
DRAIN-SOURCE DIODE CHARACTERISTICS						
V_{SD}	Source to Drain Diode Forward Voltage	V_{GS} = 0 V, I_S = 8.8 A (Note 2)	–	0.8	1.2	V
t_{rr}	Reverse Recovery Time	I_F = 8.8 A, di/dt = 100 A/μs	–	43	65	ns
Q_{rr}	Reverse Recovery Charge		–	71	107	nC

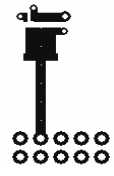
Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

NOTES:

1. $R_{\theta JA}$ is determined with the device mounted on a 1 in^2 pad 2 oz copper pad on a 1.5 x 1.5 in. board of FR−4 material. $R_{\theta JC}$ is guaranteed by design while $R_{\theta CA}$ is determined by the user’s board design.



a) 50°C/W when mounted on a 1 in^2 pad of 2 oz copper.



b) 125°C/W when mounted on a minimum pad of 2 oz copper.

2. Pulse Test: Pulse Width < 300 μs, Duty cycle < 2.0%.

TYPICAL CHARACTERISTICS

(T_J = 25°C unless otherwise noted)

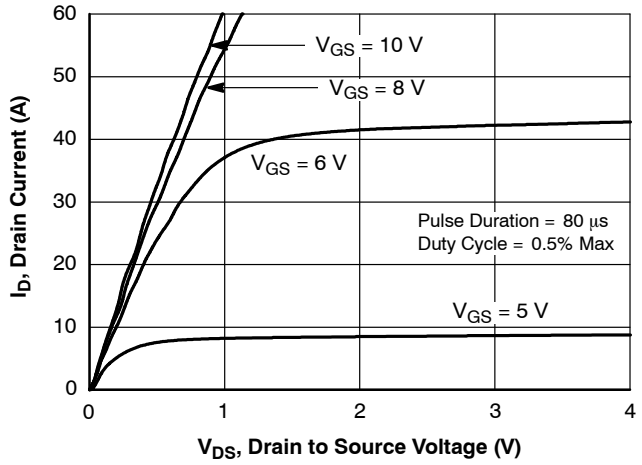


Figure 1. On Region Characteristics

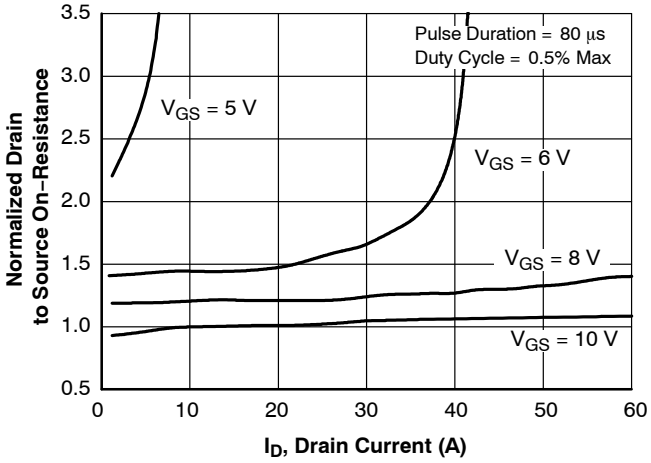


Figure 2. Normalized On−Resistance vs. Drain Current and Gate Voltage

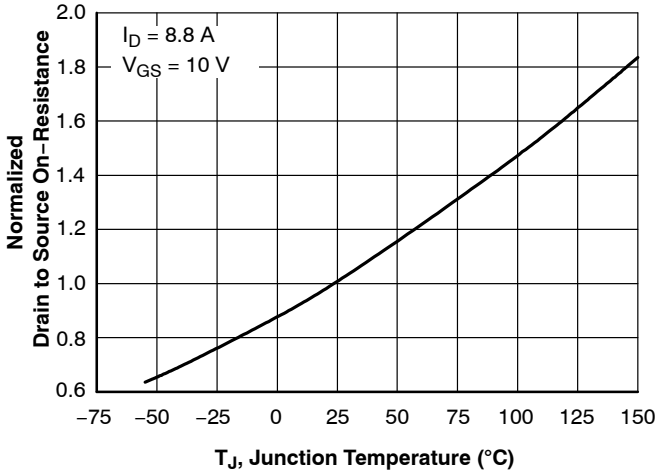


Figure 3. Normalized On Resistance vs. Junction Temperature

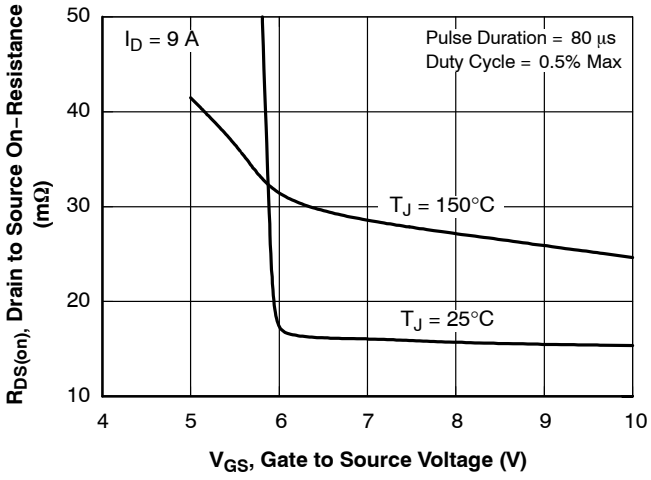


Figure 4. On−Resistance vs. Gate to Source Voltage

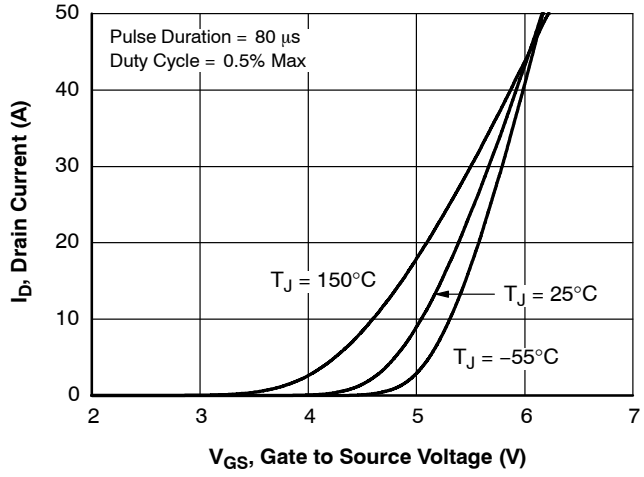


Figure 5. Transfer Characteristics

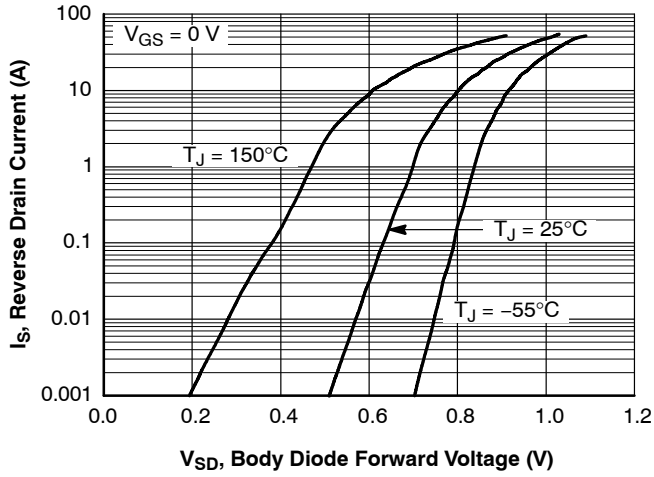


Figure 6. Source to Drain Diode Forward Voltage vs. Source Current

TYPICAL CHARACTERISTICS (continued)

(T_J = 25°C unless otherwise noted)

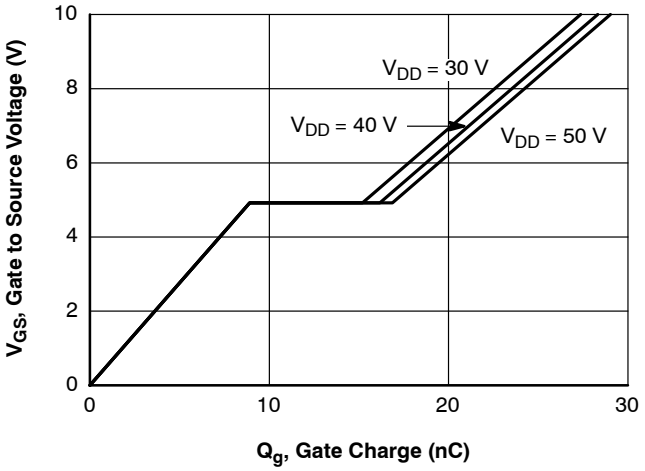


Figure 7. Gate Charge Characteristics

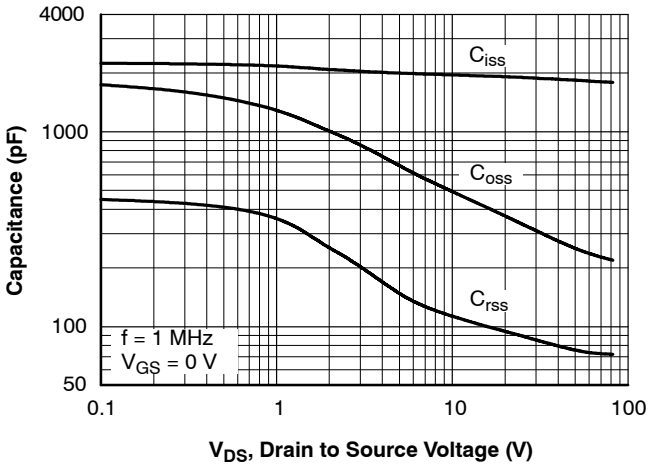


Figure 8. Capacitance vs. Drain to Source Voltage

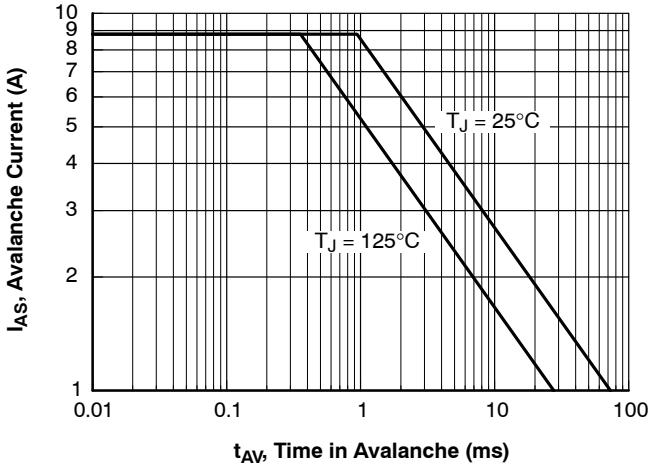


Figure 9. Unclamped Inductive Switching Capability

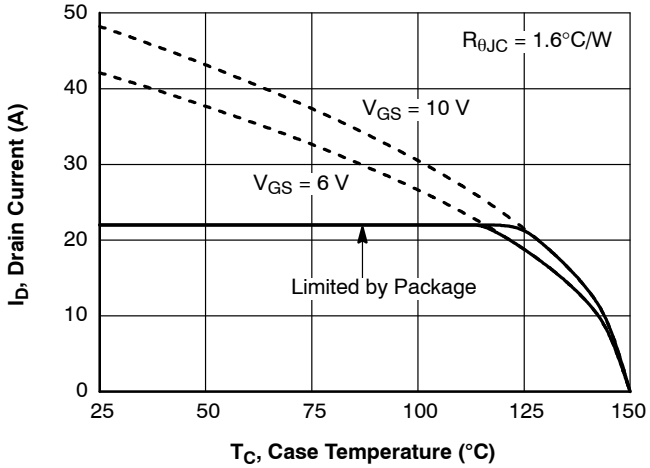


Figure 10. Maximum Continuous Drain Current vs. Case Temperature

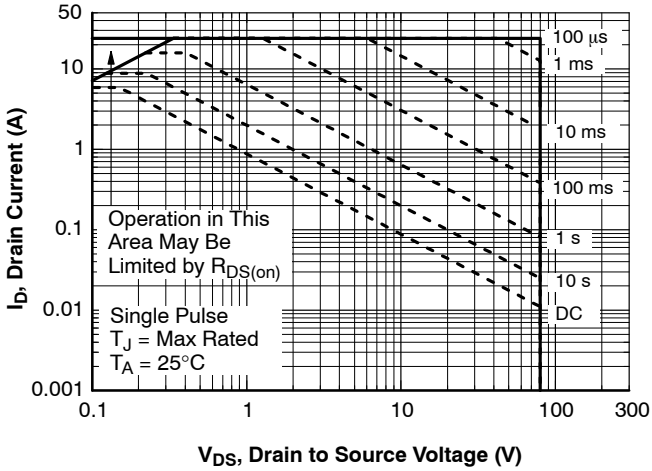


Figure 11. Forward Bias Safe Operating Area

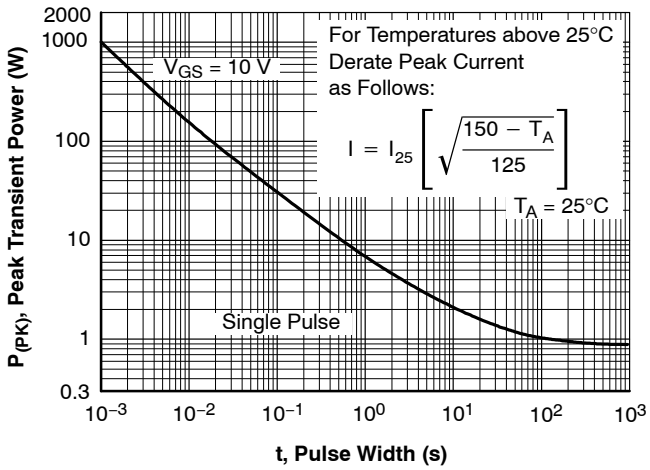


Figure 12. Single Pulse Maximum Power Dissipation

TYPICAL CHARACTERISTICS (continued)

(T_J = 25°C unless otherwise noted)

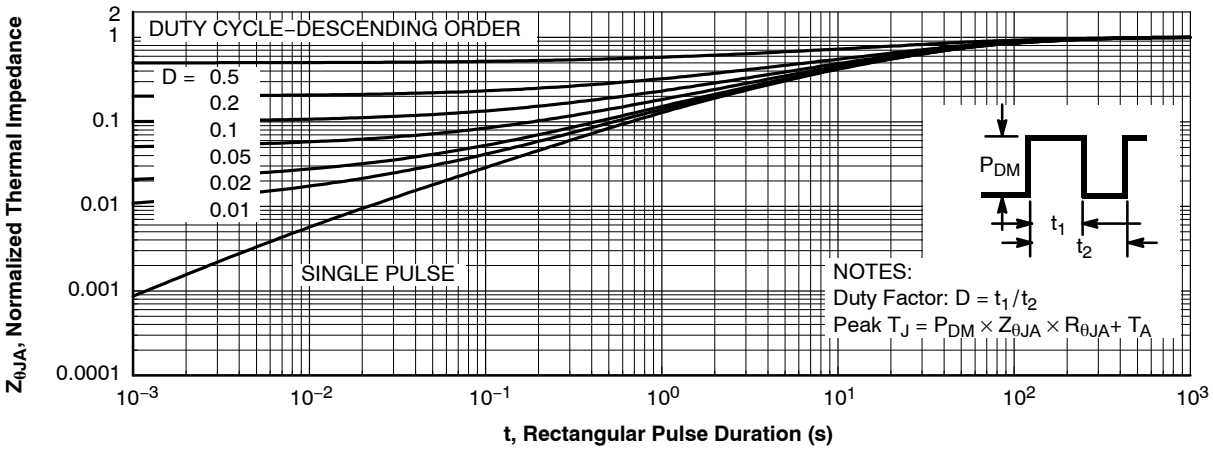
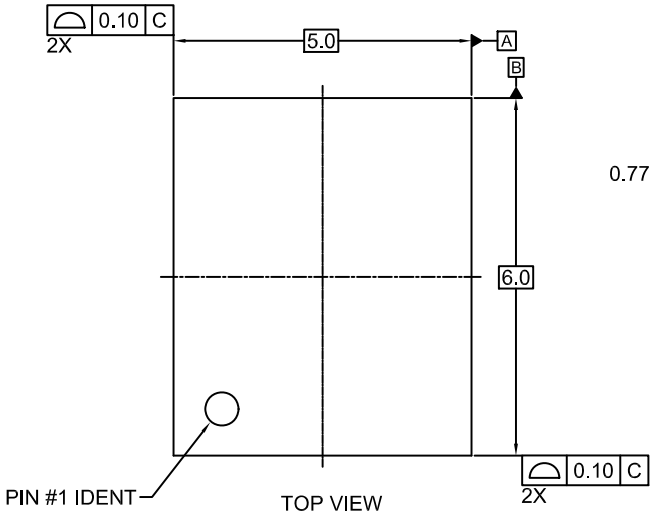
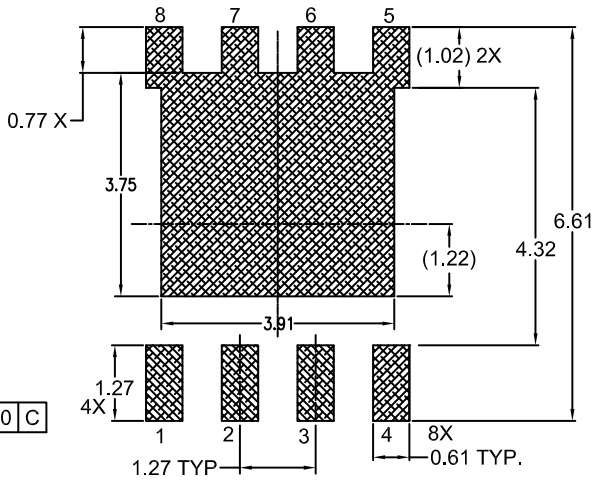


Figure 13. Transient Thermal Response Curve

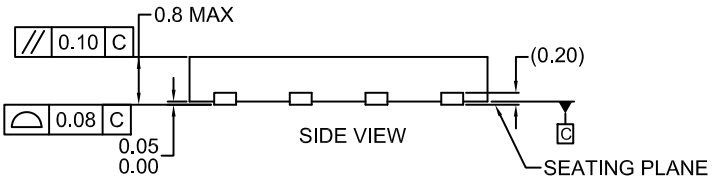
WDFN8 5x6, 1.27P
CASE 506DP
ISSUE O

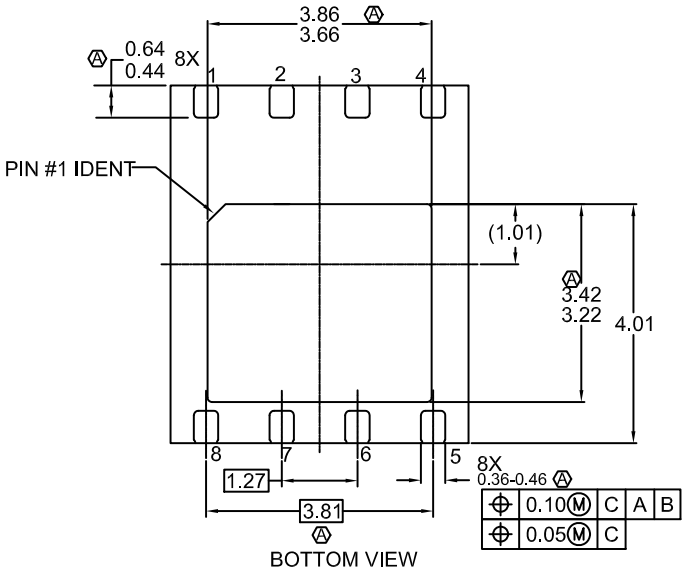
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RECOMMENDED LAND PATTERN





NOTES:

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