ON Semiconductor®

FDS8958A-F085

Dual N & P-Channel PowerTrench® MOSFET

General Description

These dual N- and P-Channel enhancement mode power field effect transistors are produced using ON Semiconductor's advanced PowerTrench process that has been especially tailored to minimize on-state ressitance and yet maintain superior switching performance.

These devices are well suited for low voltage and battery powered applications where low in-line power loss and fast switching are required.

Features

- **Q1**: N-Channel
  7.0A, 30V $R_{DS(on)}$ = 0.028Ω @ V_{GS} = 10V
  $R_{DS(on)}$ = 0.040Ω @ V_{GS} = 4.5V
- **Q2**: P-Channel
  5A, -30V $R_{DS(on)}$ = 0.05 Ω @ V_{GS} = -1 V
  $R_{DS(on)}$ = 0.080Ω @ V_{GS} = -5V
- Fast switching speed
- High power and handling capability in a widely used surface mount package
- Qualified to AEC Q1
- RoHS Compliant

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Absolute Maximum Ratings

T_A = 25°C unless otherwise noted

Symbol	Parameter		Q1	Q2	Units
V_{DSS}	Drain-Source Voltage		30	30	V
V_{GS}	Gate-Source Voltage		±20	±20	V
I_D	Drain Current - Continuous	(Note 1a)	7	-5	A
	- Pulsed		20	-20	
P_D	Power Dissipation for Dual Operation		2	2	W
	Power Dissipation for Single Operation	(Note 1a)	1.6	1.6	
		(Note 1c)	0.9	0.9	
E_{AS}	Single Pulse Avalanche Energy	(Note 3)	54	13	mJ
T_J, T_{STG}	Operating and Storage Junction Temperature Range		-55 to +150		°C

Thermal Characteristics

$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient	(Note 1a)	78	°C/W
$R_{\theta JC}$	Thermal Resistance, Junction-to-Case	(Note 1)	40	°C/W

Package Marking and Ordering Information

Device Marking	Device	Reel Size	Tape width	Quantity
FDS8958A	FDS8958A-F085	13"	12mm	2500 units

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Publication Order Number:
FDS8958A-F085/D

Electrical Characteristics

T_A = 25°C unless otherwise noted

Symbol	Parameter	Test Conditions	Type	Min	Typ	Max	Units
Off Characteristics							
BV_{DSS}	Drain-Source Breakdown Voltage	V_{GS} = 0 V, I_D = 250 µA V_{GS} = 0 V, I_D = -250 µA	Q1 Q2	30 -30			V
$\frac{\Delta BV_{DSS}}{\Delta T_J}$	Breakdown Voltage Temperature Coefficient	I_D = 250 µA, Referenced to 25°C I_D = -250 µA, Referenced to 25°C	Q1 Q2		25 -23		mV/°C
I_{DSS}	Zero Gate Voltage Drain Current	V_{DS} = 24 V, V_{GS} = 0 V V_{DS} = -24 V, V_{GS} = 0 V	Q1 Q2			1 -1	µA
I_{GSSF}	Gate-Body Leakage, Forward	V_{GS} = 20 V, V_{DS} = 0 V	All			100	nA
I_{GSSR}	Gate-Body Leakage, Reverse	V_{GS} = -20 V, V_{DS} = 0 V	All			-100	nA
On Characteristics (Note 2)							
$V_{GS(th)}$	Gate Threshold Voltage	V_{DS} = V_{GS}, I_D = 250 µA V_{DS} = V_{GS}, I_D = -250 µA	Q1 Q2	1 -1	1.9 -1.7	3 -3	V
$\frac{\Delta V_{GS(th)}}{\Delta T_J}$	Gate Threshold Voltage Temperature Coefficient	I_D = 250 µA, Referenced to 25°C I_D = -250 µA, Referenced to 25°C	Q1 Q2		-4.5 4		mV/°C
$R_{DS(on)}$	Static Drain-Source On-Resistance	V_{GS} = 10 V, I_D = 7 A V_{GS} = 10 V, I_D = 7 A, T_J = 125°C V_{GS} = 4.5 V, I_D = 6 A	Q1		19 27 [illegible]	28 42 40	mΩ
		V_{GS} = -10 V, I_D = -5 A V_{GS} = -10 V, I_D = -5 A, T[illegible]125°C V_{GS} = -4.5 V, I_D = [illegible] A	[illegible]		42 57 65	52 78 80	
$I_{D(on)}$	On-State Drain Current	V_{GS} = 10 V, V_{DS} = [illegible] V V_{GS} = -10 V, V_{DS} = [illegible] V	Q1 Q2	20 -20			A
g_{FS}	Forward Transconductance	V_{DS} = 5 V, I_D = 7 A V_{DS} = -[illegible] V, [illegible]=-5 A	Q1 Q2		[illegible] 10		S
Dynamic Characteristics							
C_{iss}	Input Capacitance	Q[illegible] V_{DS} [illegible]15 V, V_{GS} = 0 V, f = 1.0 MHz	Q1 Q2		575 528		pF
C_{oss}	Output Capacitance	[illegible]	Q1 Q2		145 132		pF
C_{rss}	Reverse Transfer Capacitance	V_{DS} = -15 V, V_{GS} = 0 V, f = 1.0 MHz	Q1 Q2		65 70		pF
R_G	Gate Resistance	V_{GS} = 15 mV, f = 1.0 MHz	Q1 Q2		2.1 6.0		Ω

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Electrical Characteristics (continued) T_A = 25°C unless otherwise noted

Symbol	Parameter	Test Conditions	Type	Min	Typ	Max	Units
Switching Characteristics (Note 2)							
$t_{d(on)}$	Turn-On Delay Time	Q1 V_{DD} = 15 V, I_D = 1 A, V_{GS} = 10V, R_{GEN} = 6 Ω	Q1 Q2		8 7	16 14	ns
t_r	Turn-On Rise Time		Q1 Q2		5 13	10 24	ns
$t_{d(off)}$	Turn-Off Delay Time	Q2 V_{DD} = -15 V, I_D = -1 A, V_{GS} = -10V, R_{GEN} = 6 Ω	Q1 Q2		23 14	37 25	ns
t_f	Turn-Off Fall Time		Q1 Q2		3 9	6 17	ns
Q_g	Total Gate Charge	Q1 V_{DS} = 15 V, I_D = 7 A, V_{GS} = 10 V	Q1 Q2		11.4 9.6	16	nC
Q_{gs}	Gate-Source Charge	Q2 V_{DS} = -15 V, I_D = -5 A, V_{GS} = -10 V	Q1 Q2		1.7 2		nC
Q_{gd}	Gate-Drain Charge		Q1 Q2		2.1		nC
Drain–Source Diode Characteristics and Maximum Ratings							
I_S	Maximum Continuous Drain-Source Diode Forward Current		Q1 Q2			1.3 -1.3	A
I_{SM}	Maximum Plused Drain-Source Diode Forward Current	(Note 2)	Q1 Q2			20 -20	A
V_{SD}	Drain-Source Diode Forward Voltage	V_{GS} = 0 V, I_S = 1.3 A (Note 2) V_{GS} = 0 V, I_S = -1.3 A (Note 2)	Q1 Q2		0.75 -0.88	1.2 -1.2	V
t_{rr}	Diode Reverse Recovery Time	Q1 I_F = 7 A, dI_F/dt = 100 A/µs	Q1 Q2		19 19		nS
Q_{rr}	Diode Reverse Recovery Charge	Q2 I_F = -5 A, dI_F/dt = 100 A/µs	Q1 Q2		9 6		nC

Notes:

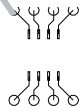
1. $R_{\theta JA}$ is the sum of the junction-to-case and case-to-ambient thermal resistance where the case thermal reference is defined as the solder mounting surface of the drain pins. $R_{\theta JC}$ is guaranteed by design while $R_{\theta CA}$ is determined by the user's board design.



a) 78°/W when mounted on a 0.5 in² pad of 2 oz copper



b) 125°/W when mounted on a 0.02 in² pad of 2 oz copper



c) 135°/W when mounted on a minimum pad.

Scale 1 : 1 on letter size paper

2. Pulse Test: Pulse Width < 300µs, Duty Cycle < 2.0%

3. Starting TJ = 25°C, L = 3mH, I_{AS} = 6A, V_{DD} = 30V, V_{GS} = 10V (Q1).

Starting TJ = 25°C, L = 3mH, I_{AS} = 5A, V_{DD} = 30V, V_{GS} = 10V (Q2).

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Typical Characteristics: Q1 (N-Channel)

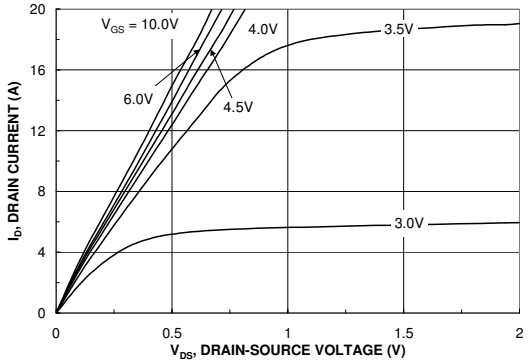


Figure 1. On-Region Characteristics.

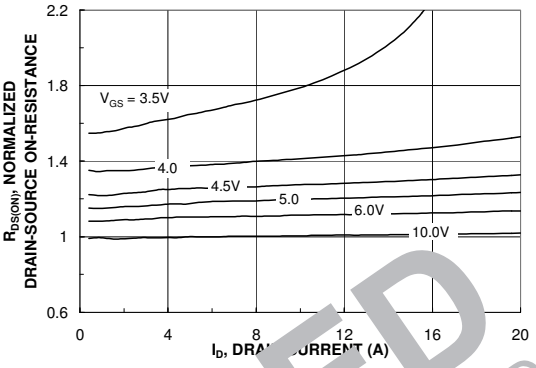


Figure 2. On-Resistance Variation with Drain Current and Gate Voltage.

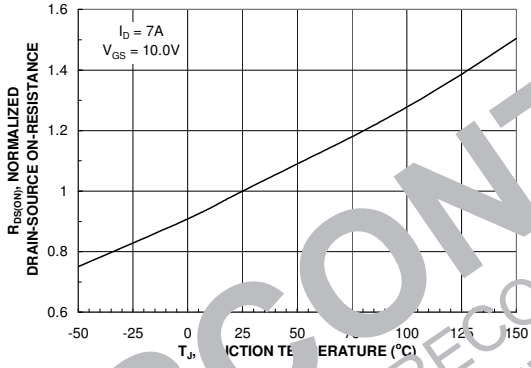


Figure 3. On-Resistance Variation with Temperature.

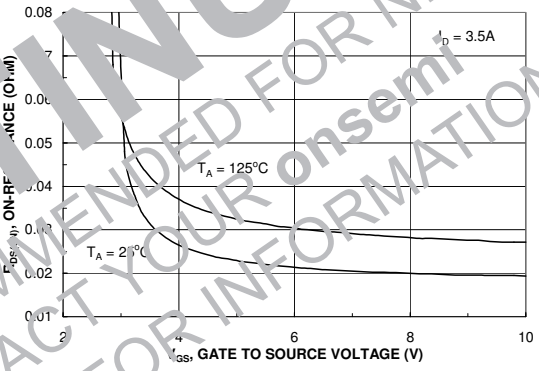


Figure 4. On-Resistance Variation with Gate-to-Source Voltage.

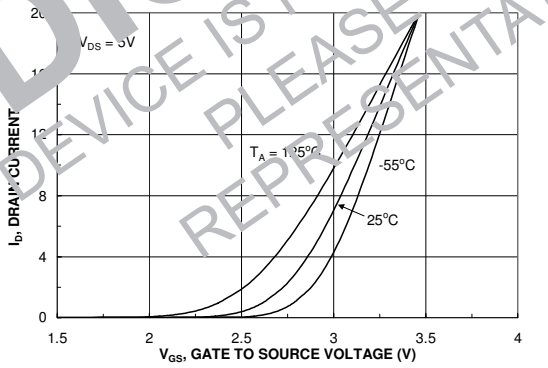


Figure 5. Transfer Characteristics.

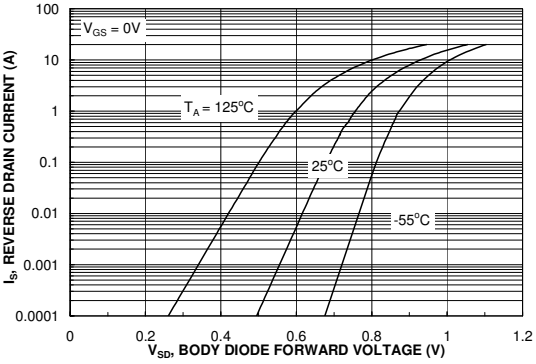


Figure 6. Body Diode Forward Voltage Variation with Source Current and Temperature.

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Typical Characteristics: Q1 (N-Channel)

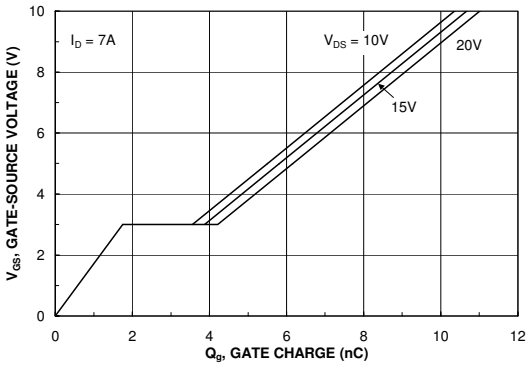


Figure 7. Gate Charge Characteristics.

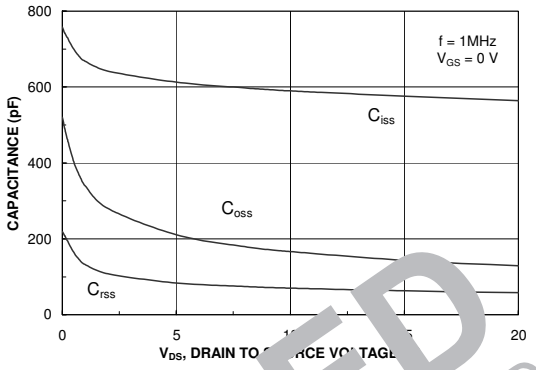


Figure 8. Capac nce haracteristics.

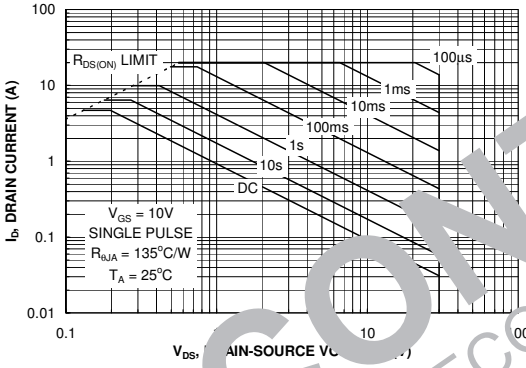


Figure . Maxim n Saf Operating Area.

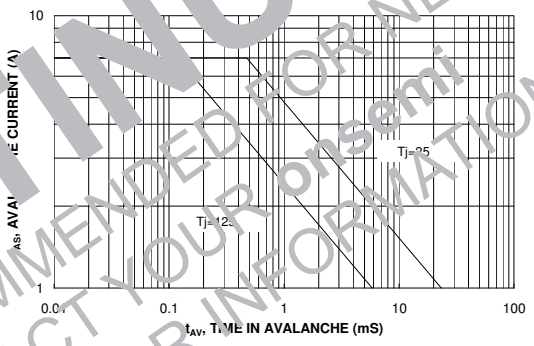


Figure 10. Unclamped Inductive Switching Capability Figure

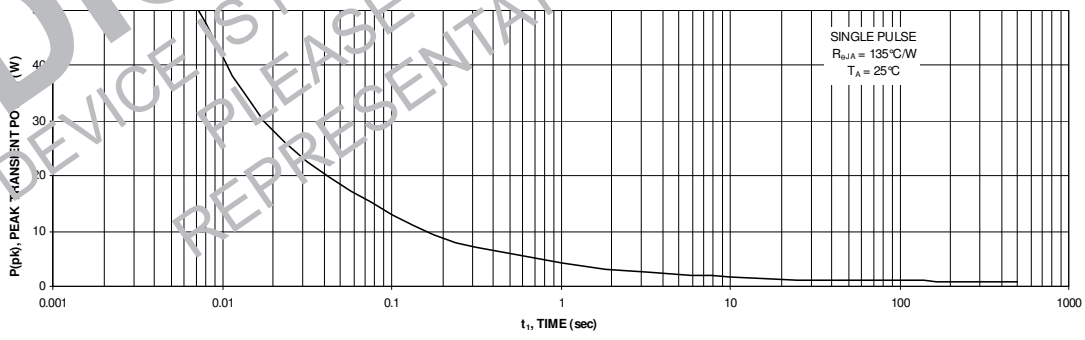


Figure 11. Single Pulse Maximum Power Dissipation.

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Typical Characteristics: Q2 (P-Channel)

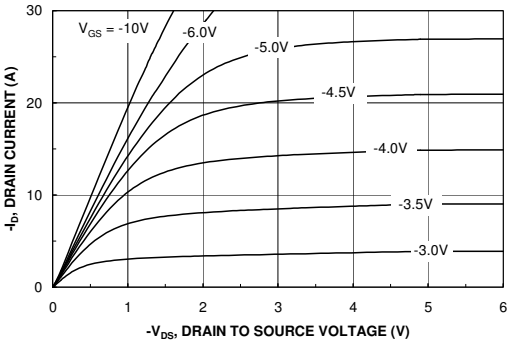


Figure 12. On-Region Characteristics.

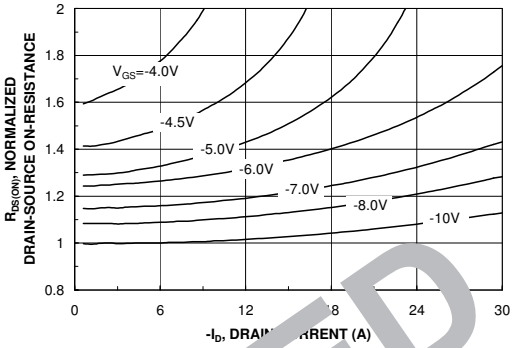


Figure 13. On-Resistance Variation with Drain Current and Gate Voltage.

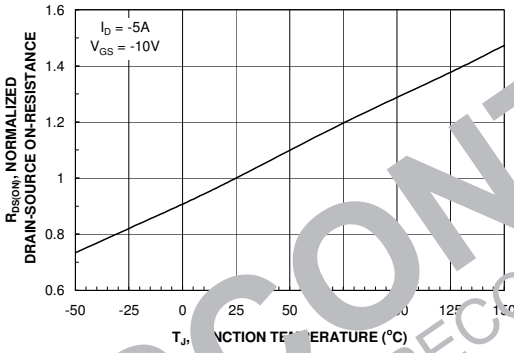


Figure 14. On-Resistance Variation with Temperature.

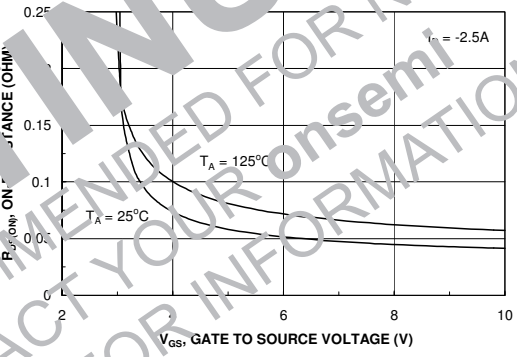


Figure 15. On-Resistance Variation with Gate-to-Source Voltage.

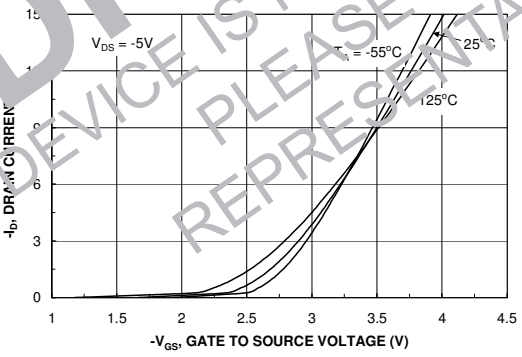


Figure 16. Transfer Characteristics.

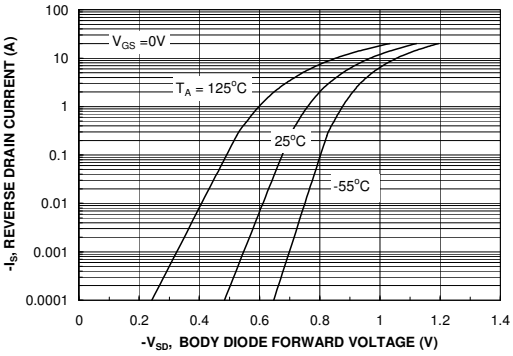


Figure 17. Body Diode Forward Voltage Variation with Source Current and Temperature.

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Typical Characteristics: Q2 (P-Channel)

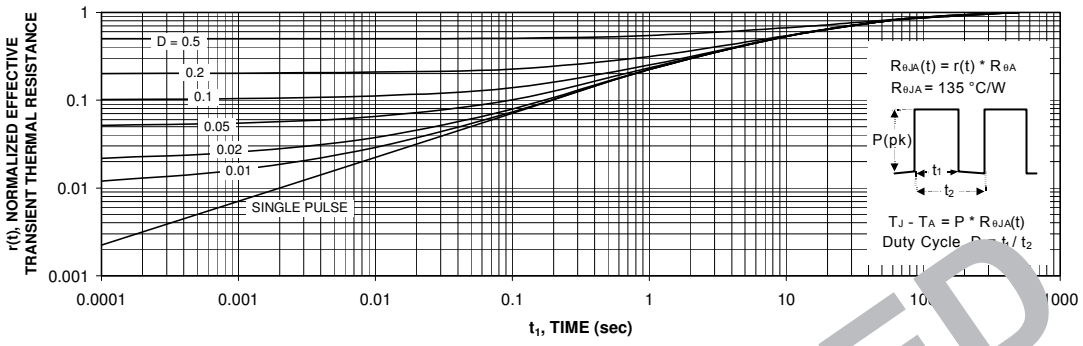


Figure 23. Transient Thermal Response Curve

Thermal characterization performed using the conditions described in Note c.
Transient thermal response will change depending on the circuit board design.

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