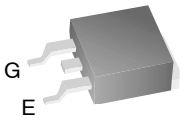
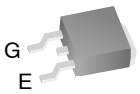
ECOSPARK®2 320 mJ, 450 V, N-Channel Ignition IGBT

FGD3245G2-F085, FGB3245G2-F085



JEDEC TO−263AB
D²PAK−3 (TO−263, 3−LEAD)
CASE 418AJ



JEDEC TO−263AA
DPAK3 (TO−252 3 LD)
CASE 369AS

General Description

The FGB3245G2−F085 and FGD3245G2 are N−channel IGBTs designed in **onsemi**'s ECOSPARK−2 technology which helps in eliminating external protection circuitry. The technology is optimized for driving the coil in the harsh environment of automotive ignition systems and offers out−standing Vsat and SCIS Energy capability also at elevated operating temperatures. The logic level gate input is ESD protected and features an integrated gate resistor. An integrated zener−circuitry clamps the IGBT's collecter−to−emitter voltage at 450 V which enables systems requiring a higher spark voltage

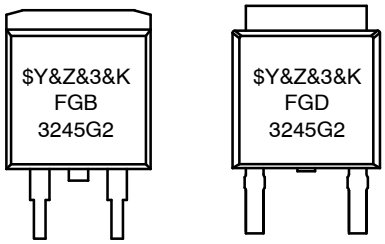
Features

- SCIS Energy = 320 mJ at T_J = 25°C
- Logic Level Gate Drive
- Low Saturation Voltage
- AEC−Q101 Qualified and PPAP Capable
- These Devices are Pb−Free and are RoHS Compliant

Applications

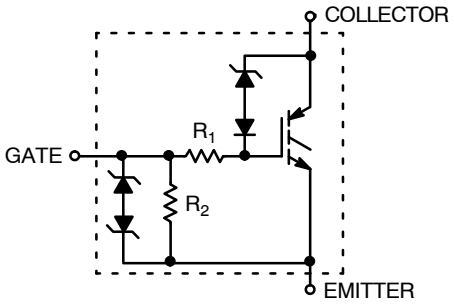
- Automotive Ignition Coil Driver Circuits
- Coil On Plug Applications

MARKING DIAGRAM



FGB3245G2 = Device Code
FGD3245G2
$Y = **onsemi** Logo
&Z = Assembly Plant Code
&3 = 3−Digit Date Code
&K = 2−Digits Lot Run Traceability Code

SYMBOL



ORDERING INFORMATION

See detailed ordering and shipping information on page 7 of this data sheet.

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DEVICE MAXIMUM RATINGS (T_A = 25°C unless otherwise noted)

Symbol	Parameter	Rating	Unit
BV_{CER}	Collector to Emitter Breakdown Voltage (I_C = 1 mA)	450	V
BV_{ECS}	Emitter to Collector Voltage − Reverse Battery Condition (I_C = 10 mA)	28	V
E_{SCIS25}	Self Clamping Inductive Switching Energy (Note 1)	320	mJ
$E_{SCIS150}$	Self Clamping Inductive Switching Energy (Note 2)	180	mJ
I_{C25}	Collector Current Continuous, at V_{GE} = 5 V, T_C = 25°C	41	A
I_{C110}	Collector Current Continuous, at V_{GE} = 5 V, T_C = 110°C	27	A
V_{GEM}	Gate to Emitter Voltage Continuous	±10	V
P_D	Power Dissipation Total, at T_C = 25°C	150	W
	Power Dissipation Derating, for T_C > 25°C	1.1	W/°C
T_J	Operating Junction Temperature Range	−40 to +175	°C
T_{STG}	Storage Junction Temperature Range	−40 to +175	°C
T_L	Max. Lead Temp. for Soldering (Leads at 1.6 mm from case for 10 s)	300	°C
T_{PKG}	Max. Lead Temp. for Soldering (Package Body for 10 s)	260	°C
ESD	Electrostatic Discharge Voltage at 100 pF, 1500 Ω	4	kV
	CDM−Electrostatic Discharge Voltage at 1 Ω	2	kV

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. Self Clamping Inductive Switching Energy (E_{SCIS25}) of 320 mJ is based on the test conditions that starting Tj = 25°C; L = 3 mHy, I_{SCIS} = 14.6 A, V_{CC} = 100 V during inductor charging and V_{CC} = 0 V during the time in clamp.
2. Self Clamping Inductive Switching Energy ($E_{SCIS150}$) of 180 mJ is based on the test conditions that starting Tj = 150°C; L = 3 mHy, I_{SCIS} = 10.9 A, V_{CC} = 100 V during inductor charging and V_{CC} = 0 V during the time in clamp.

ELECTRICAL CHARACTERISTICS (T_J = 25°C unless otherwise noted)

Symbol	Parameter	Test Conditions		Min	Typ	Max	Unit
OFF STATE CHARACTERISTICS							
BV_{CER}	Collector to Emitter Breakdown Voltage	I_{CE} = 2 mA, V_{GE} = 0, R_{GE} = 1 kΩ, T_J = −40 to 150°C		420	–	480	V
BV_{CES}	Collector to Emitter Breakdown Voltage	I_{CE} = 10 mA, V_{GE} = 0 V, R_{GE} = 0, T_J = −40 to 150°C		440	–	500	V
BV_{ECS}	Emitter to Collector Breakdown Voltage	I_{CE} = −75 mA, V_{GE} = 0 V, T_J = 25°C		28	–	–	V
BV_{GES}	Gate to Emitter Breakdown Voltage	I_{GES} = ±2 mA		±12	±14	–	V
I_{CER}	Collector to Emitter Leakage Current	V_{CE} = 250 V, R_{GE} = 1 kΩ	T_J = 25°C	–	–	25	μA
			T_J = 150°C	–	–	1	mA
I_{ECS}	Emitter to Collector Leakage Current	V_{EC} = 24 V	T_J = 25°C	–	–	1	mA
			T_J = 150°C	–	–	40	
R_1	Series Gate Resistance			–	120	–	Ω
R_2	Gate to Emitter Resistance			10 k	–	30 k	Ω
ON STATE CHARACTERISTICS							
$V_{CE(SAT)}$	Collector to Emitter Saturation Voltage	I_{CE} = 6 A, V_{GE} = 4 V	T_J = 25°C	–	1.13	1.25	V
$V_{CE(SAT)}$	Collector to Emitter Saturation Voltage	I_{CE} = 10 A, V_{GE} = 4.5 V	T_J = 150°C	–	1.32	1.50	V
$V_{CE(SAT)}$	Collector to Emitter Saturation Voltage	I_{CE} = 15 A, V_{GE} = 4.5 V	T_J = 150°C	–	1.64	1.85	V
DYNAMIC CHARACTERISTICS							
$Q_{G(ON)}$	Gate Charge	I_{CE} = 10 A, V_{CE} = 12 V, V_{GE} = 5 V		–	23	–	nC
$V_{GE(TH)}$	Gate to Emitter Threshold Voltage	I_{CE} = 1 mA, V_{CE} = V_{GE}	T_J = 25°C	1.3	1.6	2.2	V
			T_J = 150°C	0.75	1.1	1.8	
V_{GEP}	Gate to Emitter Plateau Voltage	V_{CE} = 12 V, I_{CE} = 10 A		–	2.7	–	V
SWITCHING CHARACTERISTICS							
$t_{d(ON)R}$	Current Turn−On Delay Time−Resistive	V_{CE} = 14 V, R_L = 1 kΩ V_{GE} = 5 V, R_G = 1 kΩ, T_J = 25°C		–	0.9	4	μs
t_{rR}	Current Rise Time−Resistive			–	2.6	7	μs
$t_{d(OFF)L}$	Current Turn−Off Delay Time−Inductive	V_{CE} = 300 V, L = 1 mH, V_{GE} = 5 V, R_G = 1 kΩ, I_{CE} = 6.5 A, T_J = 25°C		–	5.4	15	μs
t_{fL}	Current Fall Time−Inductive			–	2.7	15	μs
E_{SCIS}	Self Clamped Inductive Switching	L = 3.0 mHy, R_G = 1 kΩ, V_{GE} = 5 V, (Note 3)	T_J = 25°C	–	–	320	mJ
THERMAL CHARACTERISTICS							
$R_{\theta JC}$	Thermal Resistance Junction to Case	All packages		–	–	0.9	°C/W

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

3. Self Clamping Inductive Switching Energy (E_{SCIS25}) of 320 mJ is based on the test conditions that starting Tj = 25°C; L = 3 mHy, I_{SCIS} = 14.6 A, V_{CC} = 100 V during inductor charging and V_{CC} = 0 V during the time in clamp.

TYPICAL PERFORMANCE CURVES

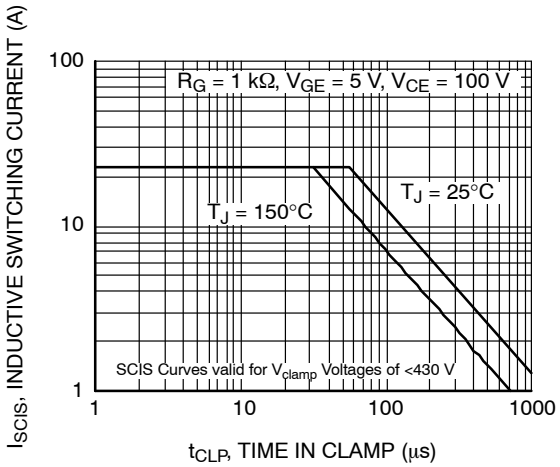


Figure 1. Self Clamped Inductive Switching Current vs. Time in Clamp

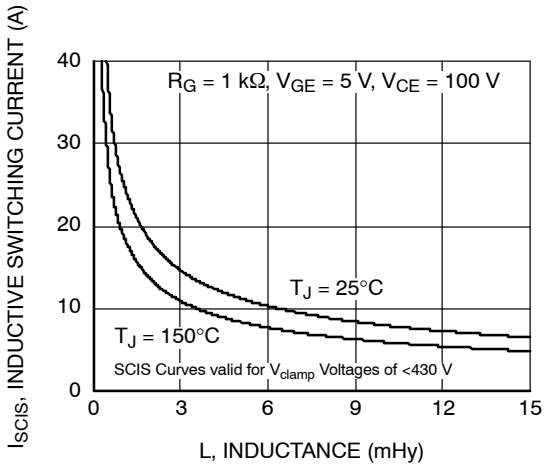


Figure 2. Self Clamped Inductive Switching Current vs. Inductance

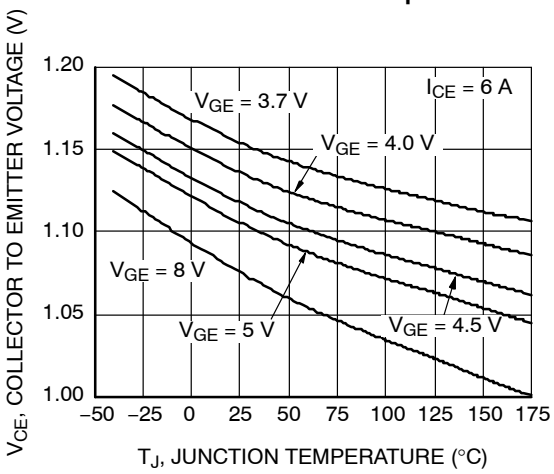


Figure 3. Collector to Emitter On−State Voltage vs. Junction Temperature

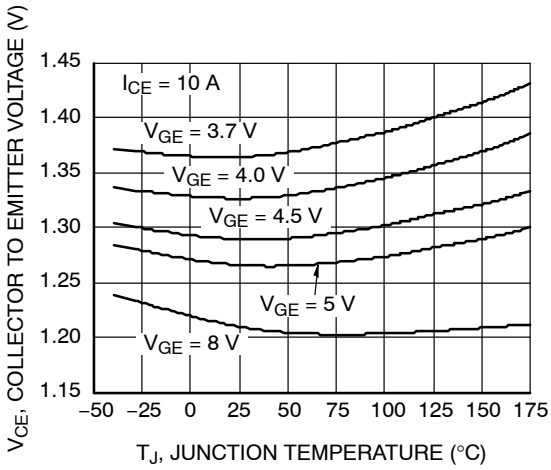


Figure 4. Collector to Emitter On−State Voltage vs. Junction Temperature

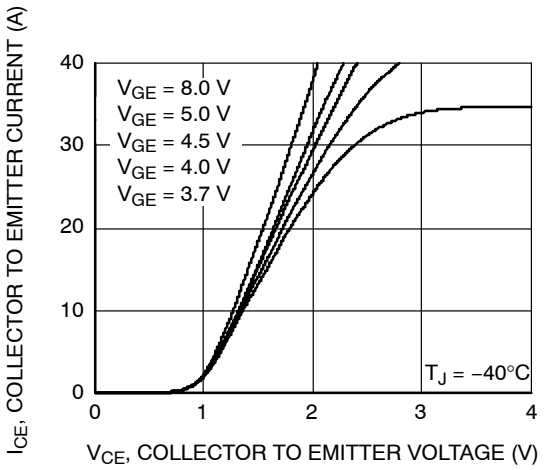


Figure 5. Collector to Emitter On−State Voltage vs. Collector Current

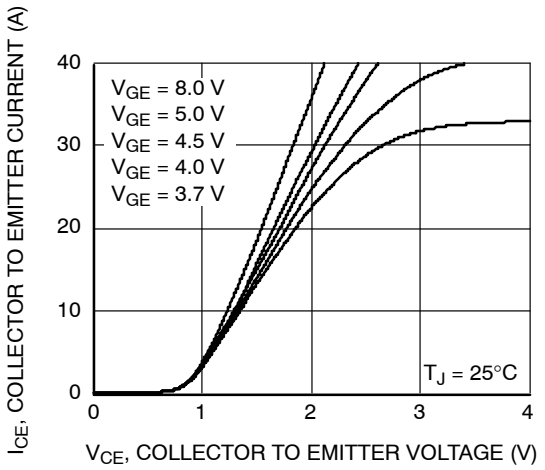


Figure 6. Collector to Emitter On−State Voltage vs. Collector Current

TYPICAL PERFORMANCE CURVES (Continued)

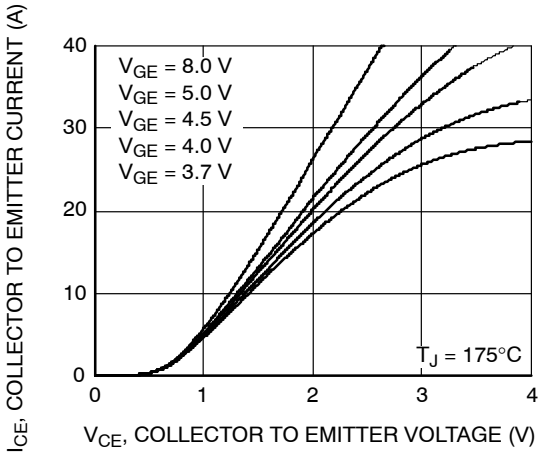


Figure 7. Collector to Emitter On−Stage Voltage vs. Collector Current

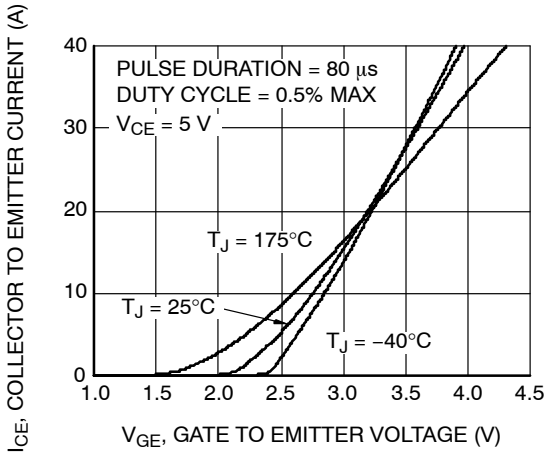


Figure 8. Transfer Characteristics

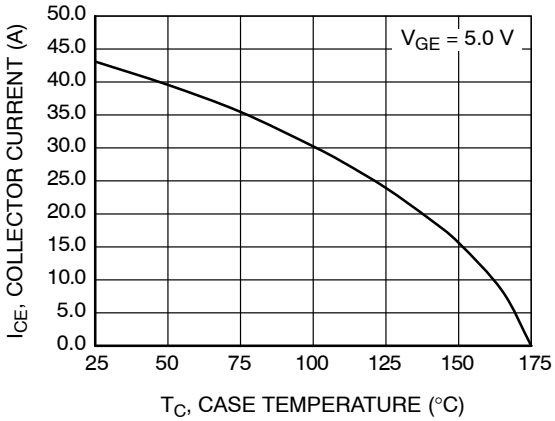


Figure 9. DC Collector Current vs. Case Temperature

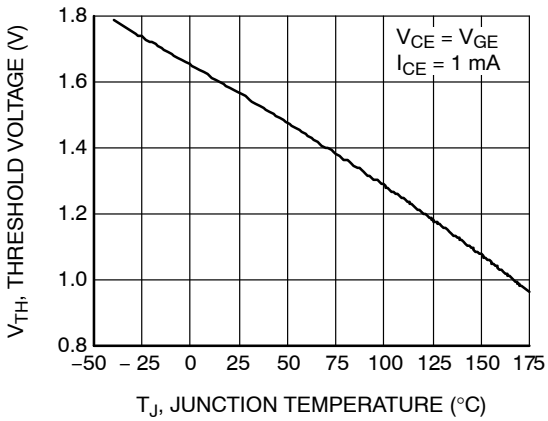


Figure 10. Threshold Voltage vs. Junction Temperature

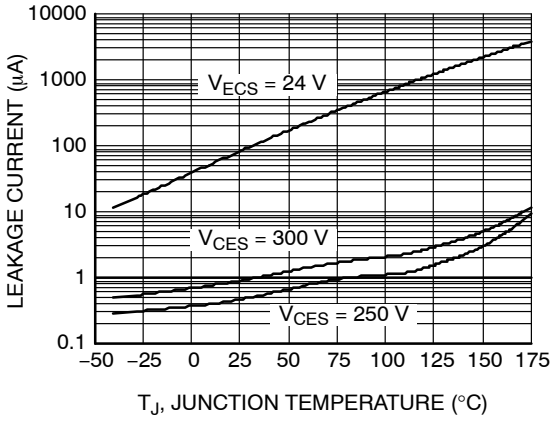


Figure 11. Leakage Current vs. Junction Temperature

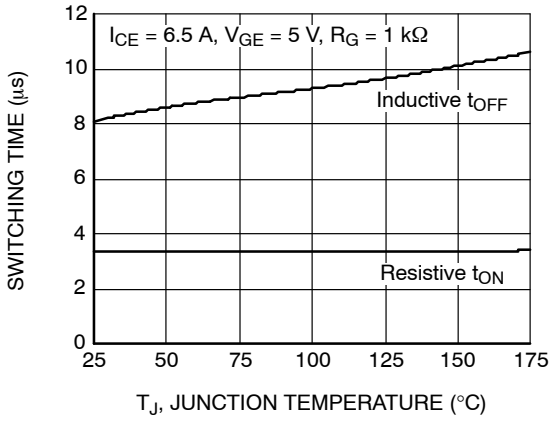


Figure 12. Switching Time vs. Junction Temperature

TYPICAL PERFORMANCE CURVES (Continued)

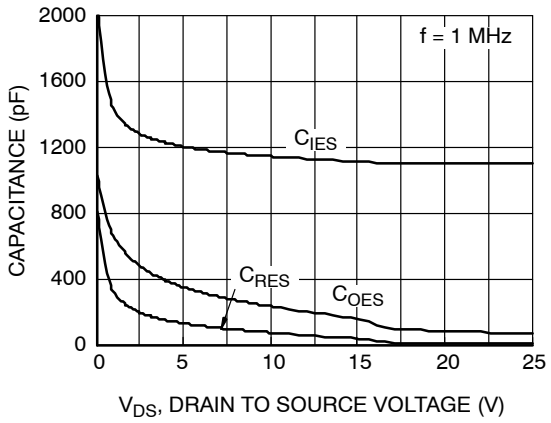


Figure 13. Capacitance Collector to Emitter Voltage

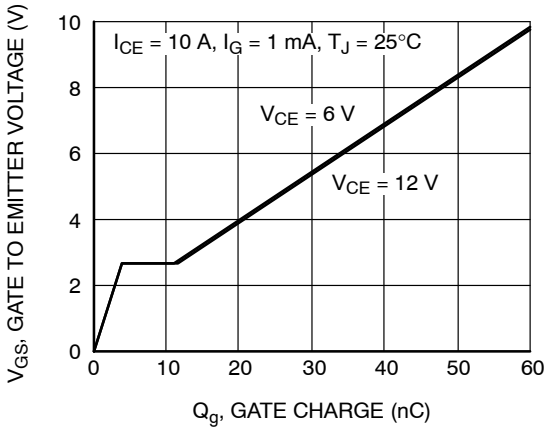


Figure 14. Gate Charge

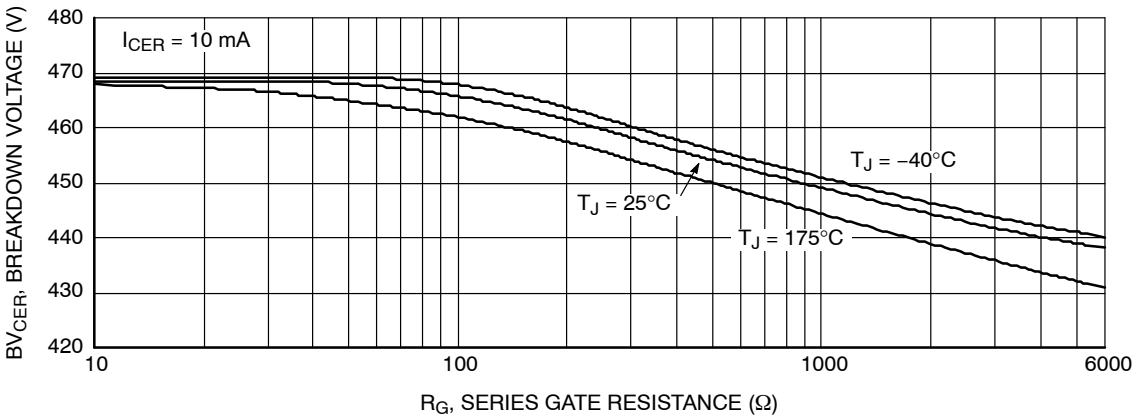


Figure 15. Breakdown Voltage vs. Series Gate Resistance

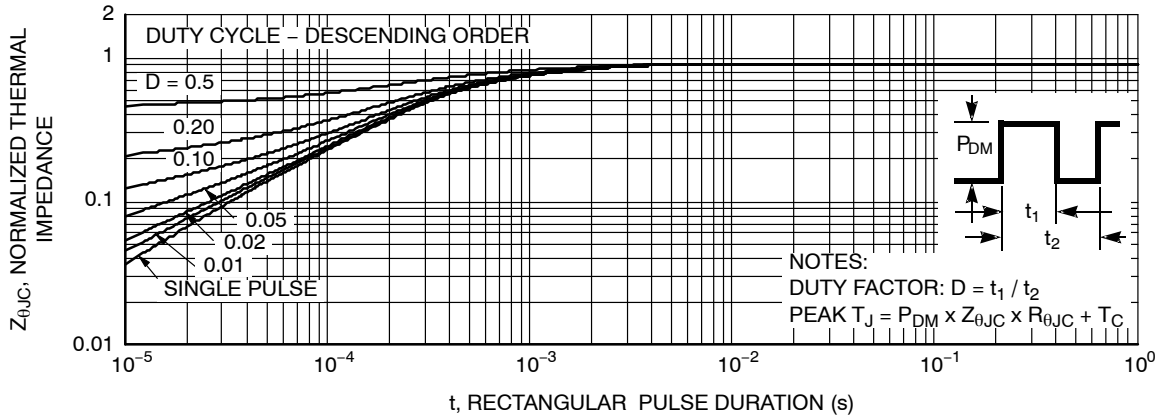


Figure 16. IGBT Normalized Transient Thermal Impedance, Junction to Case

TESTE CIRCUITS AND WAVEFORMS

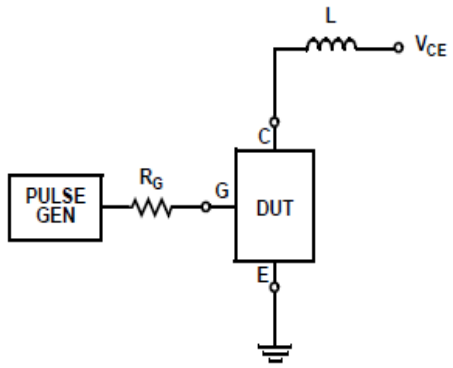


Figure 17. Inductive Switching Test Circuit

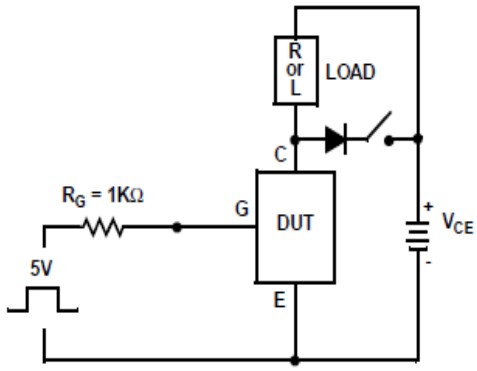


Figure 18. t_{ON} and t_{OFF} Switching Test Circuit

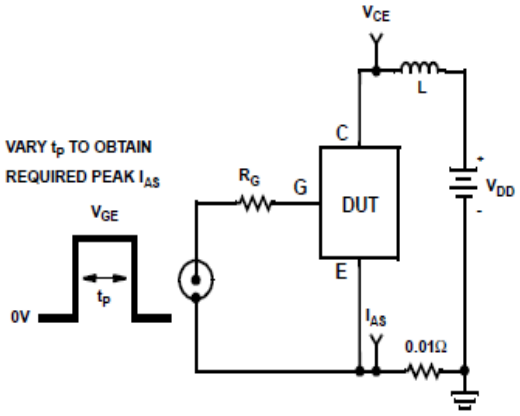


Figure 19. Energy Test Circuit

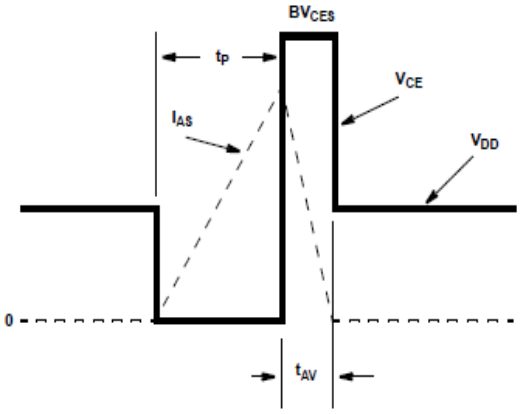


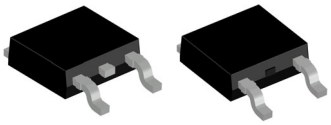
Figure 20. Energy Waveforms

PACKAGE MARKING AND ORDERING INFORMATION

Device Marking	Device	Package	Reel Size	Tape Width	Shipping†
FGD3245G2	FGD3245G2−F085	DPAK3 (TO−252 3 LD) TO252AA (Pb−Free)	330 mm	16 mm	2500 / Tape & Reel
FGB3245G2	FGB3245G2−F085	D^2PAK−3 (TO−263, 3−LEAD) TO263AB (Pb−Free)	330 mm	24 mm	800 / Tape & Reel

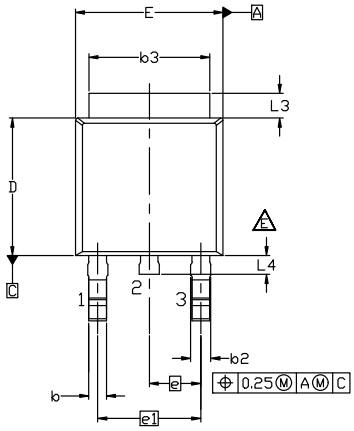
†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

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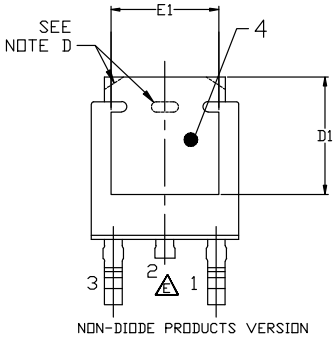


DPAK3 6.10x6.54x2.29, 4.57P
CASE 369AS
ISSUE B

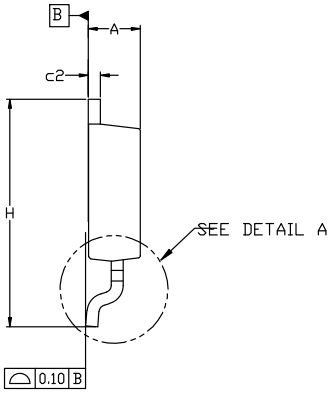
DATE 20 DEC 2023



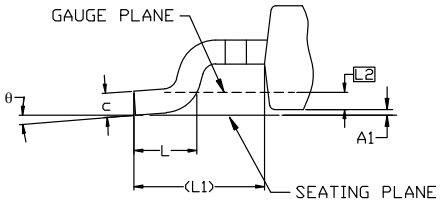
NON-DIODE PRODUCTS VERSION



NON-DIODE PRODUCTS VERSION

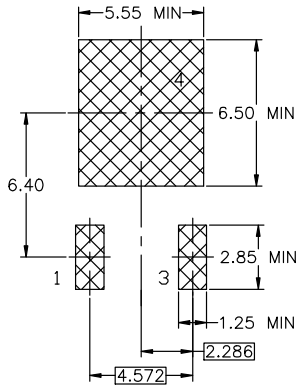


NOTES: UNLESS OTHERWISE SPECIFIED
A) THIS PACKAGE CONFORMS TO JEDEC, TO-252, ISSUE F, VARIATION AA.
B) ALL DIMENSIONS ARE IN MILLIMETERS.
C) DIMENSIONING AND TOLERANCING PER ASME Y14.5M-2018.
D) SUPPLIER DEPENDENT MOLD LOCKING HOLES OR CHAMFERED CORNERS OR EDGE PROTRUSION.
E) FOR DIODE PRODUCTS, L4 IS 0.25 MM MAX PLASTIC BODY STUB WITHOUT CENTER LEAD.
F) DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLD FLASH AND TIE BAR EXTRUSIONS.
G) LAND PATTERN RECOMMENDATION IS BASED ON IPC7351A STD TO228P991X239-3N.



DETAIL A
(ROTATED -90°)
SCALE: 12X

DIM	MILLIMETERS		
	MIN.	NOM.	MAX.
A	2.18	2.29	2.39
A1	0.00	–	0.127
b	0.64	0.77	0.89
b2	0.76	0.95	1.14
b3	5.21	5.34	5.46
c	0.45	0.53	0.61
c2	0.45	0.52	0.58
D	5.97	6.10	6.22
D1	5.21	---	---
E	6.35	6.54	6.73
E1	4.32	---	---
e	2.286 BSC		
e1	4.572 BSC		
H	9.40	9.91	10.41
L	1.40	1.59	1.78
L1	2.90 REF		
L2	0.51 BSC		
L3	0.89	1.08	1.27
L4	---	---	1.02
θ	0°	---	10°



LAND PATTERN RECOMMENDATION

*FOR ADDITIONAL INFORMATION ON OUR PB-FREE STRATEGY AND SOLDERING DETAILS, PLEASE DOWNLOAD THE ON SEMICONDUCTOR SOLDERING AND MOUNTING TECHNIQUES REFERENCE MANUAL, SOLDERRM/D.

GENERIC MARKING DIAGRAM*



*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, “G” or microdot “▪”, may or may not be present. Some products may not follow the Generic Marking.

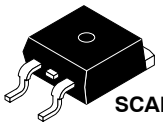
XXXX = Specific Device Code
A = Assembly Location
Y = Year
WW = Work Week
ZZ = Assembly Lot Code

DOCUMENT NUMBER:	**98AON13810G**	Electronic versions are uncontrolled except when accessed directly from the Document Repository. Printed versions are uncontrolled except when stamped “CONTROLLED COPY” in red.
DESCRIPTION:	**DPAK3 6.10x6.54x2.29, 4.57P**	**PAGE 1 OF 1**

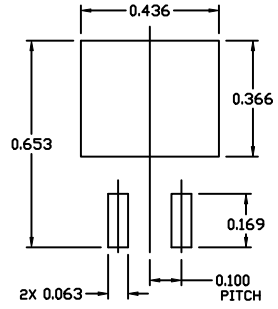
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D²PAK–3 (TO–263, 3–LEAD)
CASE 418AJ
ISSUE F

DATE 11 MAR 2021



SCALE 1:1



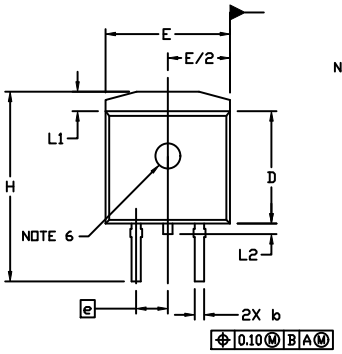
RECOMMENDED
MOUNTING FOOTPRINT

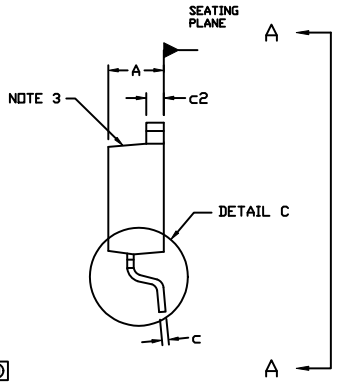
* For additional information on our Pb–Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

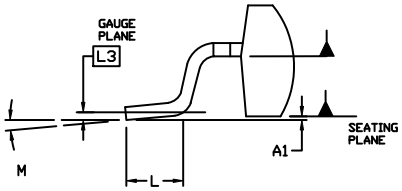
NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 2009.
2. CONTROLLING DIMENSION: INCHES
3. CHAMFER OPTIONAL.
4. DIMENSIONS D AND E DO NOT INCLUDE MOLD FLASH. MOLD FLASH SHALL NOT EXCEED 0.005 PER SIDE. THESE DIMENSIONS ARE MEASURED AT THE OUTERMOST EXTREMES OF THE PLASTIC BODY AT DATUM H.
5. THERMAL PAD CONTOUR IS OPTIONAL WITHIN DIMENSIONS E, L1, D1, AND E1.
6. OPTIONAL MOLD FEATURE.
7. ①, ② … OPTIONAL CONSTRUCTION FEATURE CALL OUTS.

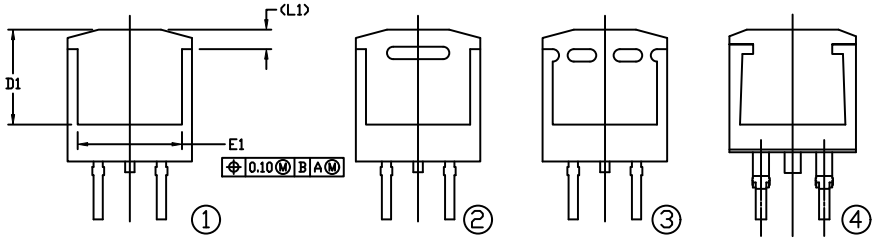
	INCHES		MILLIMETERS	
DIM	MIN.	MAX.	MIN.	MAX.
A	0.160	0.190	4.06	4.83
A1	0.000	0.010	0.00	0.25
b	0.020	0.039	0.51	0.99
c	0.012	0.029	0.30	0.74
c2	0.045	0.065	1.14	1.65
D	0.330	0.380	8.38	9.65
D1	0.260	---	6.60	---
E	0.380	0.420	9.65	10.67
E1	0.245	---	6.22	---
e	0.100 BSC		2.54 BSC	
H	0.575	0.625	14.60	15.88
L	0.070	0.110	1.78	2.79
L1	---	0.066	---	1.68
L2	---	0.070	---	1.78
L3	0.010 BSC		0.25 BSC	
M	0°	8°	0°	8°







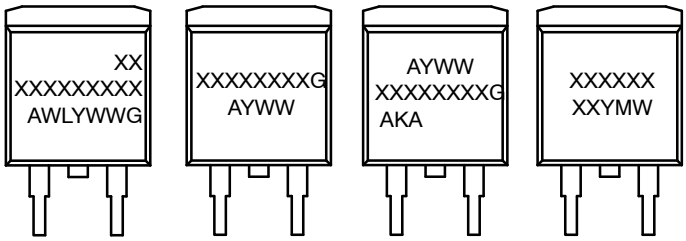
DETAIL C
TIP LEADFORM
ROTATED 90° CW



VIEW A–A

VIEW A–A
OPTIONAL CONSTRUCTIONS

GENERIC MARKING DIAGRAMS*



IC **Standard** **Rectifier** **SSG**

XXXXXX = Specific Device Code
A = Assembly Location
WL = Wafer Lot
Y = Year
WW = Work Week
W = Week Code (SSG)
M = Month Code (SSG)
G = Pb–Free Package
AKA = Polarity Indicator

*This information is generic. Please refer to device data sheet for actual part marking. Pb–Free indicator, “G” or microdot “ ▪”, may or may not be present. Some products may not follow the Generic Marking.

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DESCRIPTION:	**D²PAK–3 (TO–263, 3–LEAD)**	**PAGE 1 OF 1**

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