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FQD3N60CTM-WS

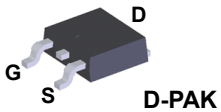
N-Channel QFET® MOSFET
600 V, 2.4 A, 3.4 Ω

Features

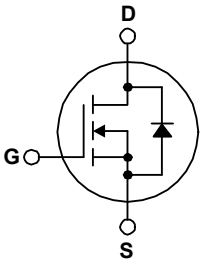
- 2.4 A, 600 V, $R_{DS(on)}$ = 3.4 Ω (Max.) @ V_{GS} = 10 V, I_D = 1.2 A
- Low Gate Charge (Typ. 10.5 nC)
- Low Crss (Typ. 5 pF)
- 100% Avalanche Tested

Description

This N-Channel enhancement mode power MOSFET is produced using ON Semiconductor's proprietary planar stripe and DMOS technology. This advanced MOSFET technology has been especially tailored to reduce on-state resistance, and to provide superior switching performance and high avalanche energy strength. These devices are suitable for switched mode power supplies, active power factor correction (PFC), and electronic lamp ballasts.



D-PAK



Absolute Maximum Ratings T_C = 25°C unless otherwise noted.

Symbol	Parameter		FQD3N60CTM_WS	Unit
V_{DSS}	Drain-Source Voltage		600	V
I_D	Drain Current - Continuous (T_C = 25°C)		2.4	A
	Drain Current - Continuous (T_C = 100°C)		1.5	A
I_{DM}	Drain Current - Pulsed	(Note 1)	9.6	A
V_{GSS}	Gate-Source Voltage		±30	V
E_{AS}	Single Pulsed Avalanche Energy	(Note 2)	150	mJ
I_{AR}	Avalanche Current	(Note 1)	2.4	A
E_{AR}	Repetitive Avalanche Energy	(Note 1)	4.0	mJ
dv/dt	Peak Diode Recovery dv/dt	(Note 3)	4.5	V/ns
P_D	Power Dissipation (T_C = 25°C)		50	W
	- Derate above 25°C		0.4	W/°C
T_J, T_{STG}	Operating and Storage Temperature Range		-55 to +150	°C
T_L	Maximum lead temperature for soldering purposes, 1/8" from case for 5 seconds		300	°C

Thermal Characteristics

Symbol	Parameter	FQD3N60CTM_WS	Unit
$R_{\theta JC}$	Thermal Resistance, Junction-to-Case, Max.	2.5	°C/W
$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient, Max.	110	°C/W

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Package Marking and Ordering Information

Device Marking	Device	Package	Reel Size	Tape Width	Quantity
FQD3N60CS	FQD3N60CTM-WS	D-PAK	330 mm	16 mm	2500 units

Electrical Characteristics T_C = 25°C unless otherwise noted.

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
Off Characteristics						
BV_{DSS}	Drain-Source Breakdown Voltage	V_{GS} = 0V, I_D = 250μA	600	--	--	V
ΔBV_{DSS} /ΔT_J	Breakdown Voltage Temperature Coefficient	I_D = 250μA, Referenced to 25°C	--	0.6	--	V/°C
I_{DSS}	Zero Gate Voltage Drain Current	V_{DS} = 600 V, V_{GS} = 0 V	--	--	1	μA
		V_{DS} = 480 V, T_C = 125°C	--	--	10	μA
I_{GSSF}	Gate-Body Leakage Current, Forward	V_{GS} = 30V, V_{DS} = 0V	--	--	100	nA
I_{GSSR}	Gate-Body Leakage Current, Reverse	V_{GS} = -30V, V_{DS} = 0V	600	--	-100	nA
On Characteristics						
$V_{GS(th)}$	Gate Threshold Voltage	V_{DS} = V_{GS}, I_D = 250μA	2.0	--	4.0	V
$R_{DS(on)}$	Static Drain-Source On-Resistance	V_{GS} = 10V, I_D = 1.2A	--	2.8	3.4	Ω
g_{FS}	Forward Transconductance	V_{DS} = 40V, I_D = 1.2A	--	3.5	--	S
Dynamic Characteristics						
C_{iss}	Input Capacitance	V_{DS} = 25V, V_{GS} = 0V, f = 1.0MHz	--	435	565	pF
C_{oss}	Output Capacitance		--	45	60	pF
C_{rss}	Reverse Transfer Capacitance		--	5	8	pF
Switching Characteristics						
$t_{d(on)}$	Turn-On Delay Time	V_{DD} = 300 V, I_D = 3 A, R_G = 25 Ω (Note 4)	--	12	34	ns
t_r	Turn-On Rise Time		--	30	70	ns
$t_{d(off)}$	Turn-Off Delay Time		--	35	80	ns
t_f	Turn-Off Fall Time		--	35	80	ns
Q_g	Total Gate Charge	V_{DS} = 480 V, I_D = 3 A, V_{GS} = 10 V (Note 4)	--	10.5	14	nC
Q_{gs}	Gate-Source Charge		--	2.1	--	nC
Q_{gd}	Gate-Drain Charge		--	4.5	--	nC
Drain-Source Diode Characteristics and Maximum Ratings						
I_S	Maximum Continuous Drain-Source Diode Forward Current		--	--	3	A
I_{SM}	Maximum Pulsed Drain-Source Diode Forward Current		--	--	12	A
V_{SD}	Drain-Source Diode Forward Voltage	V_{GS} = 0V, I_S = 2.4A	--	--	1.4	V
t_{rr}	Reverse Recovery Time	V_{GS} = 0V, I_S = 3A, dI_F/dt =100A/μs	--	260	--	ns
Q_{rr}	Reverse Recovery Charge		--	1.6	--	μC

NOTES:

1. Repetitive Rating: Pulse width limited by maximum junction temperature.
2. I_{AS} = 2.4 A, V_{DD} = 50 V, L=47 mH, R_G = 25 Ω, starting T_J = 25°C.
3. I_{SD} ≤ 3 A, di/dt ≤ 200 A/μs, V_{DD} ≤ BV_{DSS}, starting T_J = 25°C.
4. Essentially independent of operating temperature.

Typical Performance Characteristics

Figure 1. On-Region Characteristics

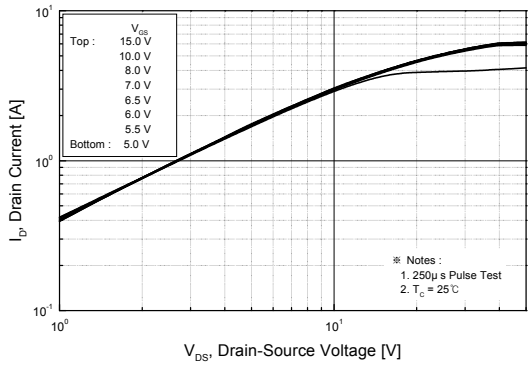


Figure 2. Transfer Characteristics

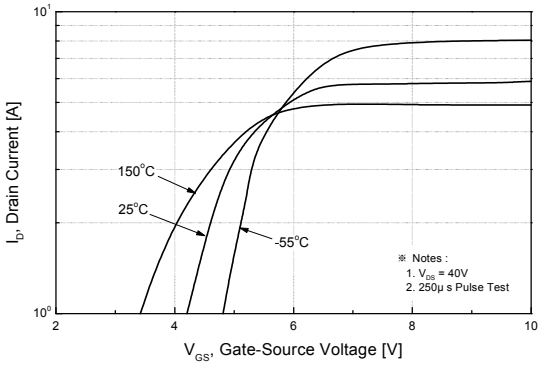


Figure 3. On-Resistance Variation vs. Drain Current and Gate Voltage

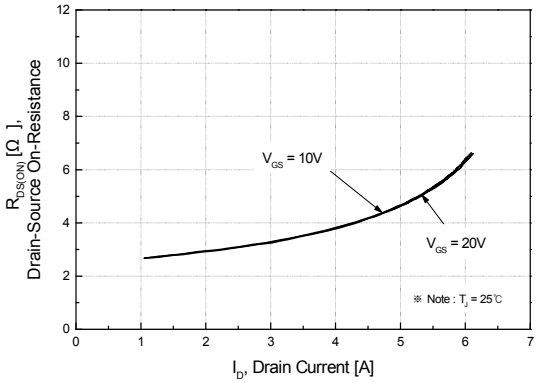


Figure 4. Body Diode Forward Voltage Variation vs. Source Current and Temperature

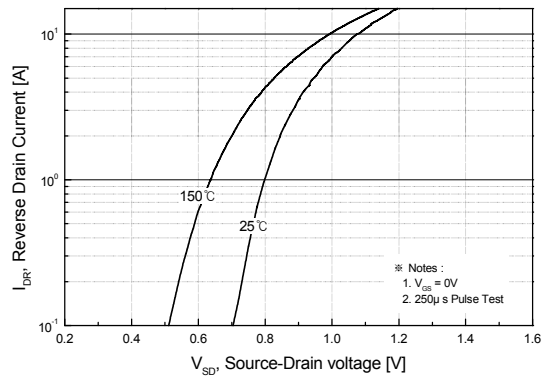


Figure 5. Capacitance Characteristics

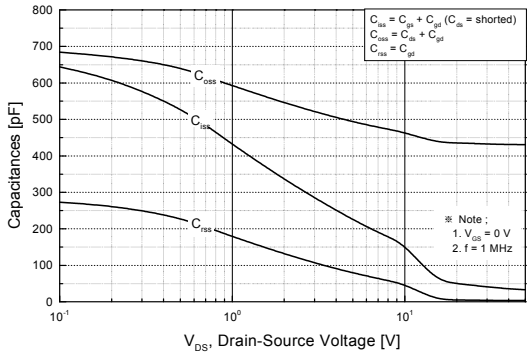
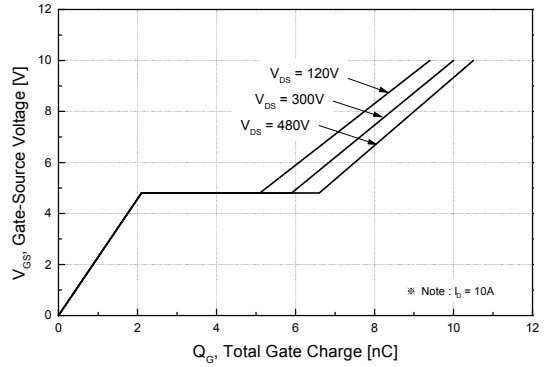


Figure 6. Gate Charge Characteristics



Typical Performance Characteristics (Continued)

Figure 7. Breakdown Voltage Variation vs. Temperature

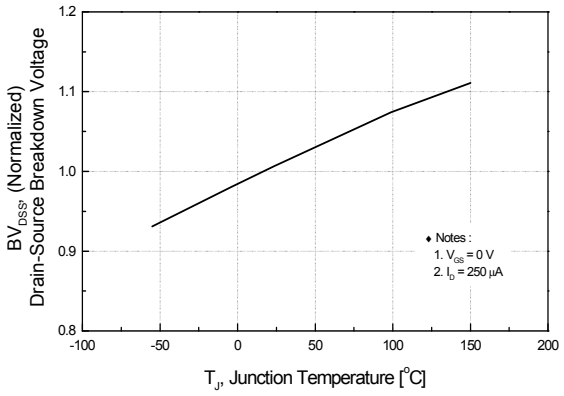


Figure 8. On-Resistance Variation vs. Temperature

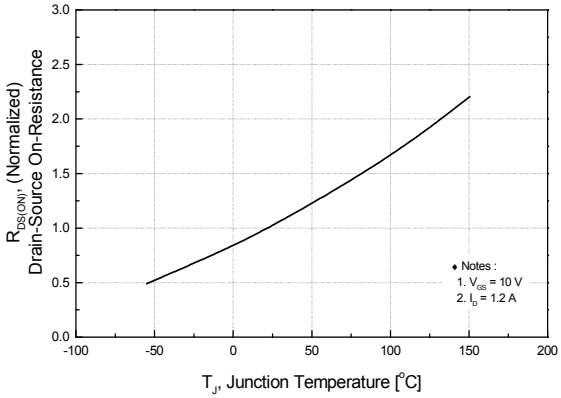


Figure 9. Maximum Safe Operating Area

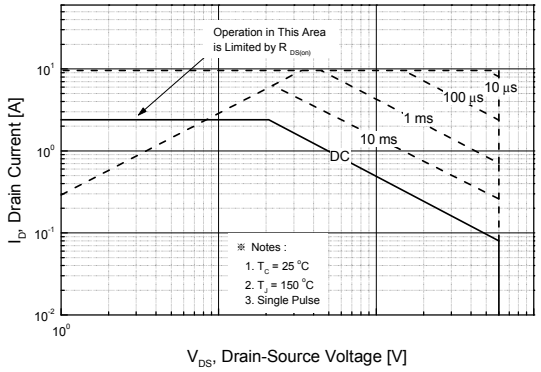


Figure 10. Maximum Drain Current vs. Case Temperature

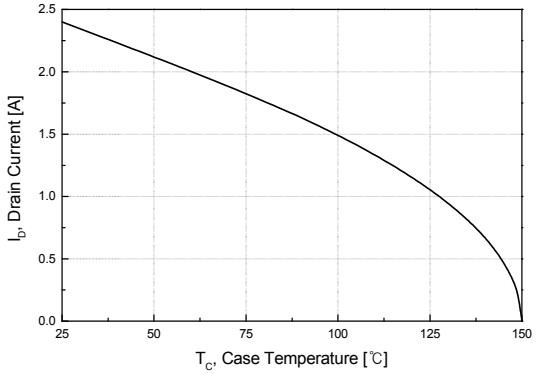


Figure 11. Transient Thermal Response Curve

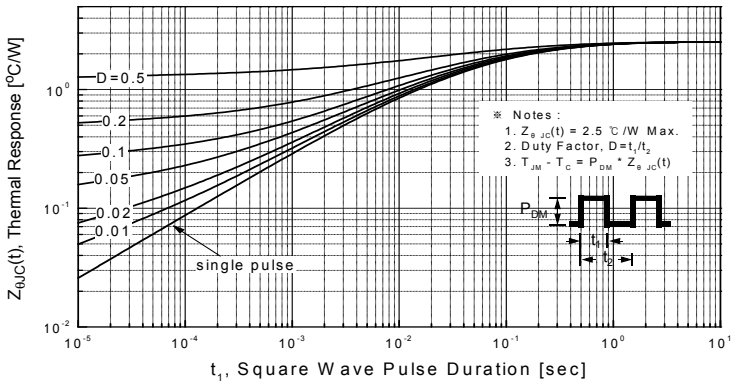


Figure 12. Gate Charge Test Circuit & Waveform

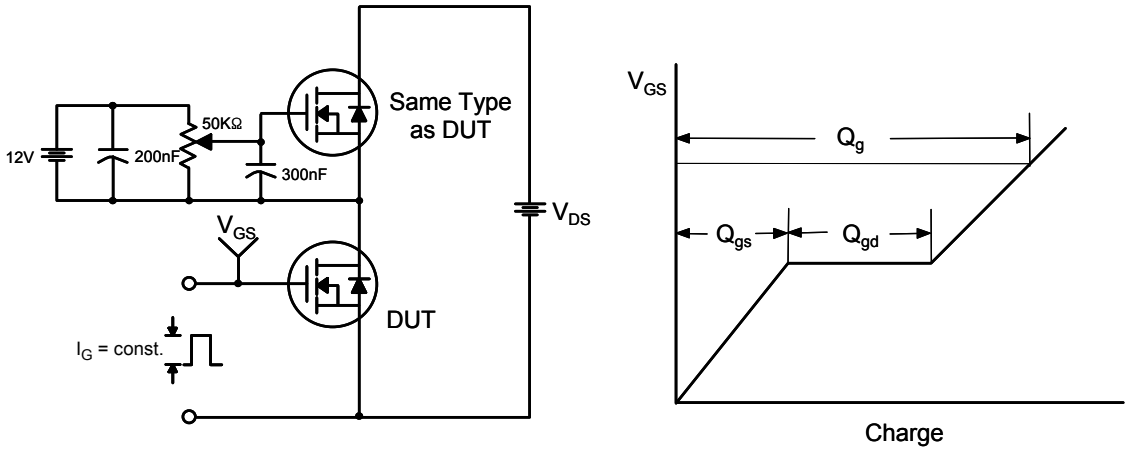


Figure 13. Resistive Switching Test Circuit & Waveforms

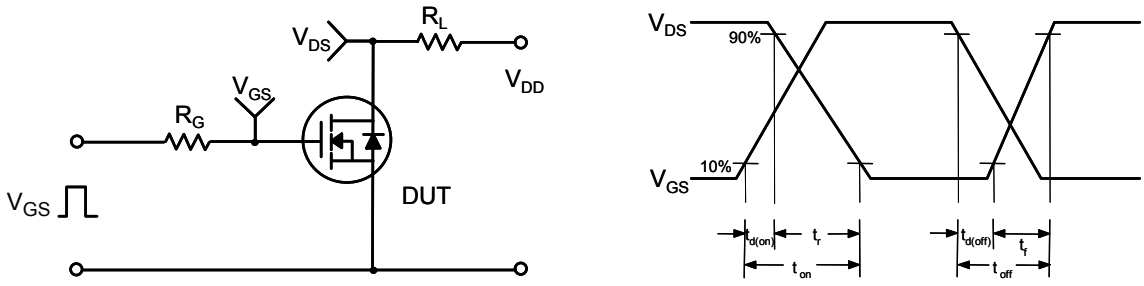


Figure 14. Unclamped Inductive Switching Test Circuit & Waveforms

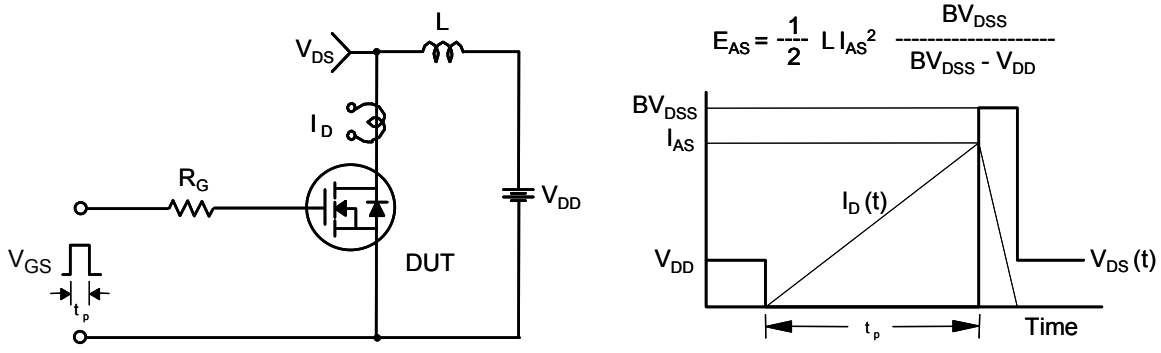
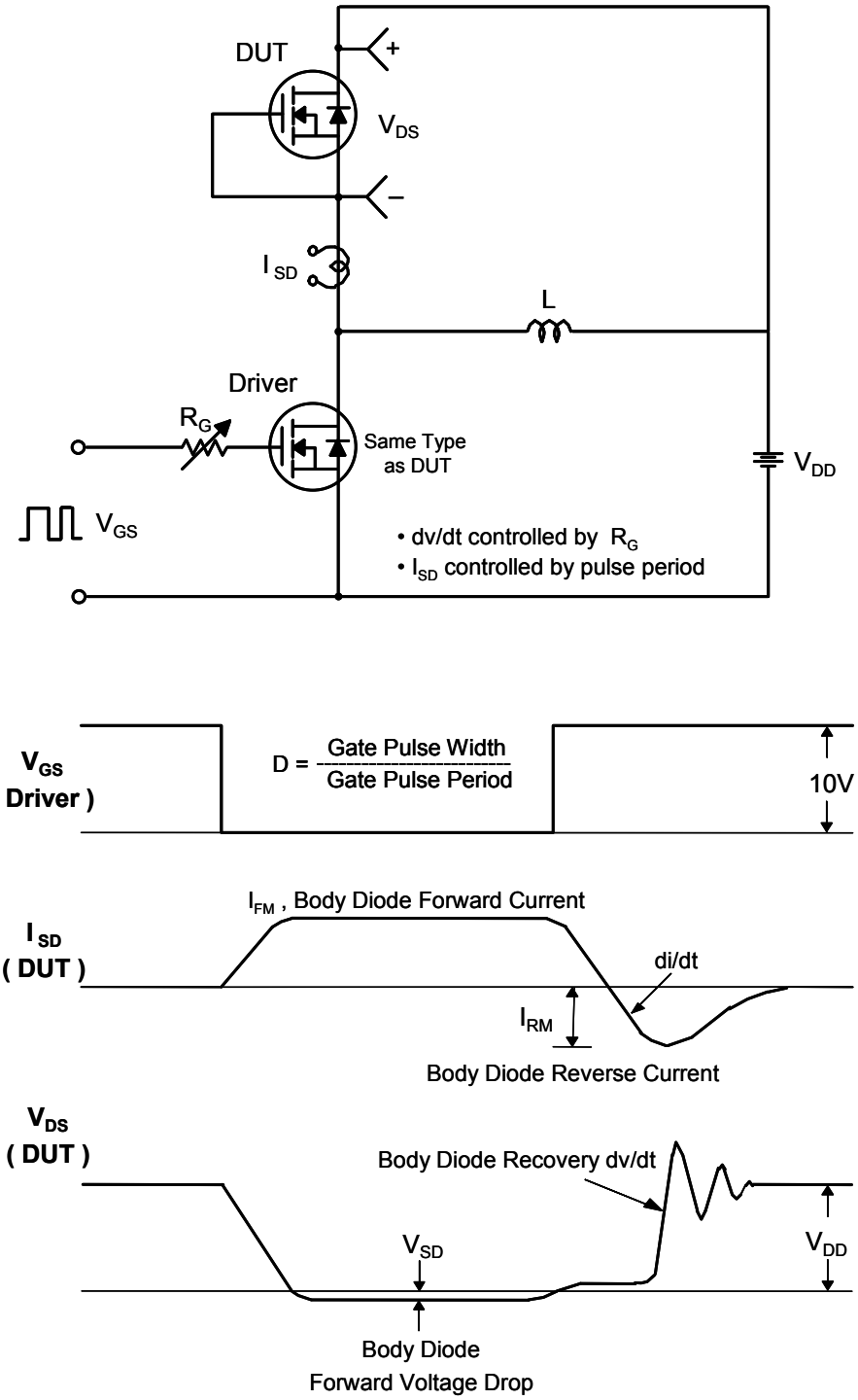
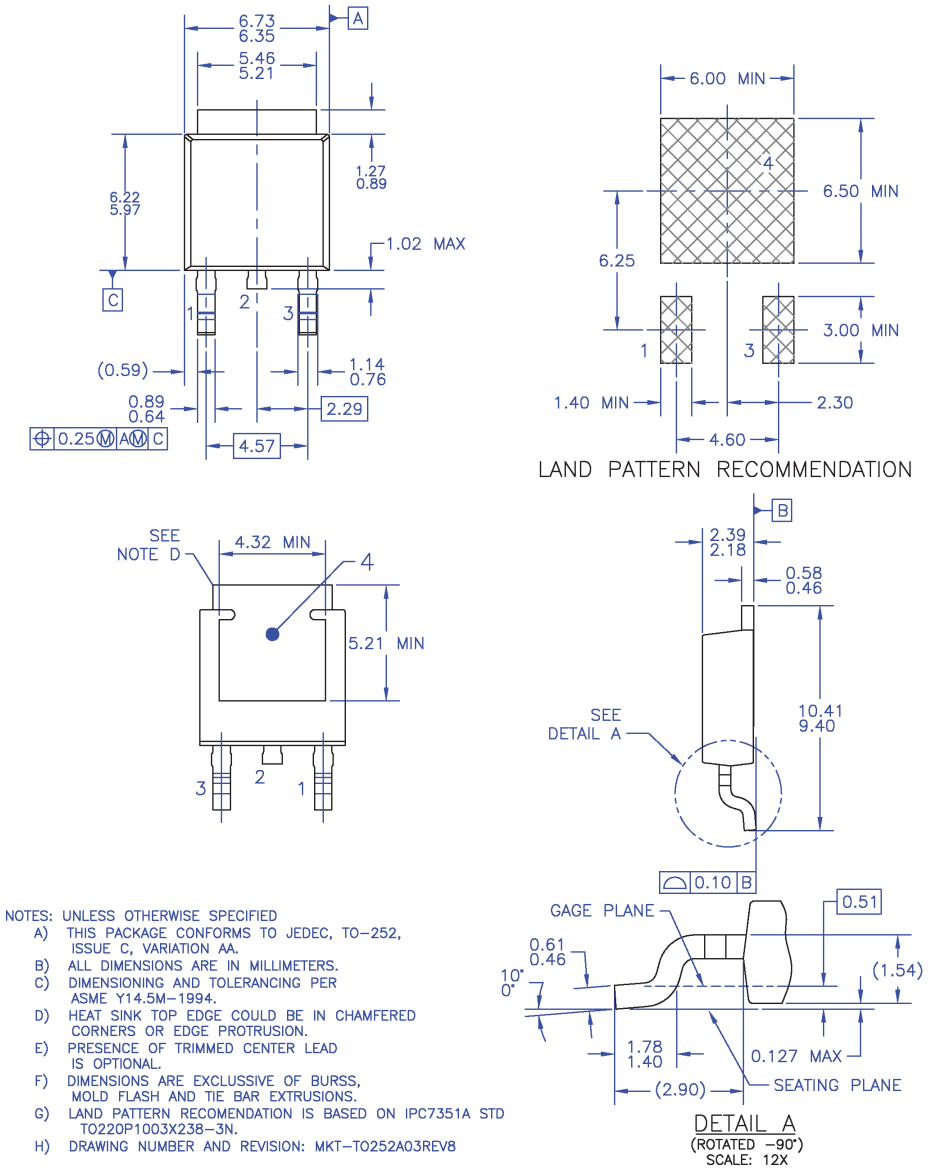


Figure 15. Peak Diode Recovery dv/dt Test Circuit & Waveforms



Mechanical Dimensions

TO-252 3L (DPAK)



NOTES: UNLESS OTHERWISE SPECIFIED

A) THIS PACKAGE CONFORMS TO JEDEC, TO−252, ISSUE C, VARIATION AA.
B) ALL DIMENSIONS ARE IN MILLIMETERS.
C) DIMENSIONING AND TOLERANCING PER ASME Y14.5M−1994.
D) HEAT SINK TOP EDGE COULD BE IN CHAMFERED CORNERS OR EDGE PROTRUSION.
E) PRESENCE OF TRIMMED CENTER LEAD IS OPTIONAL.
F) DIMENSIONS ARE EXCLUSSIVE OF BURSS, MOLD FLASH AND TIE BAR EXTRUSIONS.
G) LAND PATTERN RECOMENDATION IS BASED ON IPC7351A STD TO220P1003X238−3N.
H) DRAWING NUMBER AND REVISION: MKT−TO252A03REV8

Figure 16. TO252 (D-PAK), Molded, 3 Lead, Option AA&AB

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Dimension in Millimeters

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