MOSFET – N-Channel, QFET®

1000 V, 8.0 A, 1.45 Ω

FQH8N100C

Description

This N−Channel enhancement mode power MOSFET is produced using ON Semiconductor's proprietary planar stripe and DMOS technology. This advanced MOSFET technology has been especially tailored to reduce on−state resistance, and to provide superior switching performance and high avalanche energy strength. These devices are suitable for switched mode power supplies, active power factor correction (PFC), and electronic lamp ballasts.

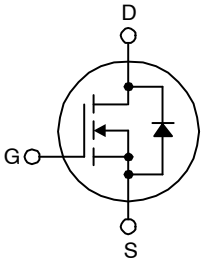
Features

- 8 A, 1000 V, $R_{DS(on)}$ = 1.45 Ω (Max.) @ V_{GS} = 10 V
- Low Gate Charge (Typ. 53 nC)
- Low Crss (Typ. 16 pF)
- Fast Switching
- 100% Avalanche Tested
- Improved dv/dt Capability
- This Device is Pb−Free and is RoHS Compliant

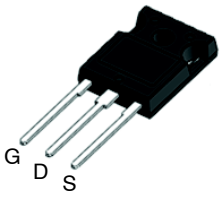
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V_{DS}	$R_{DS(ON)}$ MAX	I_D MAX
1000 V	1.45 Ω @ 10 V	8 A

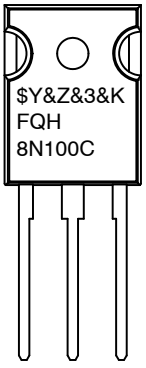


N-CHANNEL MOSFET



TO−247−3LD
CASE 340CK

MARKING DIAGRAM



$Y	= ON Semiconductor Logo
&Z	= Assembly Plant Code
&3	= Numeric Date Code
&K	= Lot Code
FQH8N100C	= Specific Device Code

ORDERING INFORMATION

See detailed ordering and shipping information on page 2 of this data sheet.

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ABSOLUTE MAXIMUM RATINGS (T_C = 25°C unless otherwise noted)

Symbol	Parameter		FQH8N100C	Unit
V_{DSS}	Drain−Source Voltage		1000	V
I_D	Drain Current:	Continuous (T_C = 25°C)	8.0	A
		Continuous (T_C = 100°C)	5.0	
I_{DM}	Drain Current:	Pulsed (Note 1)	32	A
V_{GSS}	Gate−Source Voltage		±30	V
E_{AS}	Single Pulsed Avalanche Energy (Note 2)		850	mJ
I_{AR}	Avalanche Current (Note 1)		8.0	A
E_{AR}	Repetitive Avalanche Energy (Note 1)		22	mJ
dv/dt	Peak Diode Recovery dv/dt (Note 3)		4.0	V/ns
P_D	Power Dissipation	T_C = 25°C	225	W
		Derate Above 25°C	1.79	W/°C
T_J, T_{STG}	Operating and Storage Temperature Range		−55 to + 150	°C
T_L	Maximum Lead Temperature for Soldering, 1/8″ from Case for 5 seconds		300	°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. Repetitive rating: Pulse−width limited by maximum junction temperature.
2. L = 25 mH, I_{AS} = 8.0 A, V_{DD} = 50 V, R_G = 25 Ω, Starting T_J = 25°C
3. I_{SD} ≤ 8.0 A, di/dt ≤ 200 A/μs, V_{DD} ≤ BV_{DSS}, Starting T_J = 25 °C.

PACKAGE MARKING AND ORDERING INFORMATION

Part Number	Top Marking	Package	Packing Method	Reel Size	Tape Width	Quantity
FQH8N100C	FQH8N100C	TO−247	Tube	N/A	N/A	30 Units

THERMAL CHARACTERISTICS

Symbol	Parameter	FQH8N100C	Unit
$R_{\theta JC}$	Thermal Resistance, Junction to Case, Max.	0.56	°C/W
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient, Max.	40	

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
OFF CHARACTERISTICS						
BV_{DSS}	Drain−Source Breakdown Voltage	V_{GS} = 0 V, I_D = 250 μA	1000	–	–	V
$\Delta BV_{DSS}/\Delta T_J$	Breakdown Voltage Temperature Coefficient	I_D = 250 μA, Referenced to 25°C	–	1.4	–	V/°C
I_{DSS}	Zero Gate Voltage Drain Current	V_{DS} = 1000 V, V_{GS} = 0 V	–	–	10	μA
		V_{DS} = 800 V, T_C = 125 °C	–	–	100	μA
I_{GSSF}	Gate−Body Leakage Current, Forward	V_{GS} = 30 V, V_{DS} = 0 V	–	–	100	nA
I_{GSSR}	Gate−Body Leakage Current, Reverse	V_{GS} = −30 V, V_{DS} = 0 V	–	–	−100	nA
ON CHARACTERISTICS						
$V_{GS(th)}$	Gate Threshold Voltage	V_{GS} = V_{DS}, I_D = 250 μA	3.0	–	5.0	V
$R_{DS(on)}$	Static Drain−Source On−Resistance	V_{GS} = 10 V, I_D = 4.0 A	–	1.2	1.45	Ω
g_{FS}	Forward Transconductance	V_{DS} = 50 V, I_D = 4.0 A	–	8.0	–	S
DYNAMIC CHARACTERISTICS						
C_{iss}	Input Capacitance	V_{DS} = 25 V, V_{GS} = 0 V, f = 1.0 MHz	–	2475	3220	pF
C_{oss}	Output Capacitance		–	195	255	pF
C_{rss}	Reverse Transfer Capacitance		–	16	21	pF
SWITCHING CHARACTERISTICS						
$t_{d(on)}$	Turn-On Delay Time	V_{DD} = 500 V, I_D = 8.0 A, R_G = 25 Ω (Note 4)	–	50	110	ns
t_r	Turn−On Rise Time		–	95	200	ns
$t_{d(off)}$	Turn-Off Delay Time		–	122	254	ns
t_f	Turn−Off Fall Time		–	80	170	ns
Q_g	Total Gate Charge	V_{DS} = 800 V, I_D = 8.0 A, V_{GS} = 10 V (Note 4)	–	53	70	nC
Q_{gs}	Gate−Source Charge		–	13	–	nC
Q_{gd}	Gate−Drain Charge		–	23	–	nC
DRAIN-SOURCE DIODE CHARACTERISTICS AND MAXIMUM RATINGS						
I_S	Maximum Continuous Source−Drain Diode Forward Current		–	–	8.0	A
I_{SM}	Maximum Pulsed Drain−Source Diode Forward Current		–	–	32.0	A
V_{SD}	Drain−Source Diode Forward Voltage	V_{GS} = 0 V, I_S = 8.0 A	–	–	1.4	V
t_{rr}	Reverse Recovery Time	V_{GS} = 0 V, I_S = 8.0 A, dI_F/dt = 100 A/μs	–	620	–	ns
Q_{rr}	Reverse Recovery Charge		–	5.2	–	μC

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

4. Essentially independent of operating temperature.

TYPICAL PERFORMANCE CHARACTERISTICS

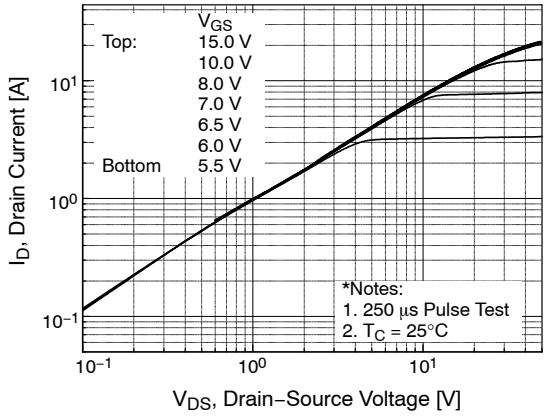


Figure 1. On−Region Characteristics

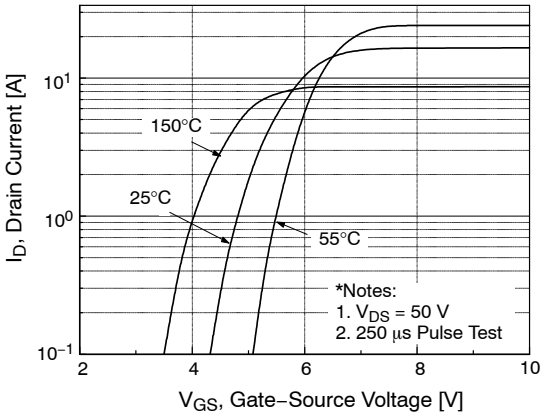


Figure 2. Transfer Characteristics

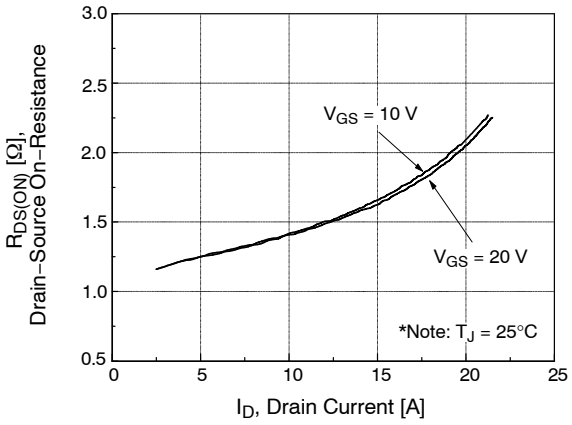


Figure 3. On−Resistance Variation vs. Drain Current and Gate Voltage

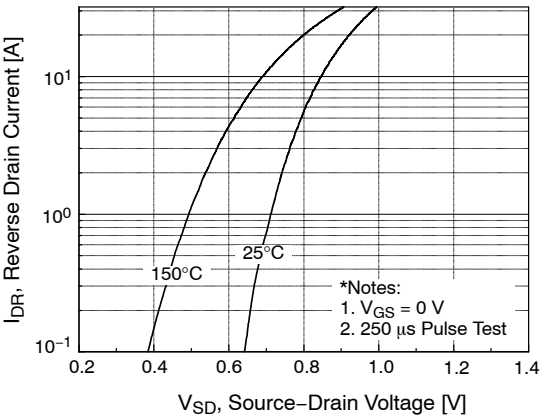


Figure 4. Body Diode Forward Voltage Variation vs. Source Current and Temperature

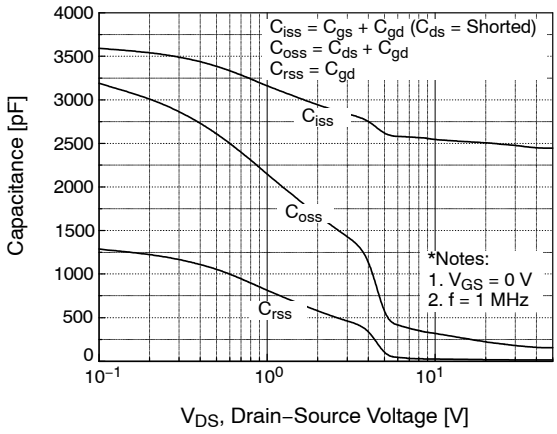


Figure 5. Capacitance Characteristics

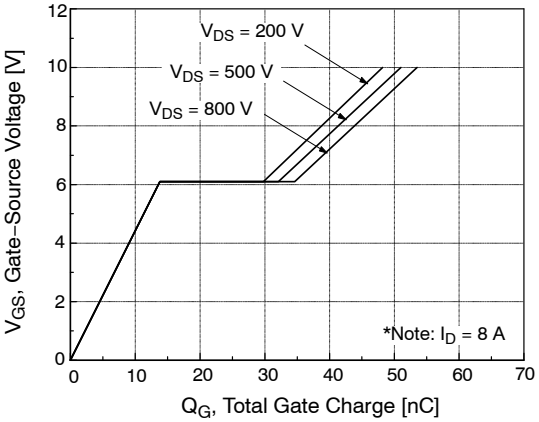


Figure 6. Gate Charge Characteristics

TYPICAL PERFORMANCE CHARACTERISTICS (continued)

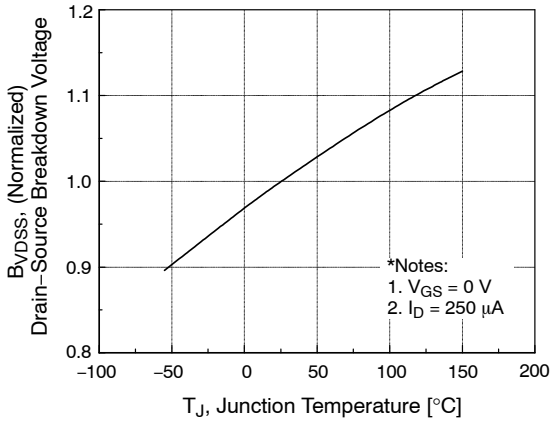


Figure 7. Breakdown Voltage Variation vs. Temperature

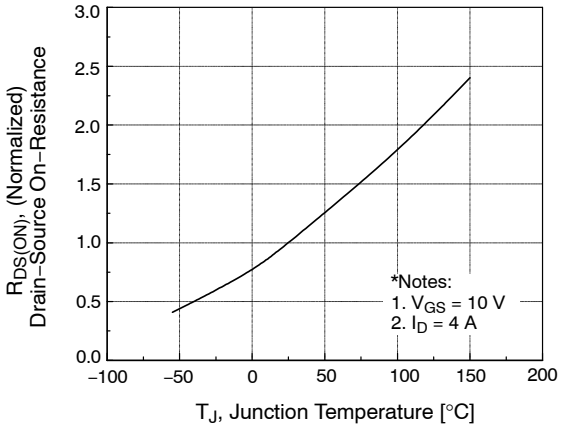


Figure 8. On−Resistance Variation vs. Temperature

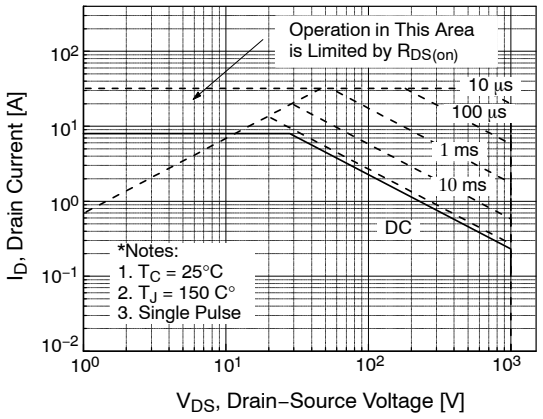


Figure 9. Maximum Safe Operating Area

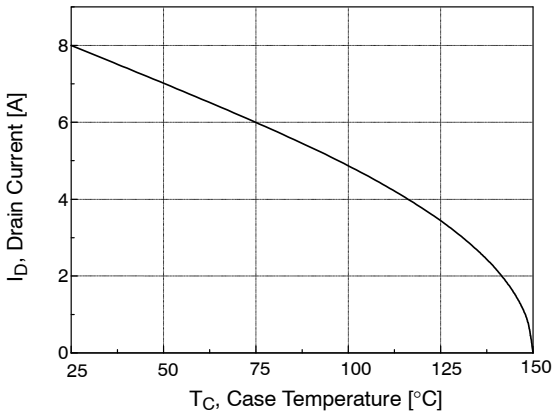


Figure 10. Maximum Drain Current vs. Case Temperature

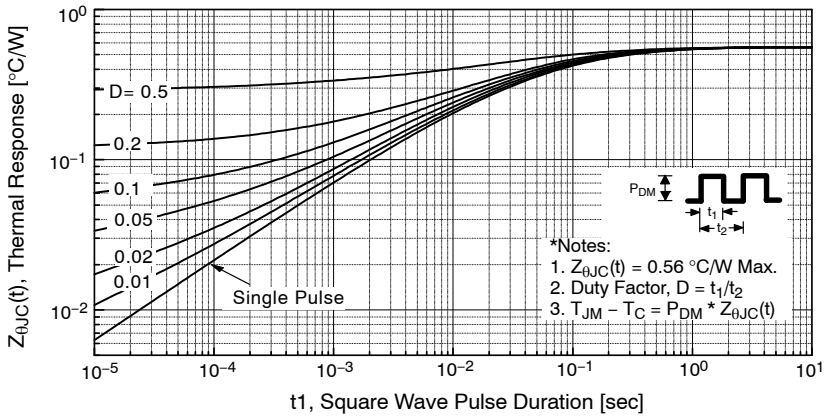


Figure 11. Transient Thermal Response Curve

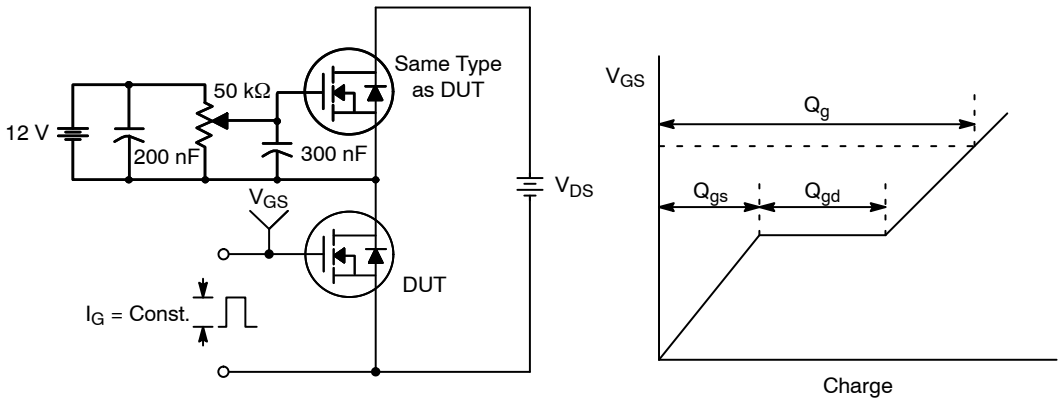


Figure 12. Gate Charge Test Circuit & Waveform

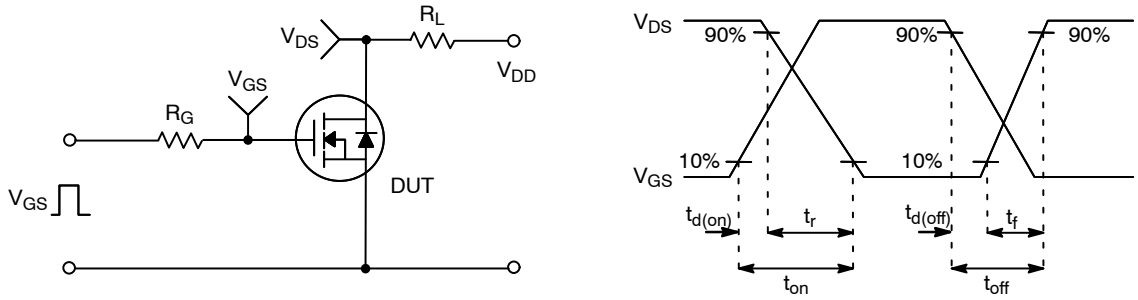


Figure 13. Resistive Switching Test Circuit & Waveforms

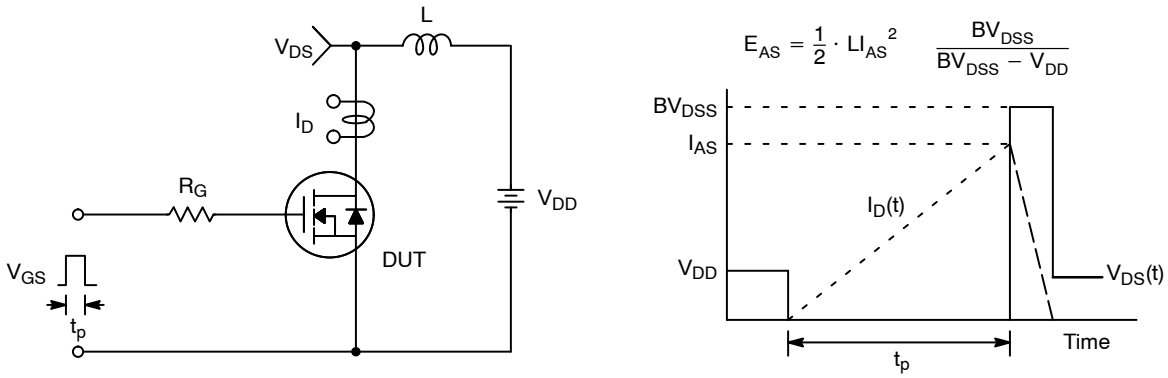


Figure 14. Unclamped Inductive Switching Test Circuit & Waveforms

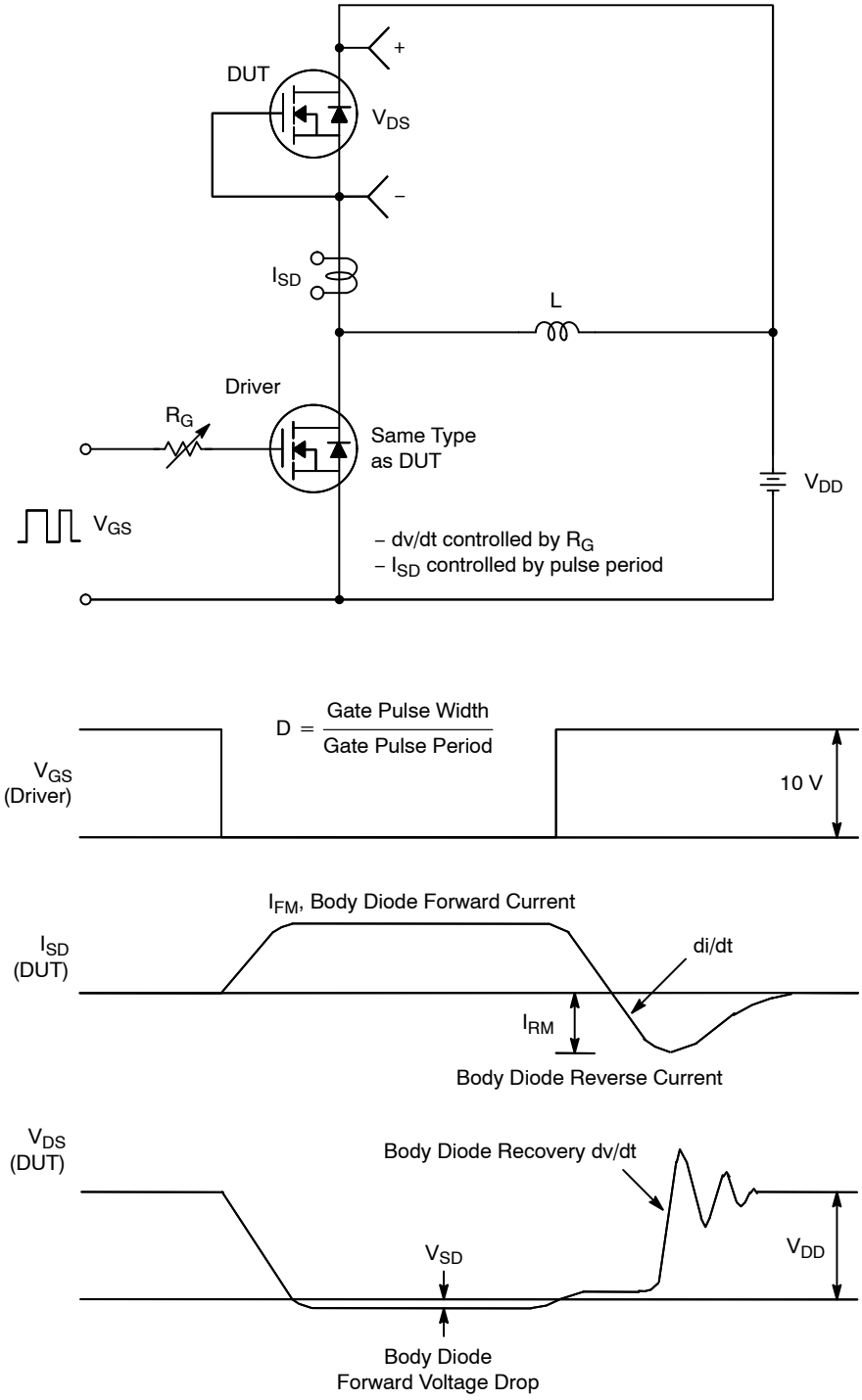
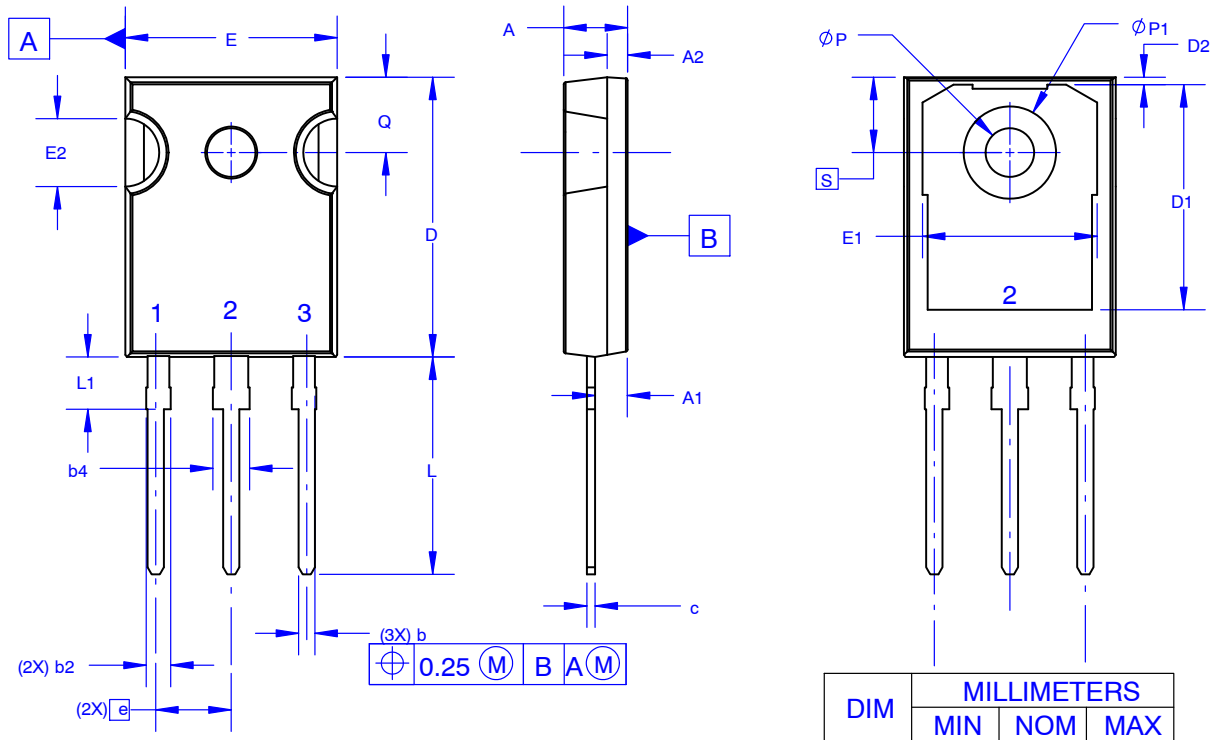


Figure 15. Peak Diode Recovery dv/dt Test Circuit & Waveforms

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CASE 340CK
ISSUE A

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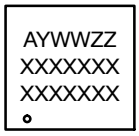


DIM	MILLIMETERS		
	MIN	NOM	MAX
A	4.58	4.70	4.82
A1	2.20	2.40	2.60
A2	1.40	1.50	1.60
b	1.17	1.26	1.35
b2	1.53	1.65	1.77
b4	2.42	2.54	2.66
c	0.51	0.61	0.71
D	20.32	20.57	20.82
D1	13.08	~	~
D2	0.51	0.93	1.35
E	15.37	15.62	15.87
E1	12.81	~	~
E2	4.96	5.08	5.20
e	~	5.56	~
L	15.75	16.00	16.25
L1	3.69	3.81	3.93
ØP	3.51	3.58	3.65
ØP1	6.60	6.80	7.00
Q	5.34	5.46	5.58
S	5.34	5.46	5.58

NOTES: UNLESS OTHERWISE SPECIFIED.

A. DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLD FLASH, AND TIE BAR EXTRUSIONS.
B. ALL DIMENSIONS ARE IN MILLIMETERS.
C. DRAWING CONFORMS TO ASME Y14.5 - 2009.
D. DIMENSION A1 TO BE MEASURED IN THE REGION DEFINED BY L1.
E. LEAD FINISH IS UNCONTROLLED IN THE REGION DEFINED BY L1.

GENERIC MARKING DIAGRAM*



XXXX = Specific Device Code
A = Assembly Location
Y = Year
WW = Work Week
ZZ = Assembly Lot Code

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, “G” or microdot “▪”, may or may not be present. Some products may not follow the Generic Marking.

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