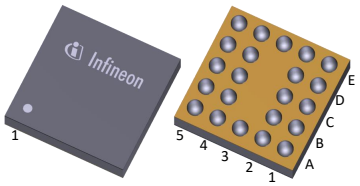
CoolGaN™

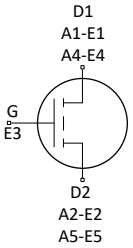
CoolGaN™ BDS 40 V

SG-UFWLB-22



Features

- E-mode bidirectional transistor - normally OFF switch
- Drain-to-Drain configuration
- Bidirectional blocking capability
- Low on-resistance, low gate charge, low output charge
- Qualified according to JEDEC for target applications
- Space saving chip scale packaging with topside protective coating



Potential applications

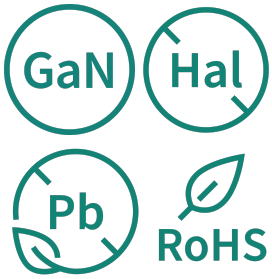
- High side load switch
- OVP protection in smart phone USB port
- Switch circuits in multiple power supply system

Product validation

Qualified according to relevant JEDEC tests.

Table 1 Key performance parameters

Parameter	Value	Unit
V_{DD}	40	V
$R_{DD(on)}$	4.2	mΩ
I_D	53	A
Q_{oss}	7.1	nC
Q_G	9.1	nC



Part number	Package	Marking	Related links
IGK048B041S	SG-UFWLB-22	48BF1	see Appendix A

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1 Maximum ratings

at T_j = 25 °C, unless otherwise specified. Stresses beyond max ratings may cause permanent damage to the device. For optimum lifetime and reliability, Infineon recommends operating conditions that do not continuously exceed 80 % of the maximum ratings stated (unless otherwise explicitly stated). For further information, contact your local Infineon sales office.

Table 2 Maximum ratings

Parameter	Symbol	Values			Unit	Note / Test condition
		Min.	Typ.	Max.		
Continuous drain-drain voltage	V_{DD}	-	-	40	V	V_{GD}=0 V
Pulsed drain-drain voltage [1]	$V_{DD,\ pulse}$	-	-	48	V	V_{GD}=0 V, 1 h total time
Continuous drain current	I_D	-	-	53	A	V_{GD}=5 V, T_C=25 °C
Pulsed drain current [2]	$I_{D,pulse}$	-	-	120	A	T_j=125 °C
Gate-drain voltage [1]	V_{GD}	-40	-	6.0	V	-
Power dissipation	P_{tot}	-	-	25	W	T_C=25 °C
				1.7		T_A=25 °C, R_{thJA}=59 °C/W [3]
Storage temperature	T_{stg}	-40	-	150	°C	-
Junction temperature	T_j			125		

[1] Provided as measure of robustness under abnormal operating conditions and not recommended for normal operation.

[2] Pulse current limited by transfer characteristic.

[3] Device on 1-layer FR4 PCB, vertical in still air.

2 Recommended operating conditions

Table 3 Recommended operating conditions

Parameter	Symbol	Values			Unit	Note / Test condition
		Min.	Typ.	Max.		
Gate-drain voltage	V_{GD}	-32	5.0	5.5	V	-

3 Thermal characteristics

Table 4 Thermal characteristics

Parameter	Symbol	Values			Unit	Note / Test condition
		Min.	Typ.	Max.		
Thermal resistance, junction - case, top	R_{thJC}	-	17	20	°C/W	-
Thermal resistance, junction - case, bottom			3.3	4.0		
Thermal resistance, junction - ambient 1s0p	R_{thJA}	-	59	-	°C/W	On 1 layer PCB, vertical in still air.

4 Electrical Characteristics

at T_j=25 °C, unless otherwise specified

Table 5 Static characteristics

Parameter	Symbol	Values			Unit	Note / Test condition
		Min.	Typ.	Max.		
Gate threshold voltage	$V_{GD(th)}$	1.2	2.0	2.9	V	V_{DD}=V_{GD}, I_D=3.0 mA
Drain-drain leakage current	I_{DDS}	-	0.05	3.0	µA	V_{DD}=40 V, V_{GD}=0 V, T_j=25 °C
Gate-drain leakage current	I_{GDS}	-	3.2	10.6	µA	V_{GD}=5 V, T_j=25 °C
			0.01	0.1		V_{GD}=-4 V, T_j=25 °C
			9.4	32		V_{GD}=5 V, T_j=85 °C
			0.01	0.1		V_{GD}=-4 V, T_j=85 °C
Drain-drain on-state resistance	$R_{DD(on)}$	-	4.2	4.8	mΩ	V_{GD}=5 V, I_D=5 A
Gate resistance [4)]	R_G	-	0.5	-	Ω	-

4) Defined by design. Not subject to production test.

Table 6 Capacitance characteristics [5)]

Parameter	Symbol	Values			Unit	Note / Test condition
		Min.	Typ.	Max.		
Input capacitance	C_{iss}	-	600	-	pF	V_{GD}=0 V, V_{DD}=20 V, f=1 MHz
Output capacitance	C_{oss}		212			
Reverse transfer capacitance	C_{rss}		127			

5) Defined by design. Not subject to production test.

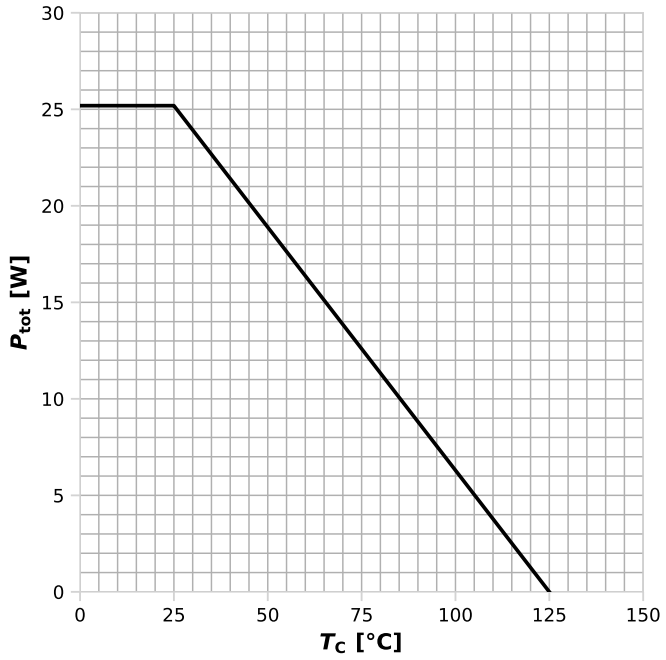
Table 7 Gate charge characteristics [6)]

Parameter	Symbol	Values			Unit	Note / Test condition
		Min.	Typ.	Max.		
Gate charge at threshold	$Q_{g(th)}$	-	1.5	-	nC	V_{DD}=20 V, I_D=5 A, V_{GD}=0 to 5 V
Gate to drain charge	Q_{gd}		5.0		nC	
Gate charge total	Q_g		9.1		nC	
Gate plateau voltage	$V_{plateau}$		2.7		V	
Output charge	Q_{oss}	-	7.1	-	nC	V_{DD}=20 V, V_{GD}=0 V

6) Defined by design. Not subject to production test.

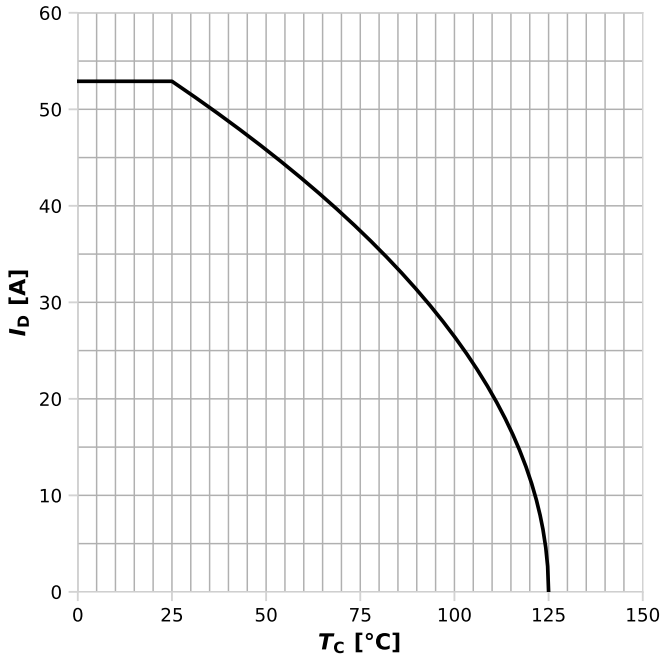
5 Electrical characteristics diagrams

Diagram 1: Power dissipation



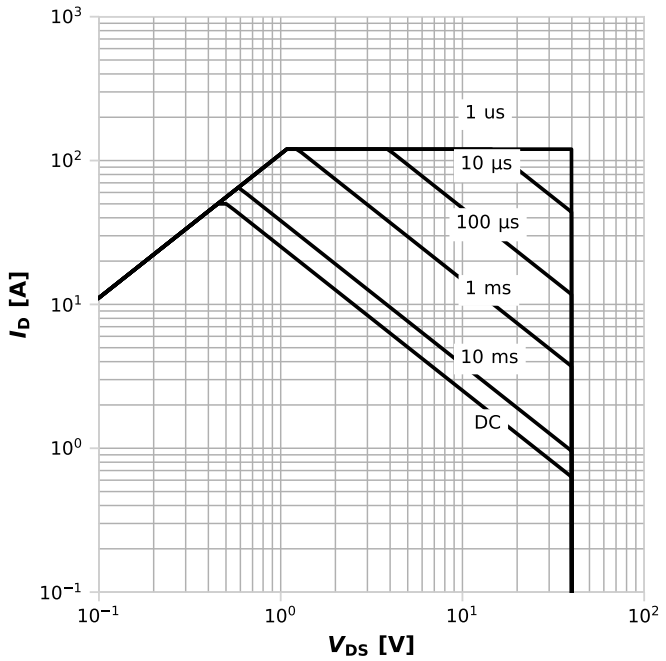
P_{tot}=f(T_C)

Diagram 2: Drain Current



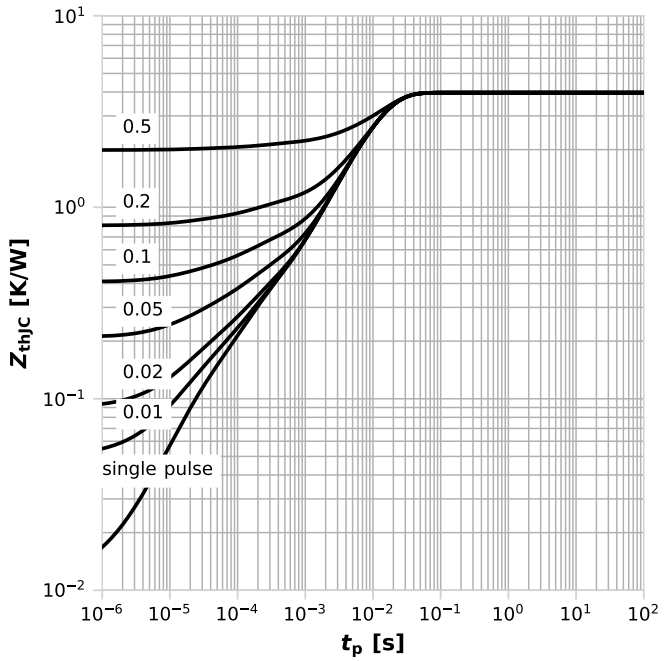
I_D=f(T_C)

Diagram 3: Safe operating area



I_D=f(V_{DS}); T_C=25 °C; D=0; parameter: t_p

Diagram 4: Max. transient thermal impedance



Z_{thJC} =f(t_P); parameter: D=t_p/T

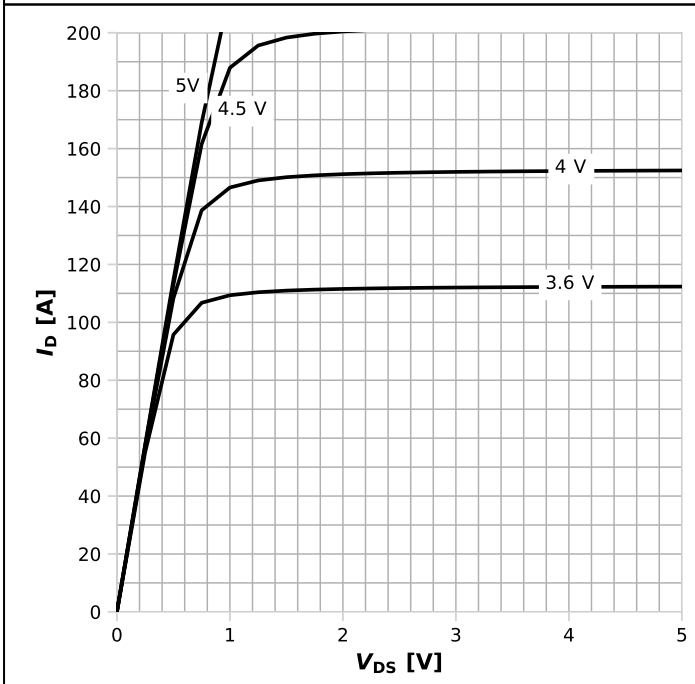
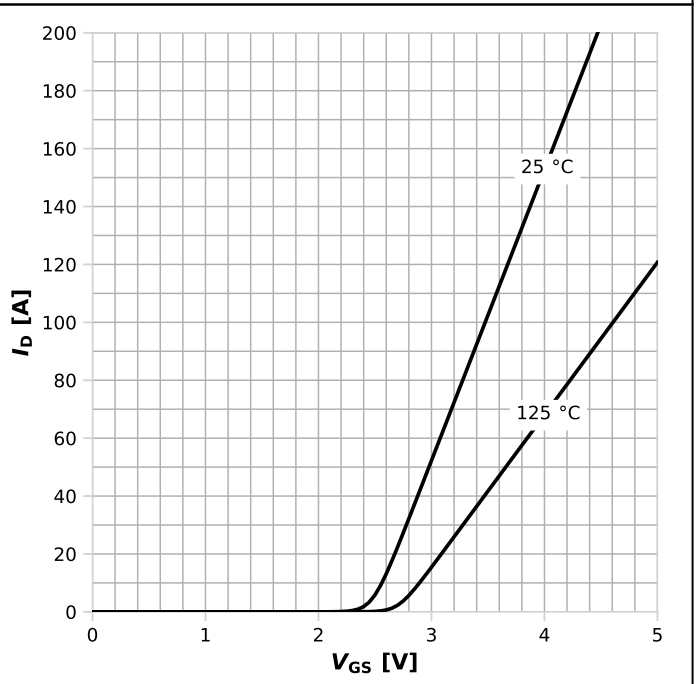
Diagram 5: Typ. output characteristics	Diagram 6: Typ. transfer characteristics
	
I_D=f(V_{DS}); T_j=25 °C; parameter: V_{GS}	I_D=f(V_{GS}); |V_{DS}|>2|I_D|$R_{DS(on)max}$; parameter: T_j

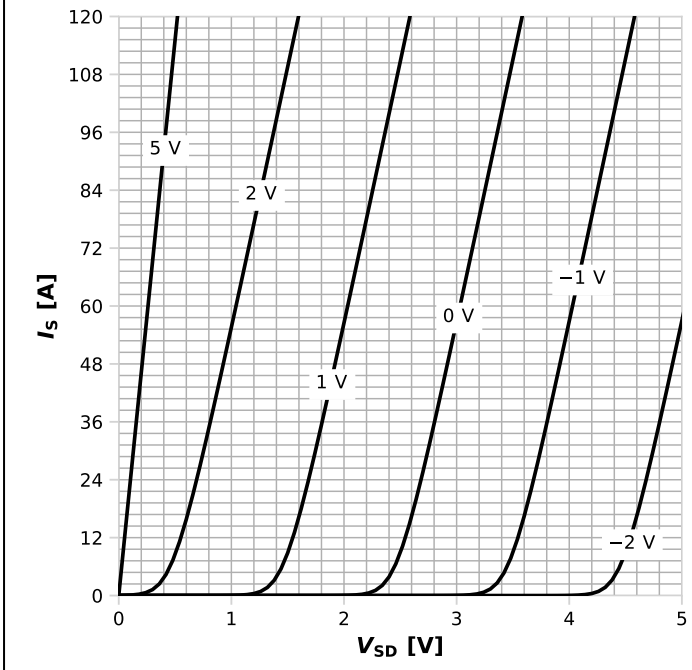
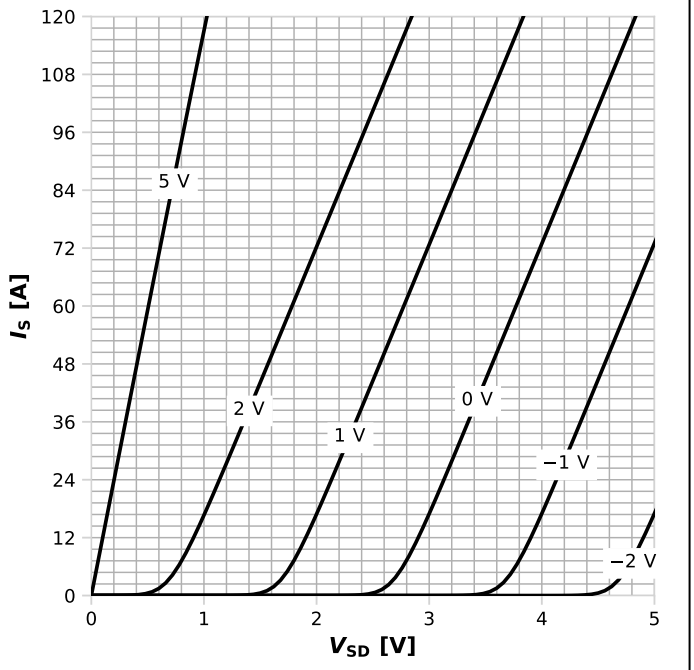
Diagram 7: Typ. channel reverse characteristics	Diagram 8: Typ. channel reverse characteristics
	
I_S=f(V_{SD}); T_j=25 °C; parameter: V_{GS}	I_S=f(V_{SD}); T_j=125 °C; parameter: V_{GS}

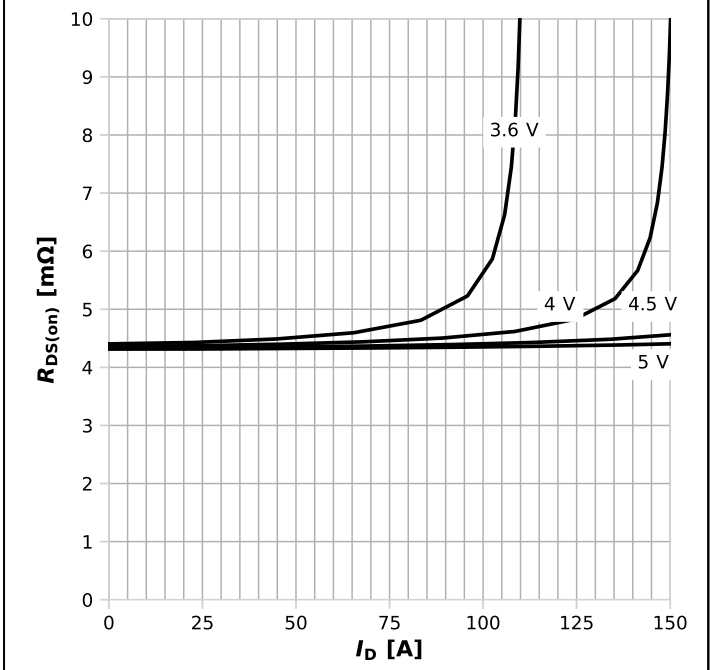
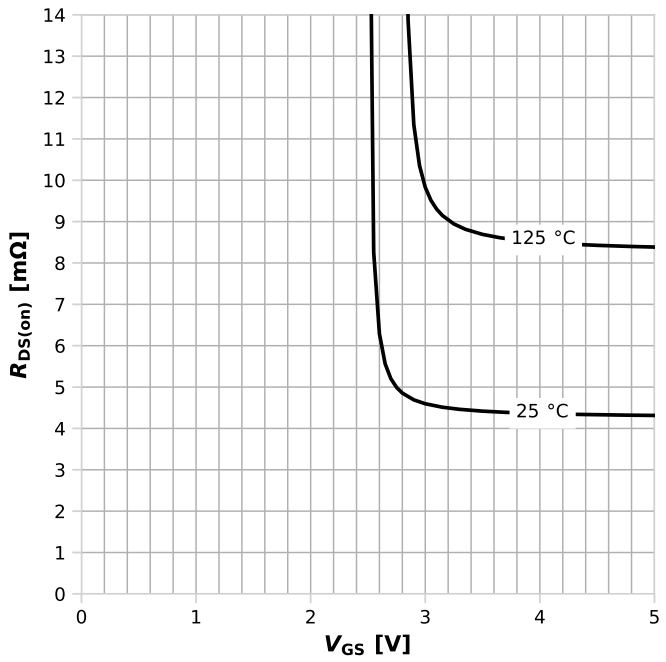
Diagram 9: Typ. drain-source on-state resistance	Diagram 10: Typ. Drain-source on-state resistance
	
$R_{DS(on)}$=f(I_D); T_j=25 °C; parameter: V_{GS}	$R_{DS(on)}$=f(V_{GS}); I_D=5 A; parameter: T_j

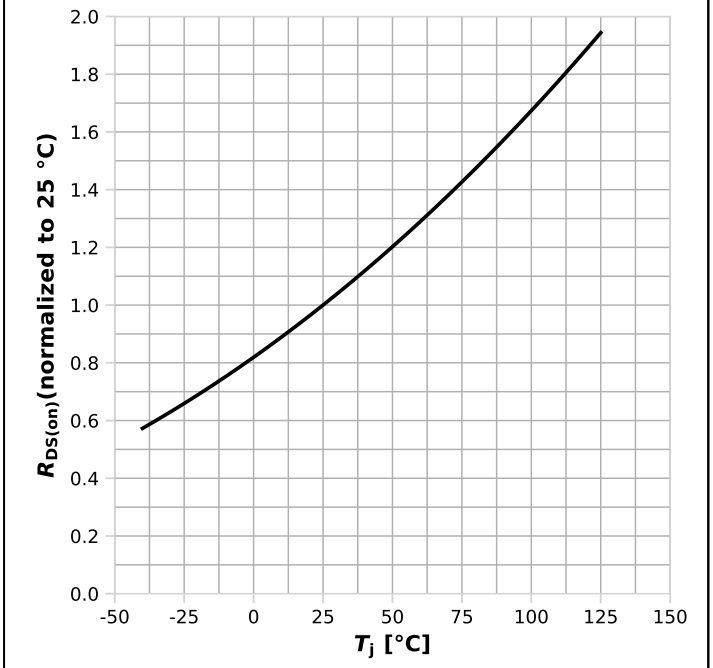
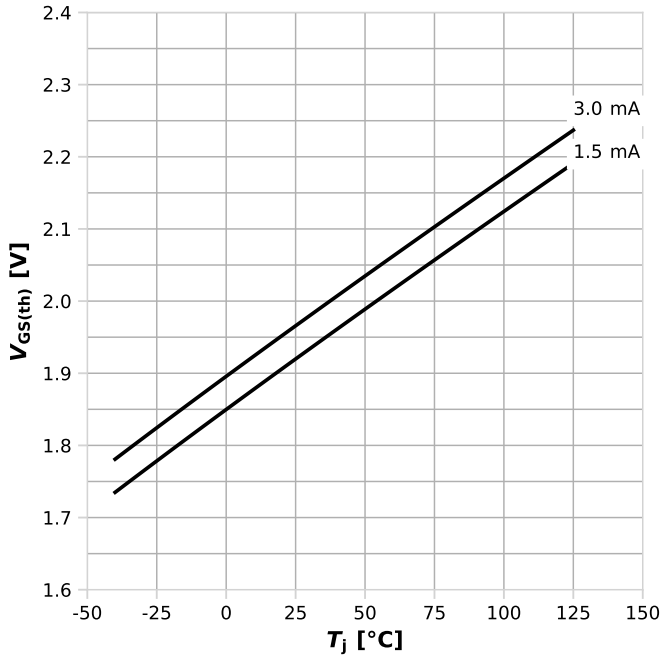
Diagram 11: Drain-source on-state resistance	Diagram 12: Typ. gate threshold voltage
	
$R_{DS(on)}$=f(T_j); I_D=5 A, V_{GS}=5V	$V_{GS(th}$=f(T_j), V_{GS}=V_{DS}; parameter: I_D

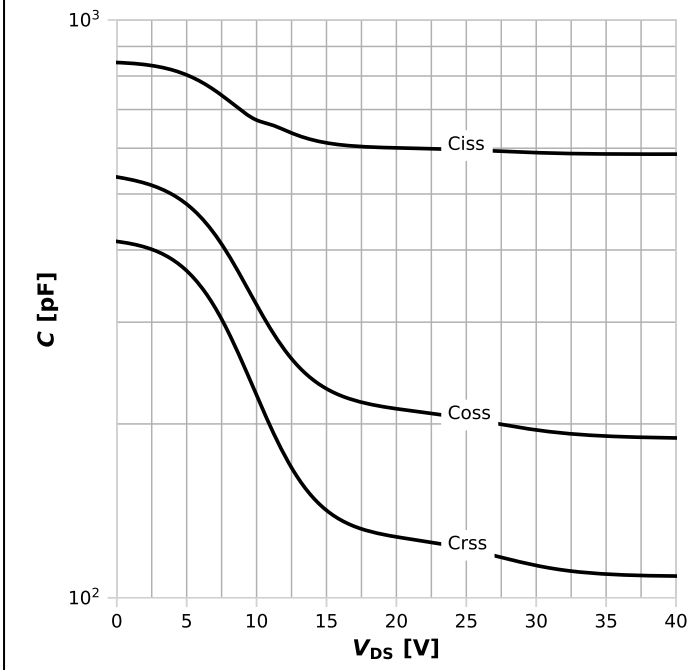
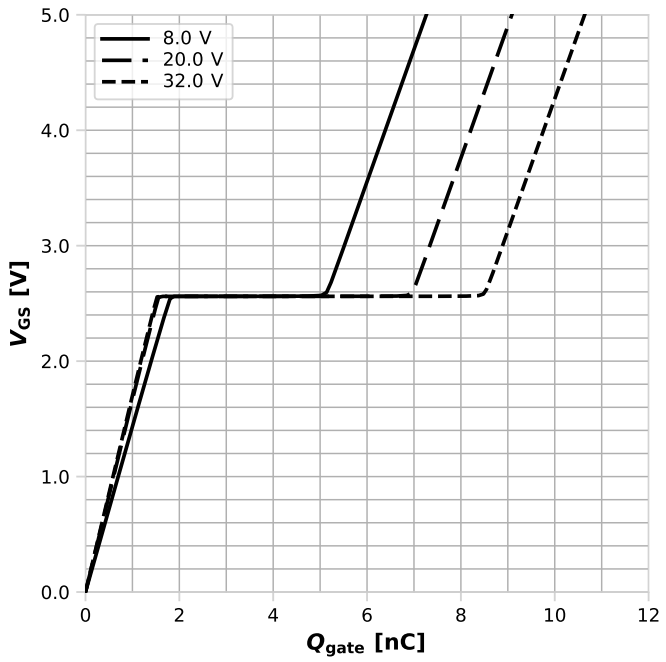
Diagram 13: Typ. capacitances	Diagram 14 Typ. gate charge
	
C=f(V_{DS}); V_{GS}=0 V	V_{GS}=f(Q_{gate}); I_D=5 A pulsed; parameter: V_{DS}

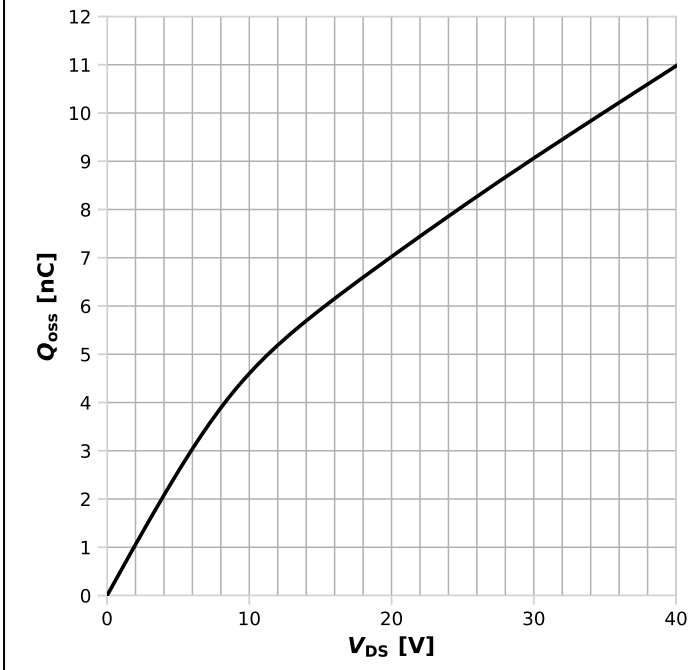
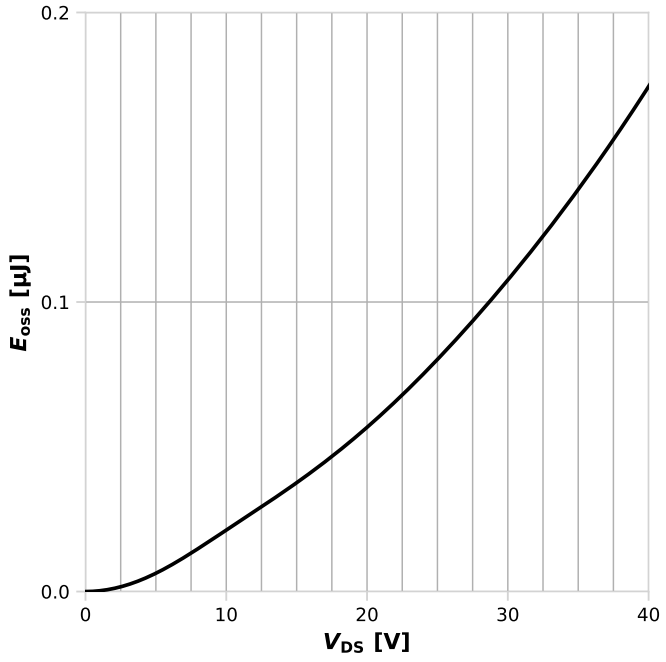
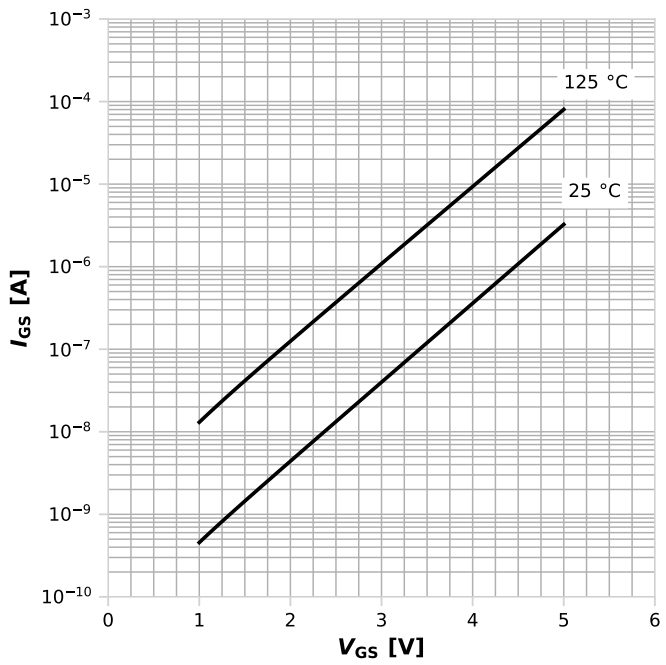
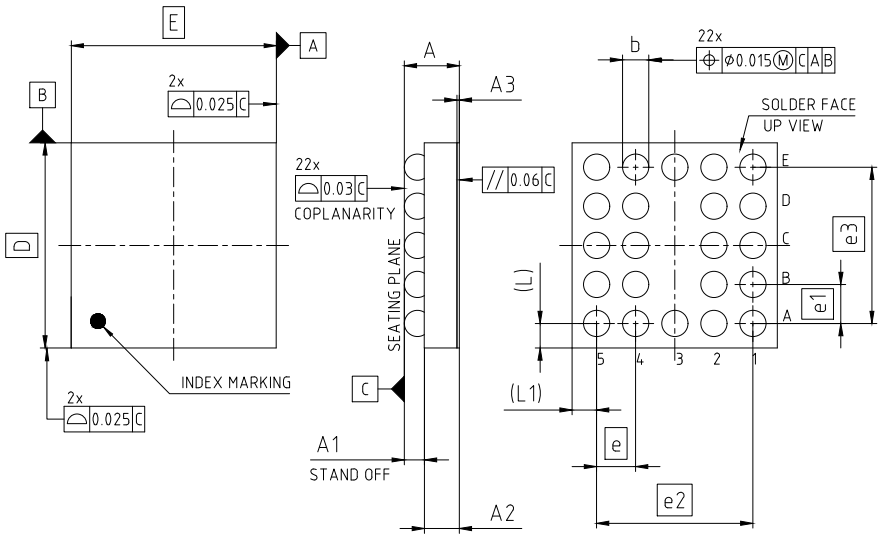
Diagram 15: Typ. output charge	Diagram 16: Typ. Coss stored Energy
	
Q_{oss}=f(V_{DS}), V_{GS}=0 V	E_{oss}=f(V_{DS}), V_{GS}=0 V

Diagram 17: Typ. gate characteristics forward



I_{GS}=f(V_{GS}); V_{DS}=0 V; parameter: T_j

6 Package outlines



PACKAGE - GROUP NUMBER:	SG-UFWLB-22-U01	
DIMENSIONS	MILLIMETERS	
	MIN.	MAX.
A	0.531	0.597
A1	0.175	0.235
A2	0.346	0.374
A3	0.022	0.028
b	0.241	0.295
D	2.10	
E	2.10	
e	0.40	
e1	0.40	
e2	1.60	
e3	1.60	
L	0.25	
L1	0.25	

Figure 1 Outline SG-UFWLB-22, dimensions in mm

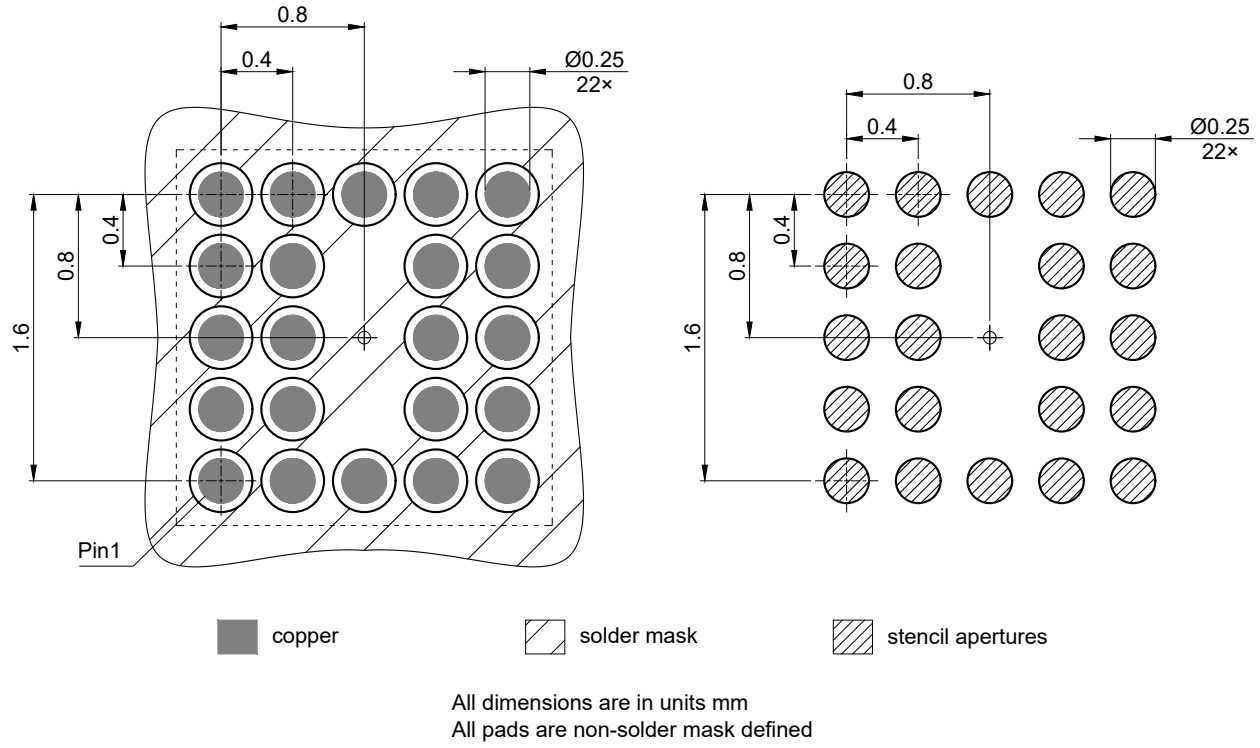


Figure 2 Footprint drawing SG-UFWLB-22, dimensions in mm

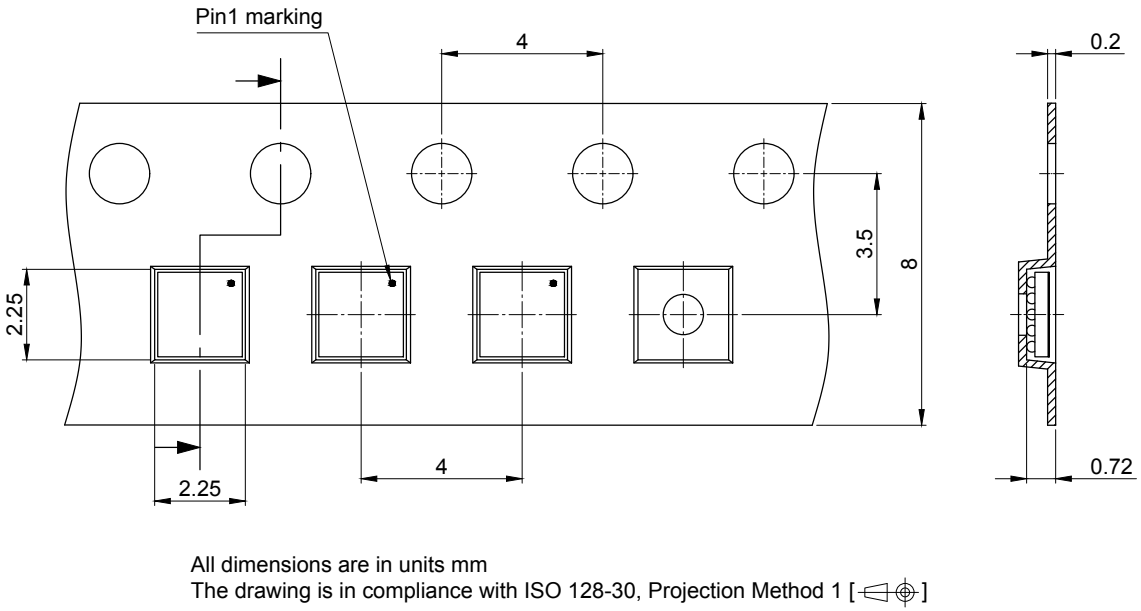


Figure 3 Packaging variant SG-UFWLB-22, dimensions in mm

7 Appendix A

Table 8 Related links

- IFX CoolGaN™ GaN webpage
- IFX CoolGaN™ reliability white paper
- IFX Packages Description-SG-UFWLB-22-1

Revision history

IGK048B041S

Revision 2026-01-07, Rev. 1.0

Previous revisions

Revision	Date	Subjects (major changes since last revision)
1.0	2026-01-07	Release of final version

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