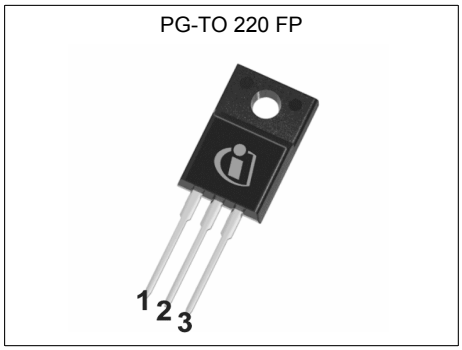
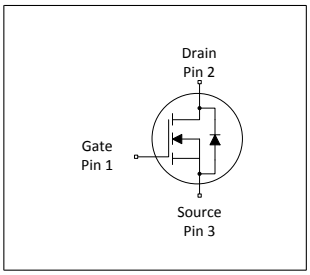
MOSFET

500V CoolMOS™ CE Power Transistor

PG-TO 220 FP



CoolMOS™ is a revolutionary technology for high voltage power MOSFETs, designed according to the superjunction (SJ) principle and pioneered by Infineon Technologies. CoolMOS™ CE is a price-performance optimized platform enabling to target cost sensitive applications in Consumer and Lighting markets by still meeting highest efficiency standards. The new series provides all benefits of a fast switching Superjunction MOSFET while not sacrificing ease of use and offering the best cost down performance ratio available on the market.



Features

- Extremely low losses due to very low FOM Rdson*Qg and Eoss
- Very high commutation ruggedness
- Easy to use/drive
- Pb-free plating, Halogen free mold compound
- Qualified for standard grade applications

Applications

PFC stages, hard switching PWM stages and resonant switching stages for e.g. PC Silverbox, Adapter, LCD & PDP TV and indoor lighting.

Please note: For MOSFET paralleling the use of ferrite beads on the gate or separate totem poles is generally recommended.

Table 1 Key Performance Parameters

Parameter	Value	Unit
V_{DS} @ $T_{j,max}$	550	V
$R_{DS(on),max}$	0.8	Ω
I_D	7.6	A
$Q_{g,typ}$	12.4	nC
$I_{D,pulse}$	15.5	A
E_{oss} @ 400V	1.46	µJ

Type / Ordering Code	Package	Marking	Related Links
IPA50R800CE	PG-TO 220 FullPAK	5R800CE	see Appendix A

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1 Maximum ratings

at T_j = 25°C, unless otherwise specified

Table 2 Maximum ratings

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Continuous drain current[1)]	I_D	- -	- -	7.6 4.8	A	T_C = 25°C T_C = 100°C
Pulsed drain current[2)]	$I_{D,pulse}$	-	-	15.5	A	T_C=25°C
Avalanche energy, single pulse	E_{AS}	-	-	83	mJ	I_D =1.9A; V_{DD} = 50V
Avalanche energy, repetitive	E_{AR}	-	-	0.13	mJ	I_D =1.9A; V_{DD} = 50V
Avalanche current, repetitive	I_{AR}	-	-	1.9	A	-
MOSFET dv/dt ruggedness	dv/dt	-	-	50	V/ns	V_{DS} =0...400V
Gate source voltage	V_{GS}	-20 -30	- -	20 30	V	static; AC (f>1 Hz)
Power disspiation (Full PAK)	P_{tot}	-	-	26.4	W	T_C=25°C
Operating and storage temperature	T_j, T_{stg}	-40	-	150	°C	-
Mounting torque	-	-	-	50	Ncm	M2.5 screws
Continuous diode forward current	I_S	-	-	3.6	A	T_C=25°C
Diode pulse current[2)]	$I_{S,pulse}$	-	-	15.5	A	T_C = 25°C
Reverse diode dv/dt[3)]	dv/dt	-	-	15	V/ns	V_{DS} =0...400V, I_{SD}<=I_S, T_j=25°C
Maximum diode commutation speed[3)]	di_f/dt	-	-	500	A/µs	V_{DS} =0...400V, I_{SD}<=I_S, T_j=25°C
Insulation withstand voltage for TO-220 FullPAK	V_{ISO}	-	-	2500	V	V_{rms}, T_C=25°C, t=1min

2 Thermal characteristics

Table 3 Thermal characteristics TO220 Full PAK

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Thermal resistance, junction - case	R_{thJC}	-	-	4.73	°C/W	-
Thermal resistance, junction - ambient	R_{thJA}	-	-	80	°C/W	leaded
Soldering temperature, wavesoldering only allowed at leads	T_{sold}	-	-	260	°C	1.6mm (0.063 in.) from case for 10s

[1)] Limited by $T_{j\,max}$ <150°C, Maximum Duty Cycle D = 0.5, TO220 equivalent
[2)] Pulse width t_p limited by $T_{j,max}$
[3)] V_{DClink}=400V; $V_{DS,peak}$<$V_{(BR)DSS}$; identical low side and high side switch with identical R_G

3 Electrical characteristics

Table 4 Static characteristics

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Drain-source breakdown voltage	$V_{(BR)DSS}$	500	-	-	V	V_{GS}=0V, I_D=1mA
Gate threshold voltage	$V_{(GS)th}$	2.50	3	3.50	V	V_{DS}=V_{GS}, I_D=0.13mA
Zero gate voltage drain current	I_{DSS}	- -	- 10	1 -	µA	V_{DS}=500V, V_{GS}=0V, T_j=25°C V_{DS}=500V, V_{GS}=0V, T_j=150°C
Gate-source leakage curent	I_{GSS}	-	-	100	nA	V_{GS}=20V, V_{DS}=0V
Drain-source on-state resistance	$R_{DS(on)}$	- -	0.72 1.87	0.80 -	Ω	V_{GS}=13V, I_D=1.5A, T_j=25°C V_{GS}=13V, I_D=1.5A, T_j=150°C
Gate resistance	R_G	-	3	-	Ω	f=1 MHz, open drain

Table 5 Dynamic characteristics

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Input capacitance	C_{iss}	-	280	-	pF	V_{GS}=0V, V_{DS}=100V, f=1MHz
Output capacitance	C_{oss}	-	23	-	pF	V_{GS}=0V, V_{DS}=100V, f=1MHz
Effective output capacitance, energy related[1)]	$C_{o(er)}$	-	18	-	pF	V_{GS}=0V, V_{DS}=0...400V
Effective output capacitance, time related[2)]	$C_{o(tr)}$	-	67	-	pF	I_D=constant, V_{GS}=0V, V_{DS}=0...400V
Turn-on delay time	$t_{d(on)}$	-	6.2	-	ns	V_{DD}=400V, V_{GS}=13V, I_D=1.9A, R_G=5.3Ω
Rise time	t_r	-	5.5	-	ns	V_{DD}=400V, V_{GS}=13V, I_D=1.9A, R_G=5.3Ω
Turn-off delay time	$t_{d(off)}$	-	26	-	ns	V_{DD}=400V, V_{GS}=13V, I_D=1.9A, R_G=5.3Ω
Fall time	t_f	-	15.9	-	ns	V_{DD}=400V, V_{GS}=13V, I_D=1.9A, R_G=5.3Ω

Table 6 Gate charge characteristics

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Gate to source charge	Q_{gs}	-	1.5	-	nC	V_{DD}=400V, I_D=1.9A, V_{GS}=0 to 10V
Gate to drain charge	Q_{gd}	-	6.8	-	nC	V_{DD}=400V, I_D=1.9A, V_{GS}=0 to 10V
Gate charge total	Q_g	-	12.4	-	nC	V_{DD}=400V, I_D=1.9A, V_{GS}=0 to 10V
Gate plateau voltage	$V_{plateau}$	-	5.3	-	V	V_{DD}=400V, I_D=1.9A, V_{GS}=0 to 10V

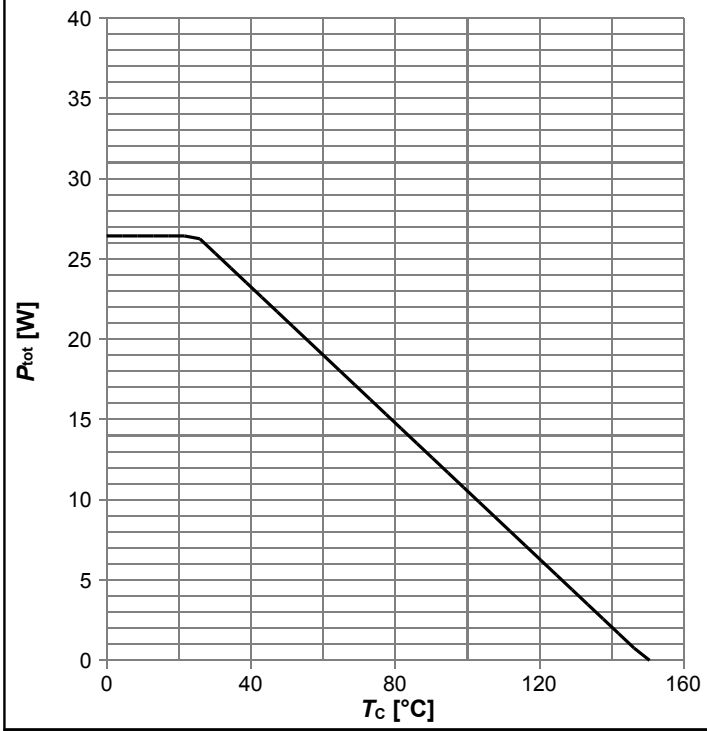
[1)] $C_{o(er)}$ is a fixed capacitance that gives the same stored energy as C_{oss} while V_{DS} is rising from 0 to 400V
[2)] $C_{o(tr)}$ is a fixed capacitance that gives the same charging time as C_{oss} while V_{DS} is rising from 0 to 400V

Table 7 Reverse diode characteristics

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Diode forward voltage	V_{SD}	-	0.83	-	V	V_{GS}=0V, I_F=1.9A, T_j=25°C
Reverse recovery time	t_{rr}	-	158	-	ns	V_R=400V, I_F=1.9A, di_F/dt=100A/µs
Reverse recovery charge	Q_{rr}	-	0.84	-	µC	V_R=400V, I_F=1.9A, di_F/dt=100A/µs
Peak reverse recovery current	I_{rrm}	-	9.6	-	A	V_R=400V, I_F=1.9A, di_F/dt=100A/µs

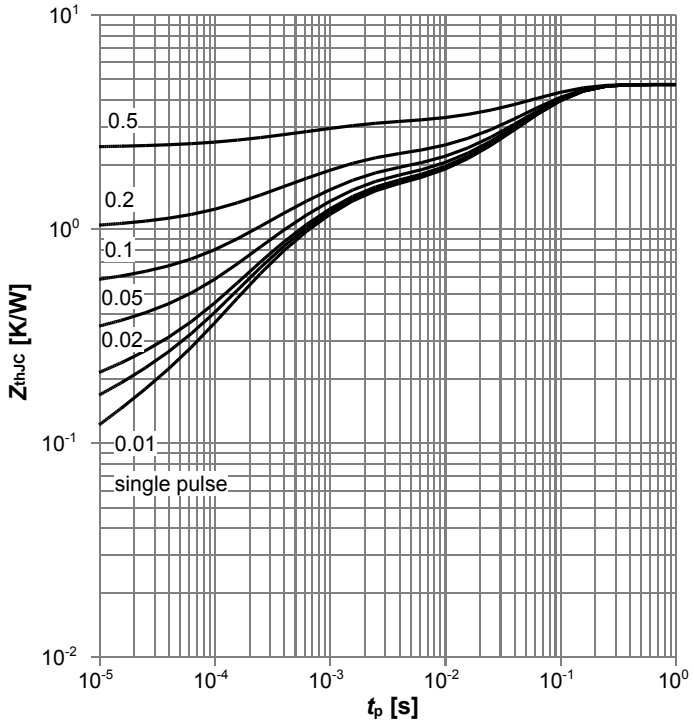
4 Electrical characteristics diagrams

Power dissipation (FullPAK)



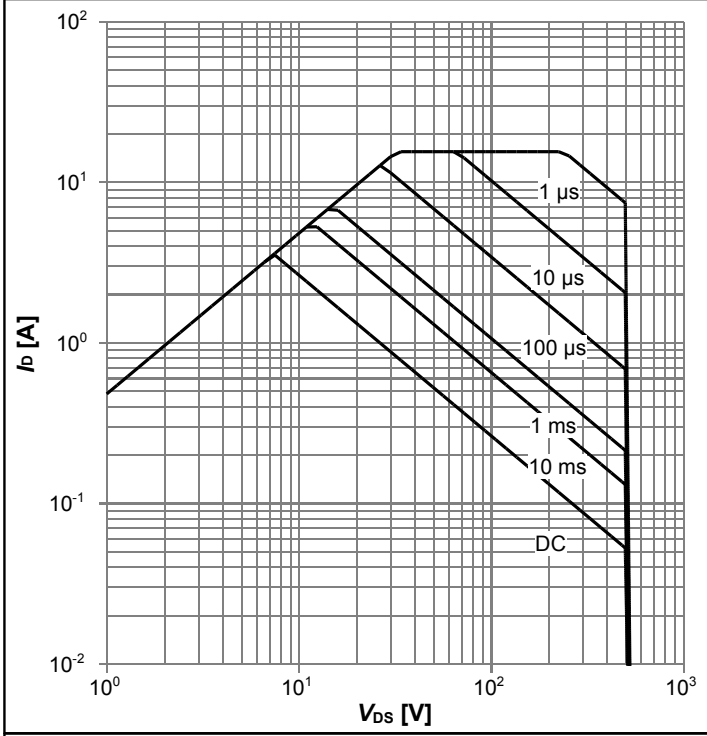
$P_{tot}=f(T_C)$

Max. transient thermal impedance (FullPAK)



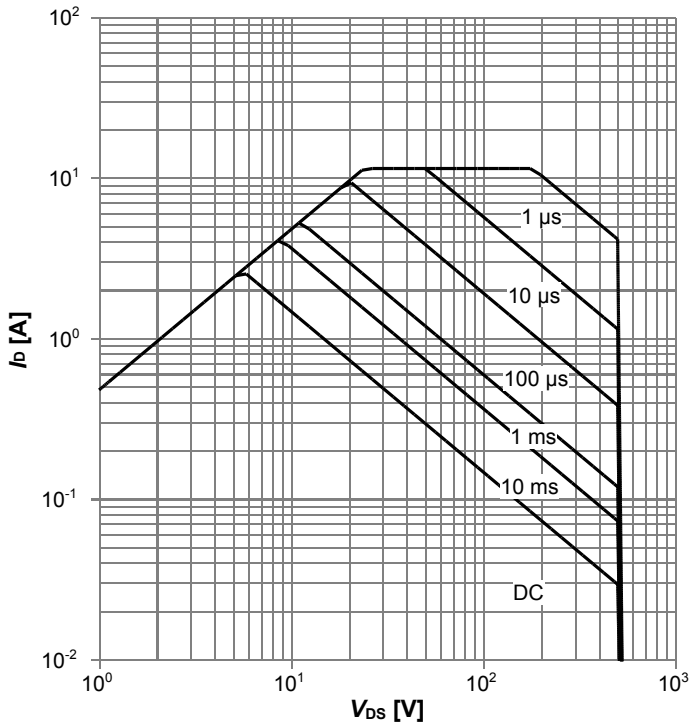
$Z_{thJC}=f(t_P)$; parameter: $D=t_p/T$

Safe operating area (FullPAK) Tj=25°C



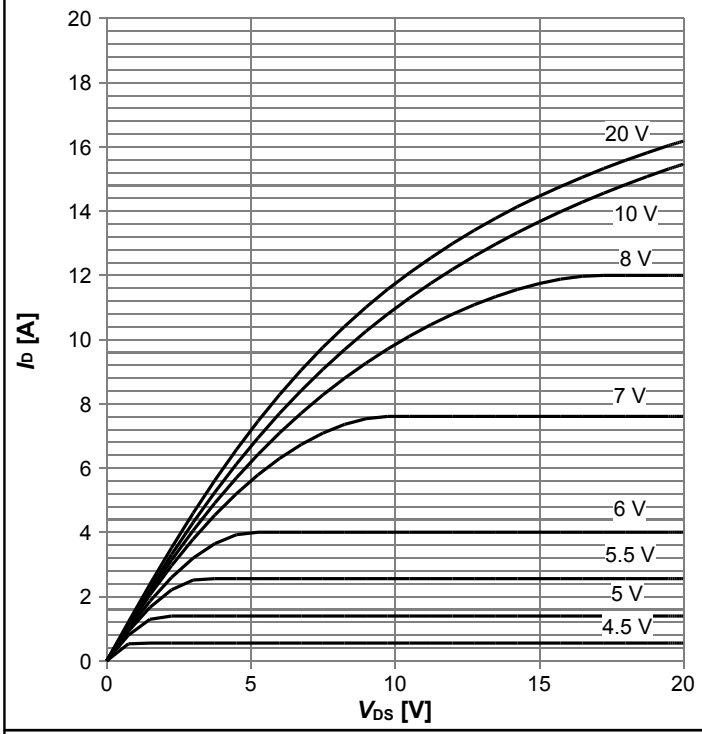
$I_D=f(V_{DS})$; $T_C=25$ °C; $D=0$; parameter: t_p

Safe operating area (FullPAK) Tj=80°C



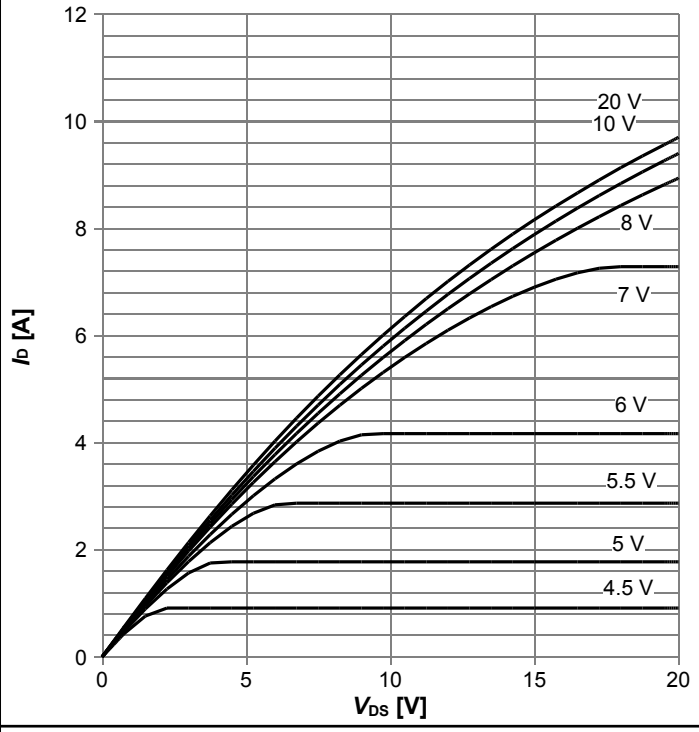
$I_D=f(V_{DS})$; $T_C=80$ °C; $D=0$; parameter: t_p

Typ. output characteristics Tj=25°C



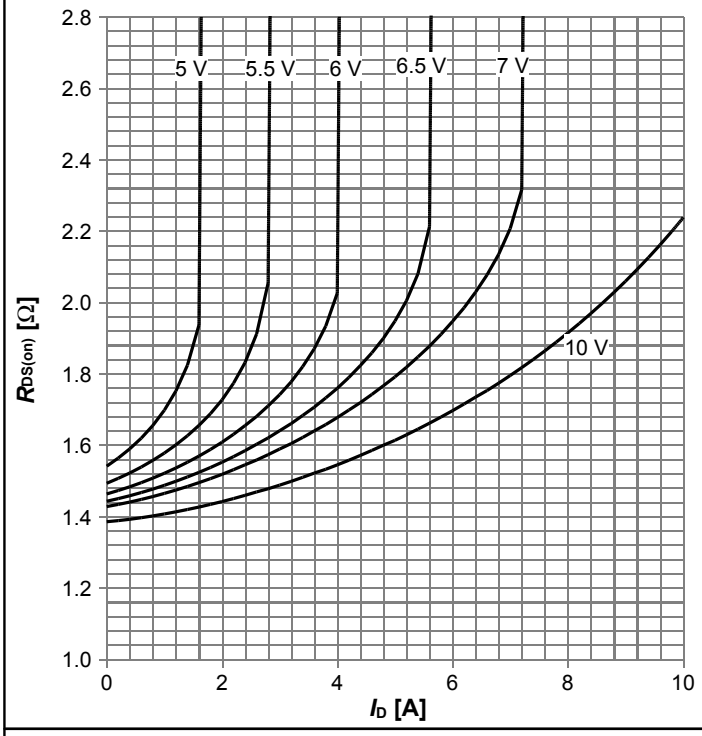
$I_D=f(V_{DS})$; $T_j=25$ °C; parameter: V_{GS}

Typ. output characteristics Tj=125°C



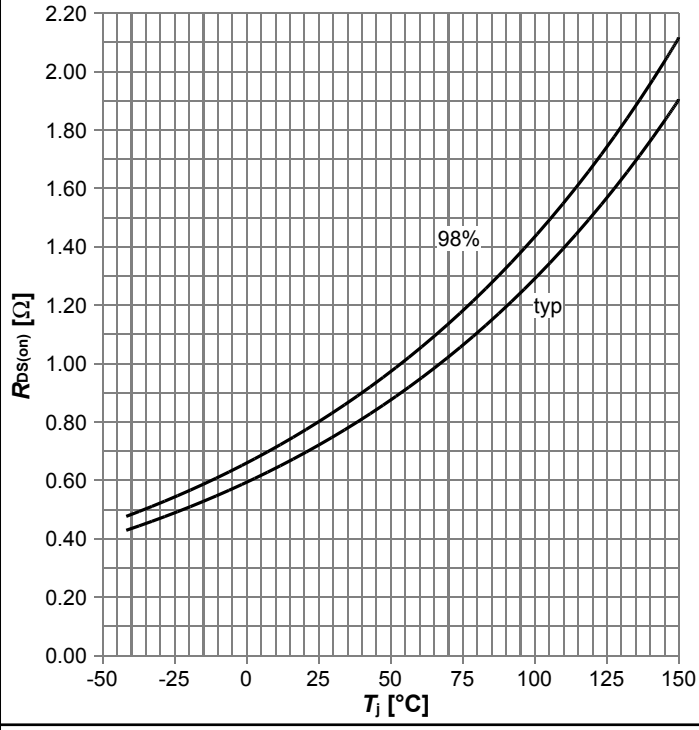
$I_D=f(V_{DS})$; $T_j=125$ °C; parameter: V_{GS}

Typ. drain-source on-state resistance



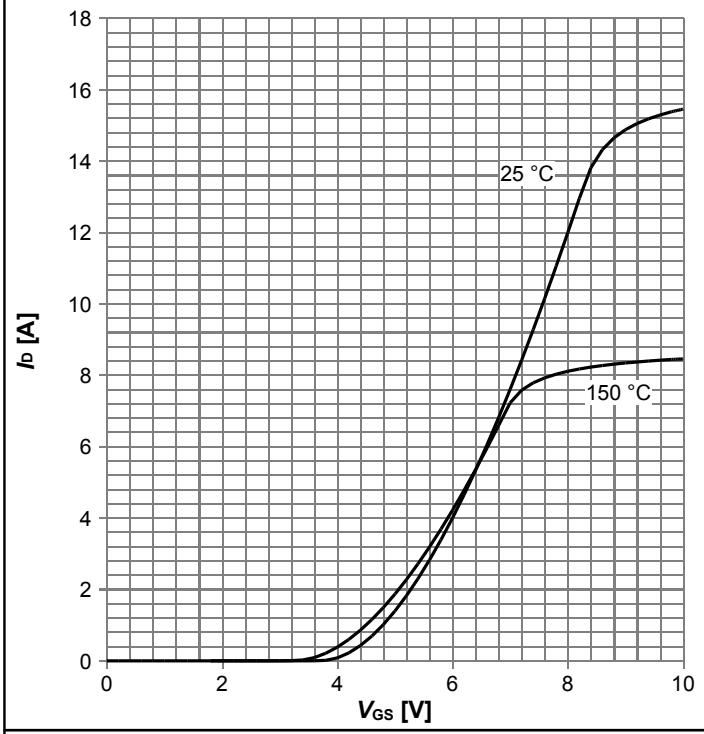
$R_{DS(on)}=f(I_D)$; $T_j=125$ °C; parameter: V_{GS}

Drain-source on-state resistance



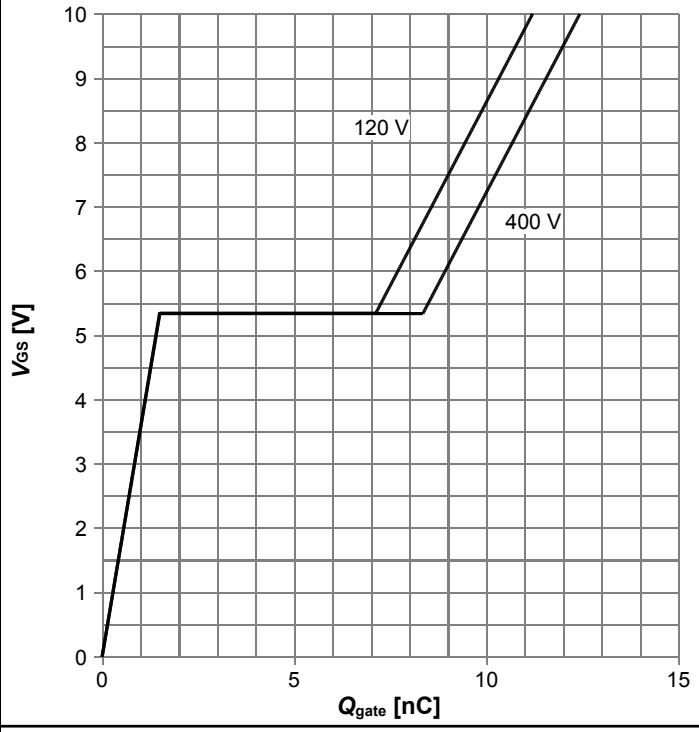
$R_{DS(on)}=f(T_j)$; $I_D=1.5$ A; $V_{GS}=13$ V

Typ. transfer characteristics



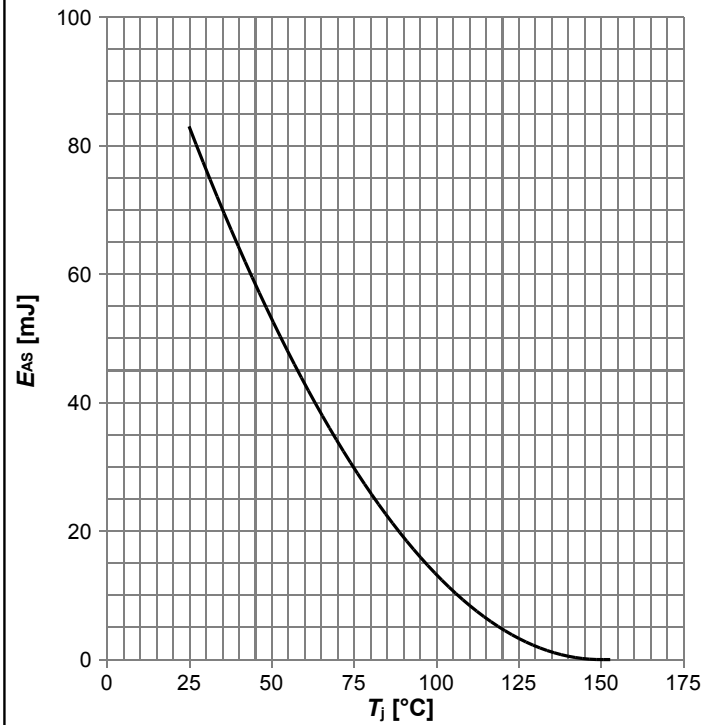
I_D=f(V_{GS});V_{DS}=20V; parameter: T_j

Typ. gate charge



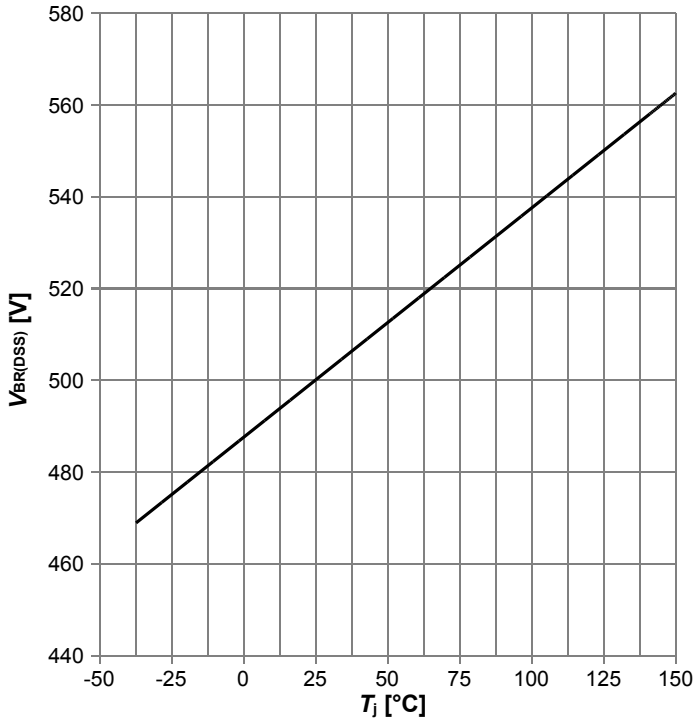
V_{GS}=f(Q_{gate}); I_D=1.9 A pulsed; parameter: V_{DD}

Avalanche energy



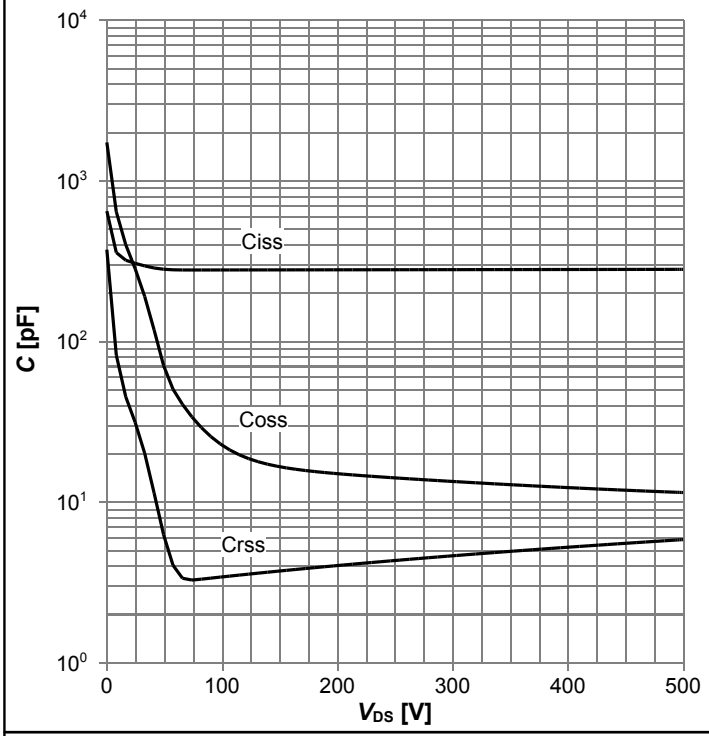
E_{AS}=f(T_j); I_D=1.9 A; V_{DD}=50 V

Drain-source breakdown voltage



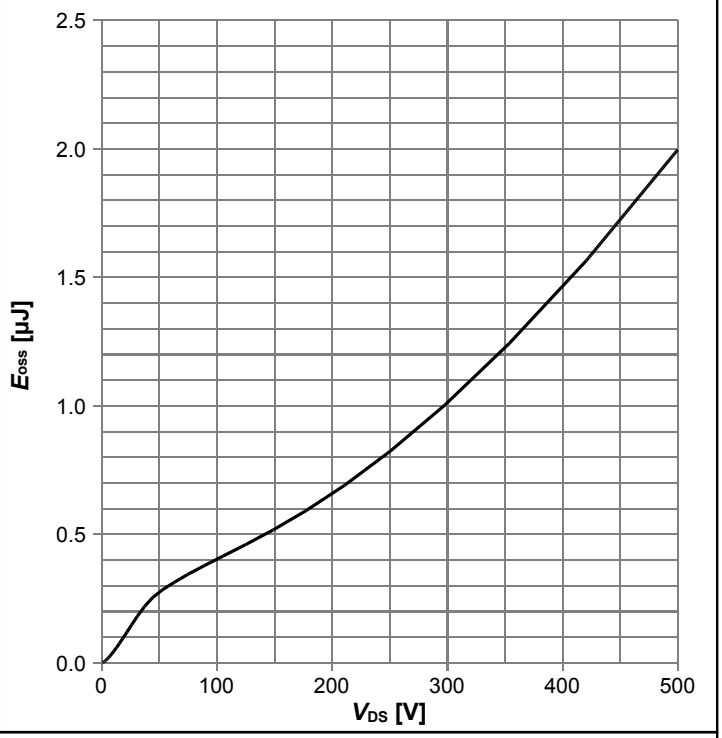
$V_{BR(DSS)}$=f(T_j); I_D=1 mA

Typ. capacitances



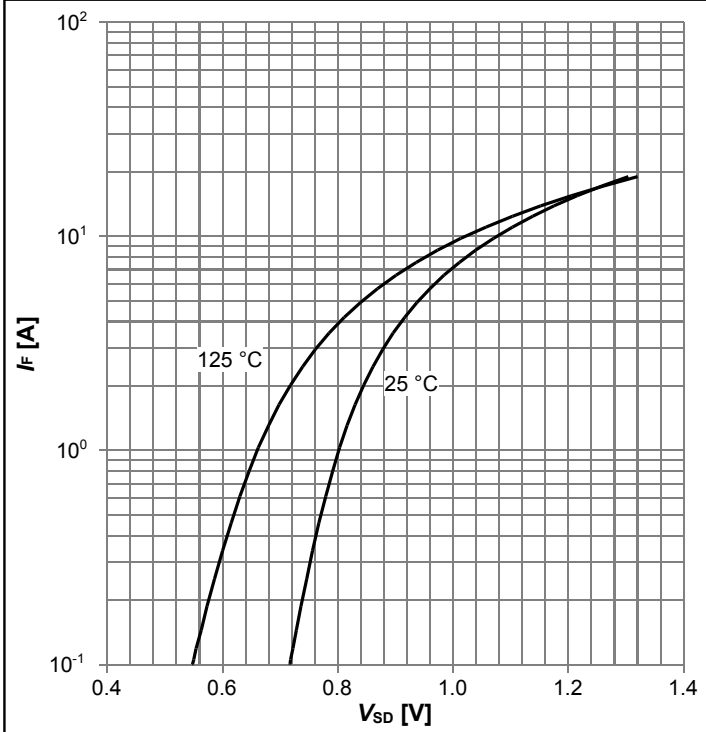
C=f(V_{DS}); V_{GS}=0 V; f=1 MHz

Typ. Coss stored energy



E_{oss}=f(V_{DS})

Forward characteristics of reverse diode



I_F=f(V_{SD}); parameter: T_j

5 Test Circuits

Table 8 Diode characteristics

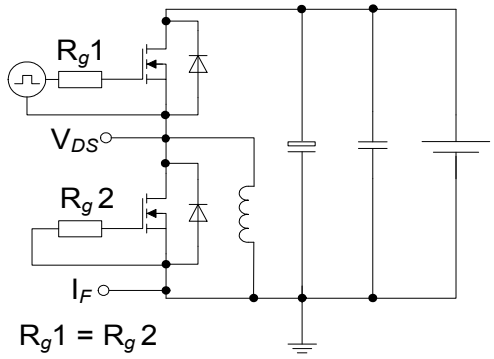
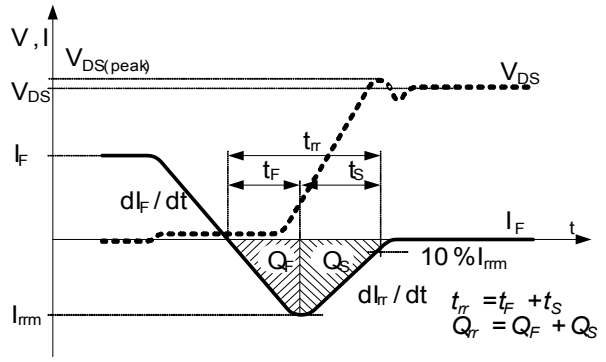
Test circuit for diode characteristics	Diode recovery waveform
	

Table 9 Switching times

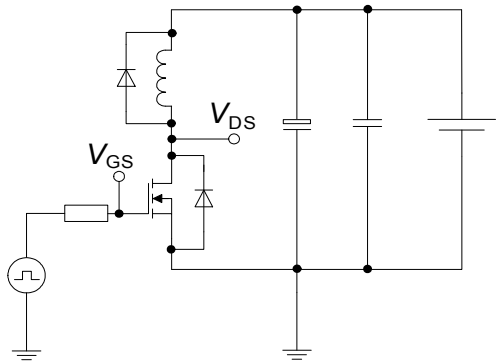
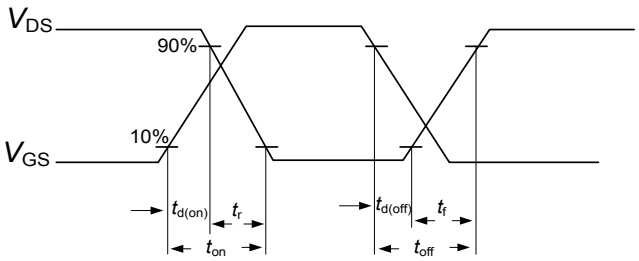
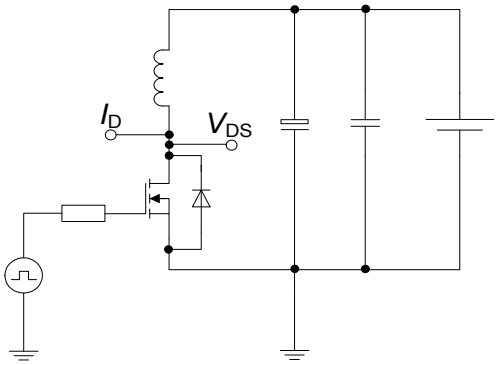
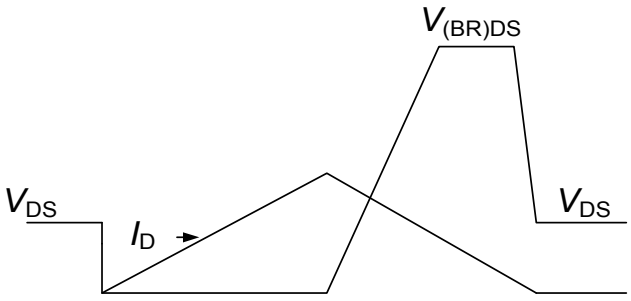
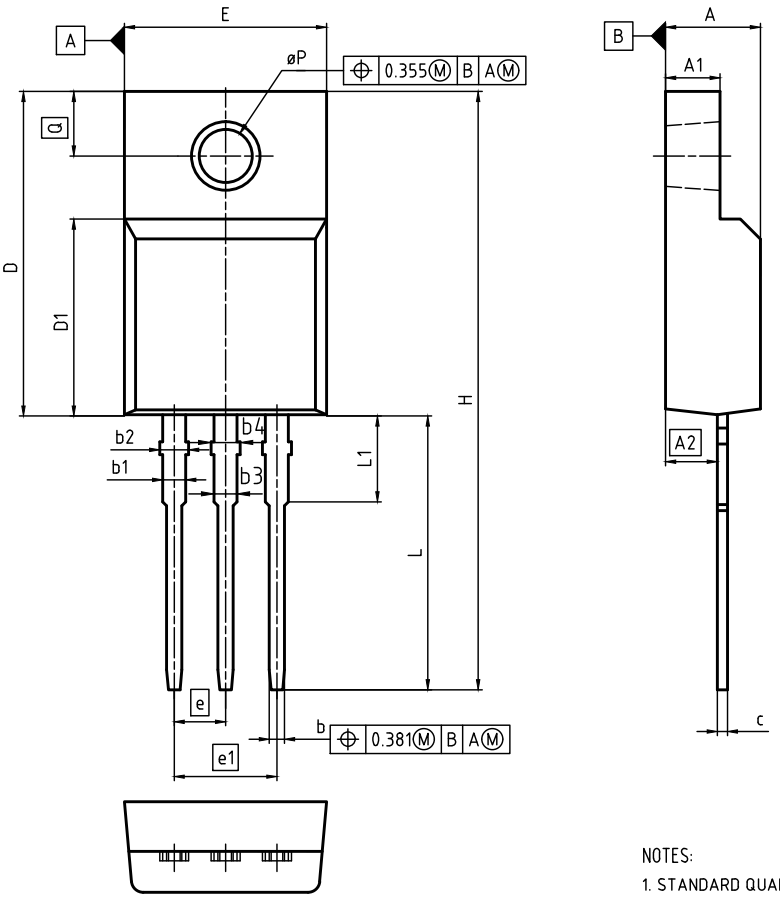
Switching times test circuit for inductive load	Switching times waveform
	

Table 10 Unclamped inductive load

Unclamped inductive load test circuit	Unclamped inductive waveform
	

6 Package Outlines



NOTES:

1. STANDARD QUALITY GRADE
2. ALL DIMENSIONS REFER TO JEDEC STANDARD TO-281 NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS

DIMENSIONS DO NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	4.50	4.90	0.177	0.193
A1	2.34	2.80	0.092	0.110
A2	2.42	2.86	0.095	0.113
b	0.65	0.90	0.026	0.035
b1	0.95	1.38	0.037	0.054
b2	1.20	1.50	0.047	0.059
b3	0.65	1.38	0.026	0.054
b4	1.20	1.50	0.047	0.059
c	0.40	0.63	0.016	0.025
D	15.67	16.15	0.617	0.636
D1	8.97	9.83	0.353	0.387
E	10.00	10.65	0.394	0.419
e	2.54 (BSC)		0.100 (BSC)	
e1	5.08		0.200	
N	3		3	
H	28.70	29.75	1.130	1.171
L	12.78	13.75	0.503	0.541
L1	2.83	3.45	0.111	0.136
øP	3.00	3.38	0.118	0.133
Q	3.15	3.50	0.124	0.138

DOCUMENT NO.
Z8B00181328
SCALE 0 2.5 0 2.5 5mm
EUROPEAN PROJECTION
ISSUE DATE 29-04-2016
REVISION 01

Figure 1 Outline PG-TO 220 FullPAK, dimensions in mm/inches

7 Appendix A

Table 11 Related Links

- **IFX CoolMOS Webpage:** www.infineon.com
- **IFX Design tools:** www.infineon.com

Revision History

IPA50R800CE

Revision: 2016-07-12, Rev. 2.3

Previous Revision

Revision	Date	Subjects (major changes since last revision)
2.0	2012-08-24	Release of final version
2.1	2014-06-12	Release of final datasheet
2.2	2016-06-13	Updated ID ratings, package marking code & package drawing
2.3	2016-07-12	Changed marking information in page 1

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Trademarks updated August 2015

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For further information on technology, delivery terms and conditions and prices please contact your nearest Infineon Technologies Office (**www.infineon.com**).

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Due to technical requirements, components may contain dangerous substances. For information on the types in question, please contact the nearest Infineon Technologies Office.
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Parça koduyla arama

Üretici parça numarasını yazın; stok ve fiyatı hemen görün.

www.entegreci.com

Ürün kategorileri

Entegreden kapasitöre tüm elektronik komponent kategorileri.

Kategorilere göz atın

Üreticiler

Aradığınız üreticinin ürünlerini tek sayfada inceleyin.

Üreticileri görün

Toplu alım ve teklif

Listede olmayan ya da yüksek adetli parçalar için teklif isteyin.

Teklif isteyin

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