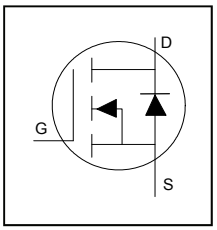
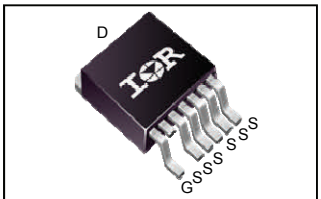
HEXFET® Power MOSFET

Application

- Brushed Motor drive applications
- BLDC Motor drive applications
- Battery powered circuits
- Half-bridge and full-bridge topologies
- Synchronous rectifier applications
- Resonant mode power supplies
- OR-ing and redundant power switches
- DC/DC and AC/DC converters
- DC/AC Inverters



V_{DSS}	135V
$R_{DS(on)}$ typ.	4.7mΩ
max	5.9mΩ
I_D (Silicon Limited)	160A



D²PAK-7Pin
IRF135SA204

Benefits

- Improved Gate, Avalanche and Dynamic dV/dt Ruggedness
- Fully Characterized Capacitance and Avalanche SOA
- Enhanced body diode dV/dt and dI/dt Capability
- Lead-Free, RoHS Compliant, Halogen-Free

G	D	S
Gate	Drain	Source

Base part number	Package Type	Standard Pack		Orderable Part Number
		Form	Quantity	
IRF135SA204	D²PAK-7Pin	Tape and Reel	800	IRF135SA204

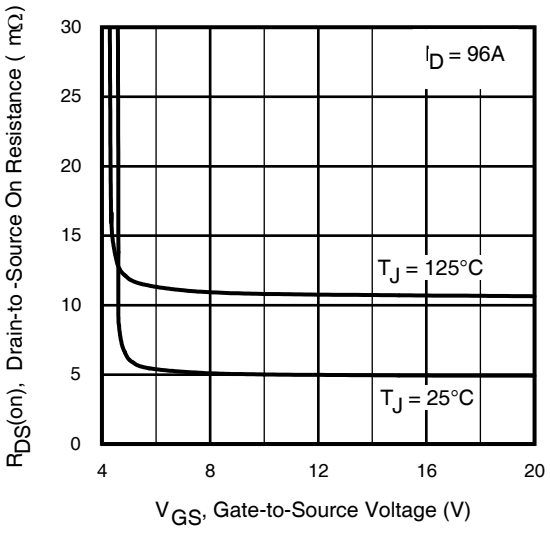


Fig 1. Typical On– Resistance vs. Gate Voltage

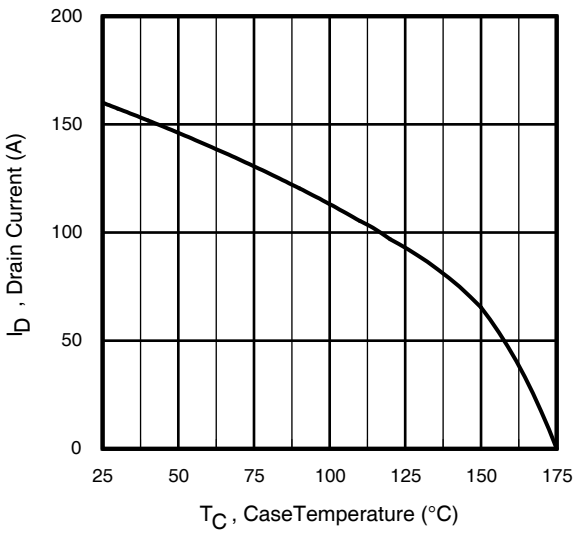


Fig 2. Maximum Drain Current vs. Case Temperature

Absolute Maximum Rating

Symbol	Parameter	Max.	Units
I_D @ T_C = 25°C	Continuous Drain Current, V_{GS} @ 10V	160	A
I_D @ T_C = 100°C	Continuous Drain Current, V_{GS} @ 10V	113	
I_{DM}	Pulsed Drain Current ①	608	
P_D @T_C = 25°C	Maximum Power Dissipation	500	W
	Linear Derating Factor	3.3	W/°C
V_{GS}	Gate-to-Source Voltage	± 20	V
T_J T_{STG}	Operating Junction and Storage Temperature Range	-55 to + 175	°C
	Soldering Temperature, for 10 seconds (1.6mm from case)	300	

Avalanche Characteristics

$E_{AS\ (Thermally\ limited)}$	Single Pulse Avalanche Energy ②	670	mJ
$E_{AS\ (Thermally\ limited)}$	Single Pulse Avalanche Energy ⑨	1280	
I_{AR}	Avalanche Current ①	See Fig 15, 16, 23a, 23b	A
E_{AR}	Repetitive Avalanche Energy ①		mJ

Thermal Resistance

Symbol	Parameter	Typ.	Max.	Units
$R_{\theta JC}$	Junction-to-Case ⑦	–––	0.3	°C/W
$R_{\theta JA}$	Junction-to-Ambient (PCB Mount) ⑧	–––	40	

Static @ T_J = 25°C (unless otherwise specified)

Symbol	Parameter	Min.	Typ.	Max.	Units	Conditions
$V_{(BR)DSS}$	Drain-to-Source Breakdown Voltage	135	–––	–––	V	V_{GS} = 0V, I_D = 250µA
$\Delta V_{(BR)DSS}/\Delta T_J$	Breakdown Voltage Temp. Coefficient	–––	0.14	–––	V/°C	Reference to 25°C, I_D = 5mA ①
$R_{DS(on)}$	Static Drain-to-Source On-Resistance	–––	4.7	5.9	mΩ	V_{GS} = 10V, I_D = 96A
$V_{GS(th)}$	Gate Threshold Voltage	2.0	3.0	4.0	V	V_{DS} = V_{GS}, I_D = 250µA
I_{DSS}	Drain-to-Source Leakage Current	–––	–––	20	µA	V_{DS} =135 V, V_{GS} = 0V
		–––	–––	250		V_{DS} = 135V,V_{GS} = 0V,T_J =125°C
I_{GSS}	Gate-to-Source Forward Leakage	–––	–––	100	nA	V_{GS} = 20V
	Gate-to-Source Reverse Leakage	–––	–––	-100		V_{GS} = -20V
R_G	Gate Resistance	–––	2.2	–––	Ω	

Notes:

① Repetitive rating; pulse width limited by max. junction temperature.

② Limited by T_{Jmax}, starting T_J = 25°C, L = 146µH, R_G = 50Ω, I_{AS} = 96A, V_{GS} =10V.

③ I_{SD} ≤ 96A, di/dt ≤ 2200A/µs, V_{DD} ≤ $V_{(BR)DSS}$, T_J ≤ 175°C.

④ Pulse width ≤ 400µs; duty cycle ≤ 2%.

⑤ C_{oss} eff. (TR) is a fixed capacitance that gives the same charging time as C_{oss} while V_{DS} is rising from 0 to 80% V_{DSS}.

⑥ C_{oss} eff. (ER) is a fixed capacitance that gives the same energy as C_{oss} while V_{DS} is rising from 0 to 80% V_{DSS}.

⑦ R_θ is measured at T_J approximately 90°C.

⑧ When mounted on 1 inch square PCB (FR-4). Please refer to AN-994 for more details:
http://www.irf.com/technical-info/appnotes/an-994.pdf

⑨ Limited by T_{Jmax}, starting T_J = 25°C, L = 1.0mH, R_G = 50Ω, I_{AS} = 49A, V_{GS} =10V.

Dynamic Electrical Characteristics @ T_J = 25°C (unless otherwise specified)

Symbol	Parameter	Min.	Typ.	Max.	Units	Conditions
gfs	Forward Transconductance	270	—	—	S	V_{DS} = 10V, I_D = 96A
Q_g	Total Gate Charge	—	210	315	nC	I_D = 96A
Q_{gs}	Gate-to-Source Charge	—	54	—		V_{DS} = 68V
Q_{gd}	Gate-to-Drain Charge	—	57	—		V_{GS} = 10V
Q_{sync}	Total Gate Charge Sync. (Qg– Qgd)	—	153	—		
$t_{d(on)}$	Turn-On Delay Time	—	20	—	ns	V_{DD} = 81V
t_r	Rise Time	—	56	—		I_D = 96A
$t_{d(off)}$	Turn-Off Delay Time	—	140	—		R_G= 2.7Ω
t_f	Fall Time	—	56	—		V_{GS} = 10V④
C_{iss}	Input Capacitance	—	11690	—	pF	V_{GS} = 0V
C_{oss}	Output Capacitance	—	650	—		V_{DS} = 50V
C_{rss}	Reverse Transfer Capacitance	—	290	—		f = 1.0MHz, See Fig.7
$C_{oss\ eff.(ER)}$	Effective Output Capacitance (Energy Related)	—	630	—		V_{GS} = 0V, VDS = 0V to 108V⑥
$C_{oss\ eff.(TR)}$	Output Capacitance (Time Related)	—	845	—		V_{GS} = 0V, VDS = 0V to 108V⑤

Diode Characteristics

Symbol	Parameter	Min.	Typ.	Max.	Units	Conditions
I_S	Continuous Source Current (Body Diode)	—	—	160	A	MOSFET symbol showing the integral reverse p-n junction diode. 
I_{SM}	Pulsed Source Current (Body Diode) ①	—	—	608		
V_{SD}	Diode Forward Voltage	—	—	1.3	V	T_J = 25°C,I_S = 96A,V_{GS} = 0V ④
dv/dt	Peak Diode Recovery dv/dt③	—	22	—	V/ns	T_J = 175°C,I_S =96A,V_{DS} = 135V
t_{rr}	Reverse Recovery Time	—	85	—	ns	T_J = 25°C V_{DD} = 115V
		—	98	—		T_J = 125°C I_F = 96A,
Q_{rr}	Reverse Recovery Charge	—	315	—	nC	T_J = 25°C di/dt = 100A/μs ④
		—	430	—		T_J = 125°C
I_{RRM}	Reverse Recovery Current	—	6.6	—	A	T_J = 25°C

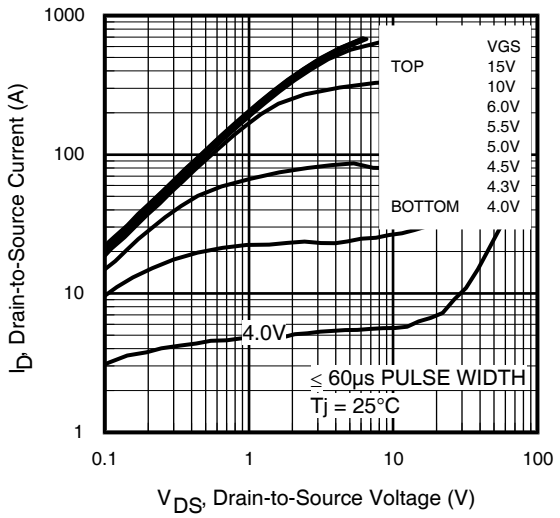


Fig 3. Typical Output Characteristics

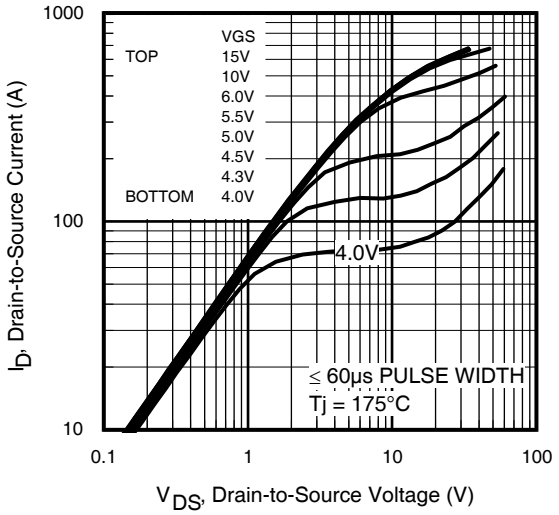


Fig 4. Typical Output Characteristics

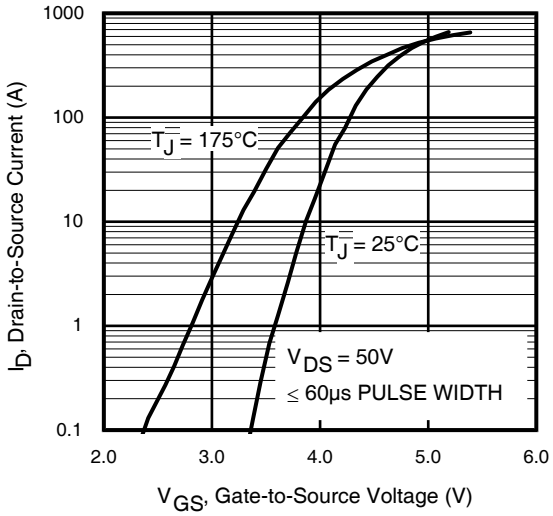


Fig 5. Typical Transfer Characteristics

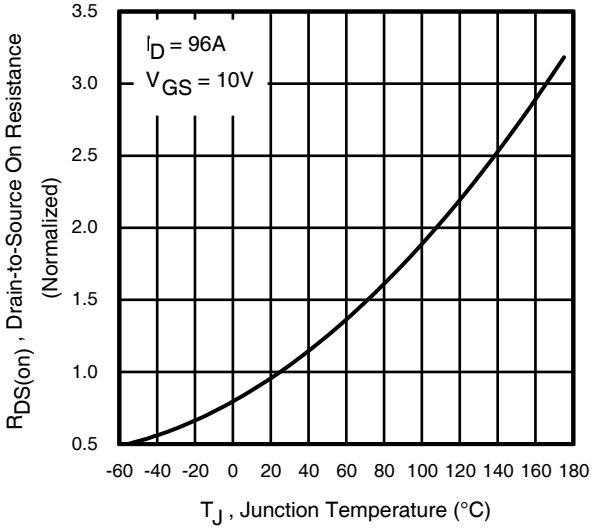


Fig 6. Normalized On-Resistance vs. Temperature

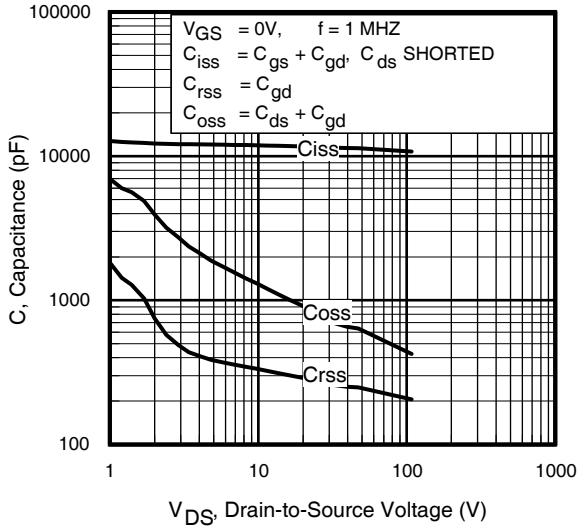


Fig 7. Typical Capacitance vs. Drain-to-Source Voltage

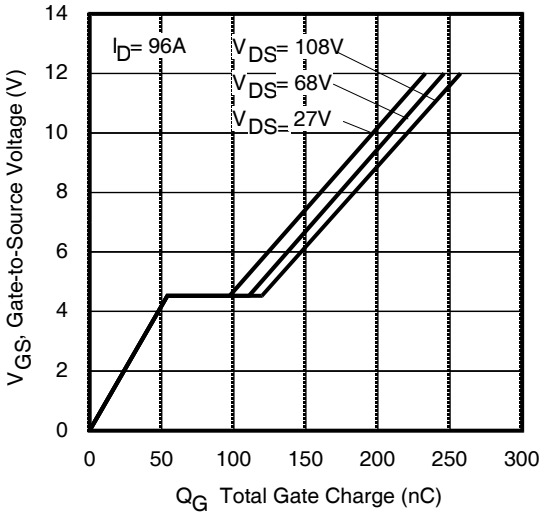


Fig 8. Typical Gate Charge vs.Gate-to-Source Voltage

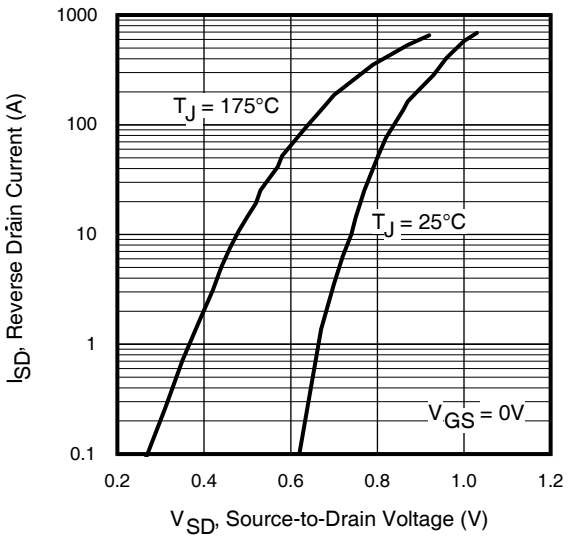


Fig 9. Typical Source-Drain Diode Forward Voltage

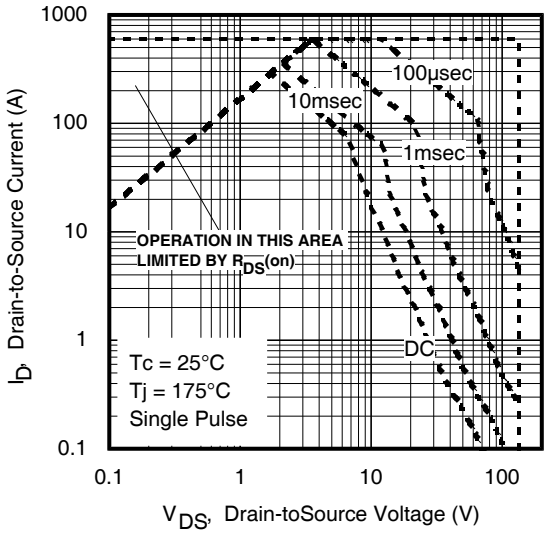


Fig 10. Maximum Safe Operating Area

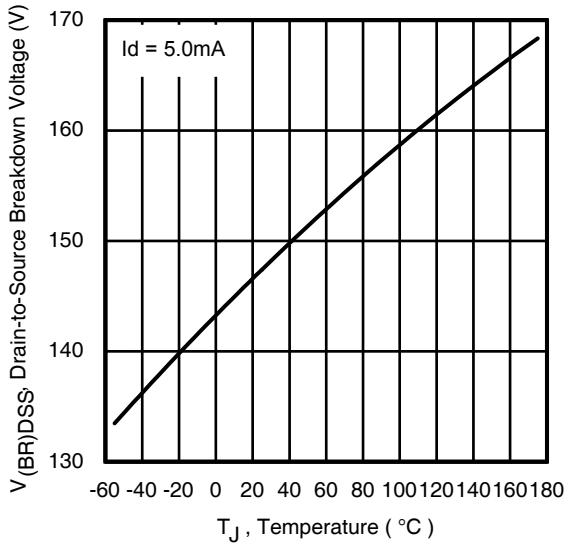


Fig 11. Drain-to-Source Breakdown Voltage

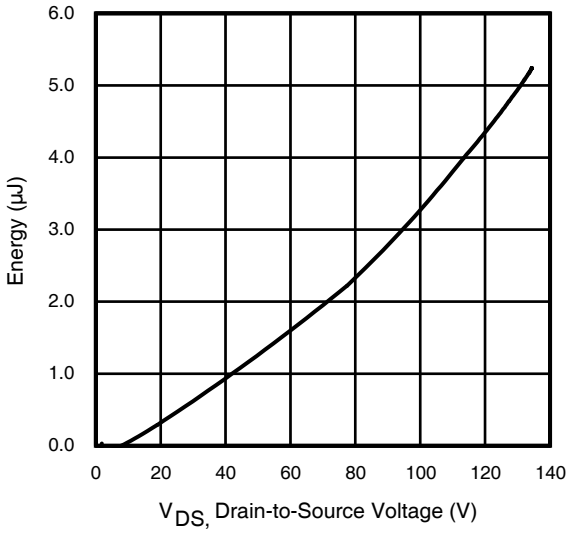


Fig 12. Typical C_{oss} Stored Energy

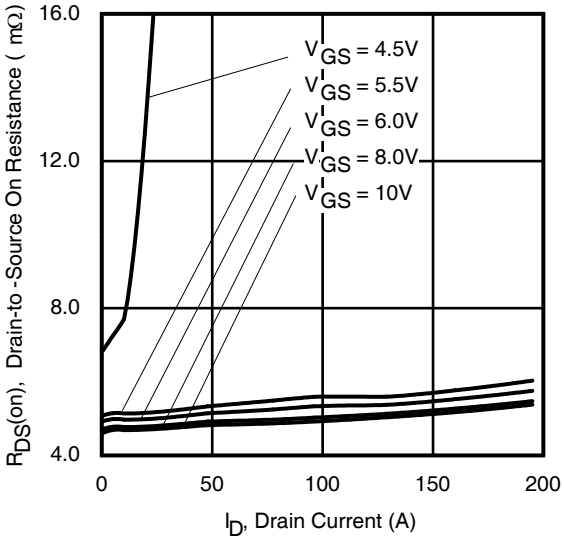


Fig 13. Typical On–Resistance vs. Drain Current

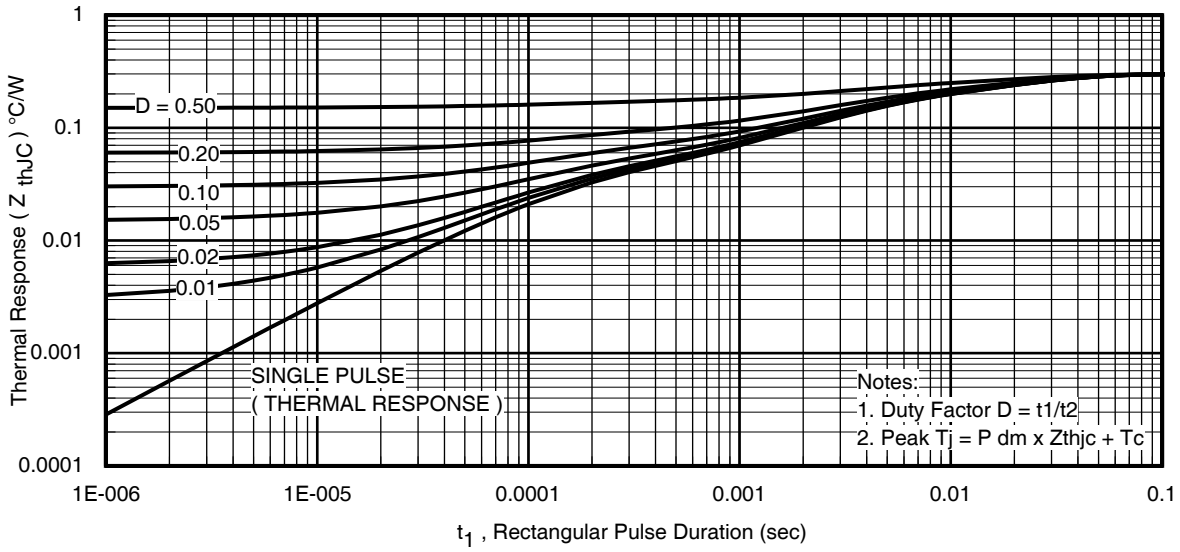


Fig 14. Maximum Effective Transient Thermal Impedance, Junction-to-Case

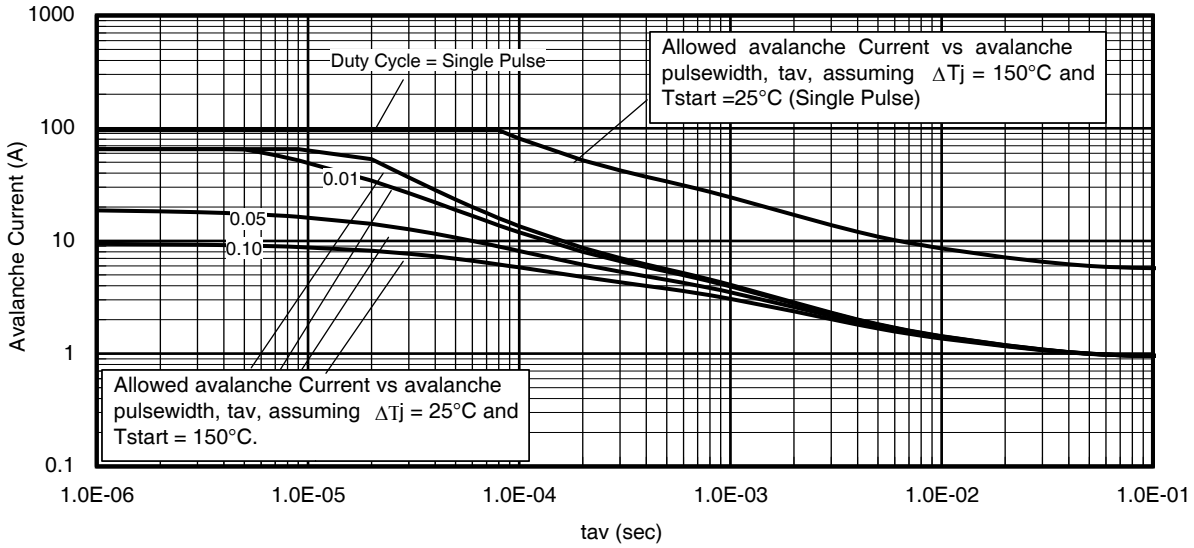


Fig 15. Avalanche Current vs. Pulse Width

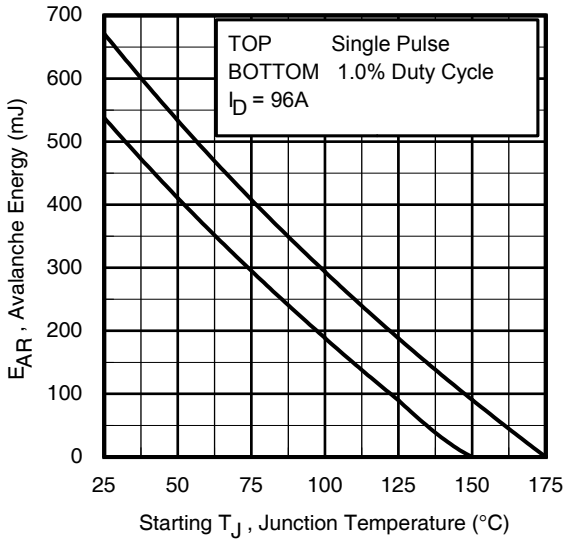


Fig 16. Maximum Avalanche Energy vs. Temperature

Notes on Repetitive Avalanche Curves , Figures 15, 16:
(For further info, see AN-1005 at www.irf.com)

1.Avalanche failures assumption:
Purely a thermal phenomenon and failure occurs at a temperature far in excess of T_{jmax}. This is validated for every part type.

2. Safe operation in Avalanche is allowed as long asT_{jmax} is not exceeded.

3. Equation below based on circuit and waveforms shown in Figures 23a, 23b.

4. $P_{D\ (ave)}$ = Average power dissipation per single avalanche pulse.

5. BV = Rated breakdown voltage (1.3 factor accounts for voltage increase during avalanche).

6. I_{av} = Allowable avalanche current.

7. ΔT = Allowable rise in junction temperature, not to exceed T_{jmax} (assumed as 25°C in Figure 14, 15).

t_{av} = Average time in avalanche.

D = Duty cycle in avalanche = tav ·f

$Z_{thJC}(D, t_{av})$ = Transient thermal resistance, see Figures 14)

PD (ave) = 1/2 (1.3·BV·I_{av}) = $\Delta T/ Z_{thJC}$

$I_{av} = 2\Delta T/ [1.3 \cdot BV \cdot Z_{th}]$

$E_{AS\ (AR)} = P_{D\ (ave)} \cdot t_{av}$

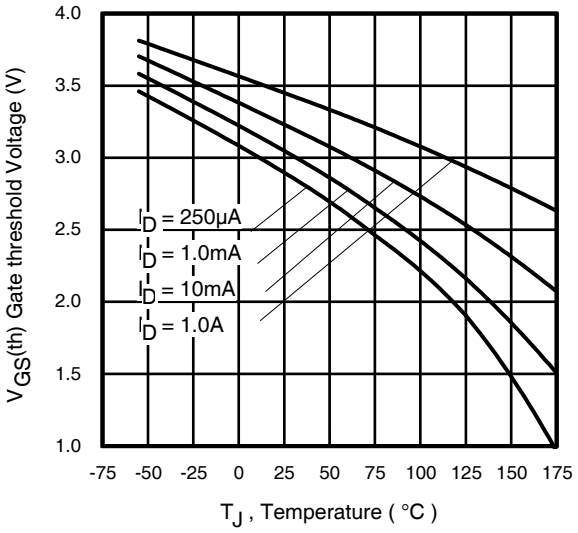


Fig 17. Threshold Voltage vs. Temperature

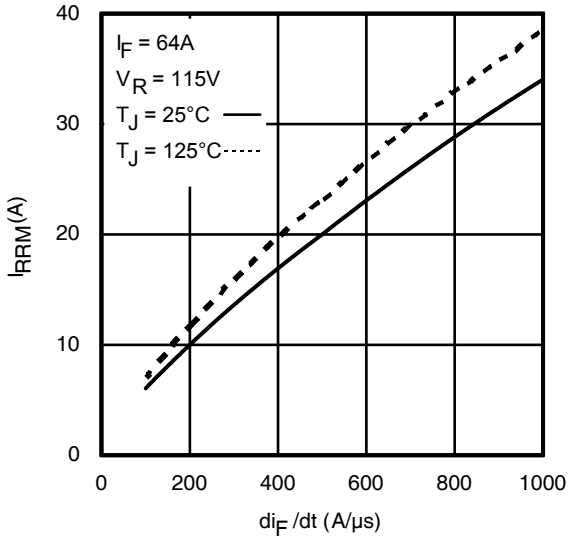


Fig 18. Typical Recovery Current vs. dif/dt

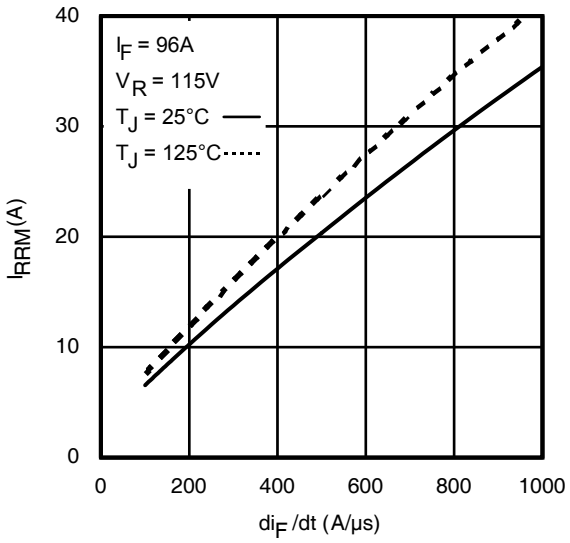


Fig 19. Typical Recovery Current vs. dif/dt

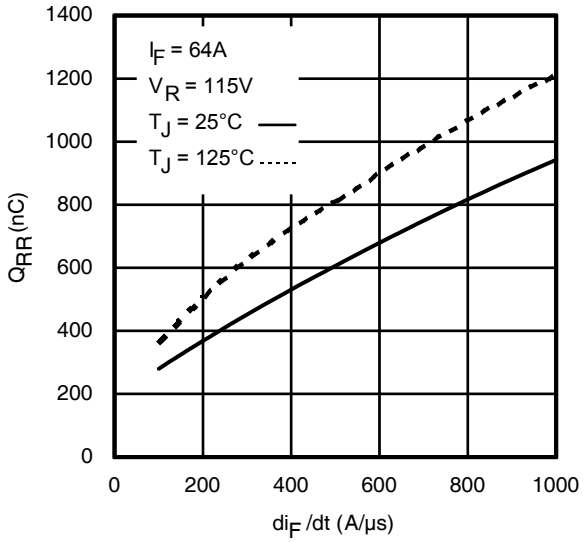


Fig 20. Typical Stored Charge vs. dif/dt

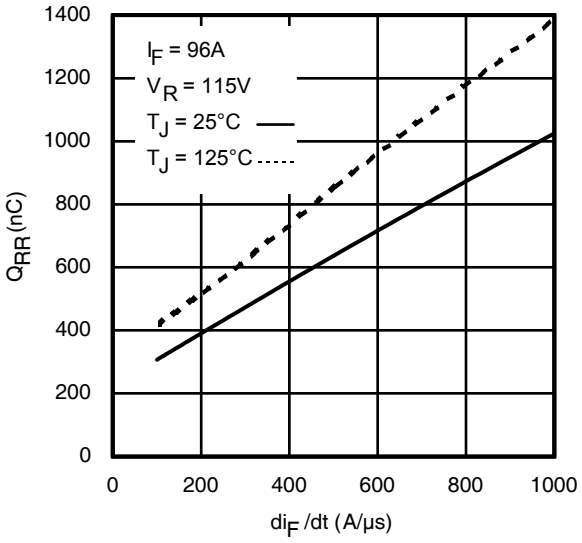


Fig 21. Typical Stored Charge vs. dif/dt

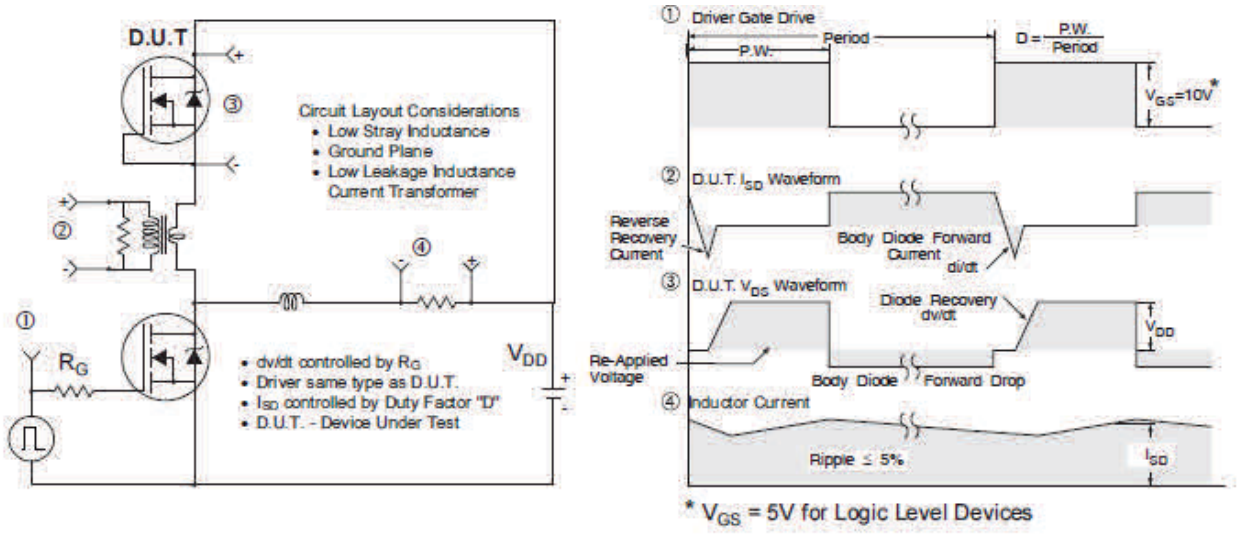


Fig 22. Peak Diode Recovery dv/dt Test Circuit for N-Channel HEXFET® Power MOSFETs

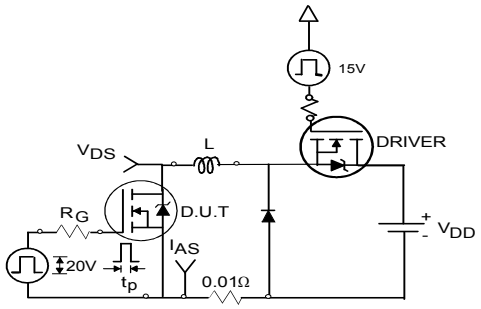


Fig 23a. Unclamped Inductive Test Circuit

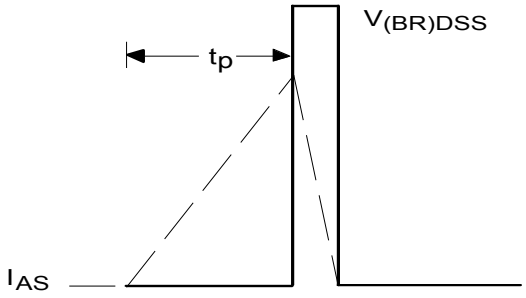


Fig 23b. Unclamped Inductive Waveforms

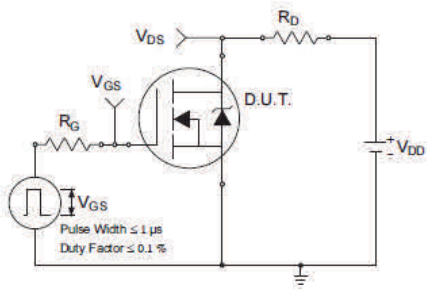


Fig 24a. Switching Time Test Circuit

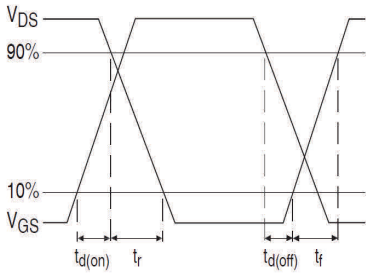


Fig 24b. Switching Time Waveforms

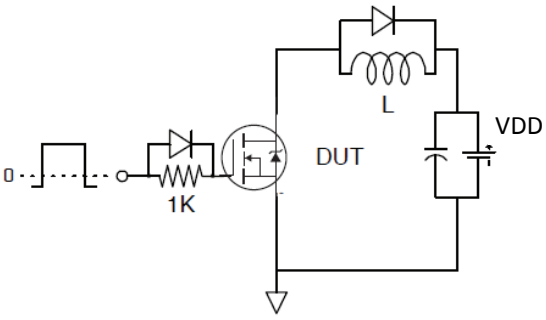


Fig 25a. Gate Charge Test Circuit

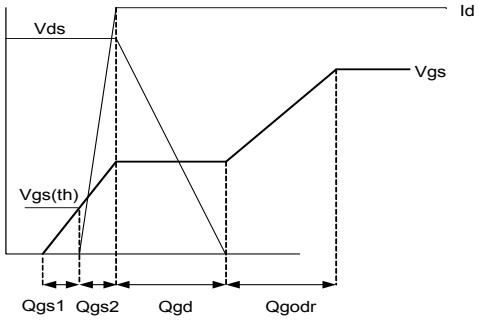
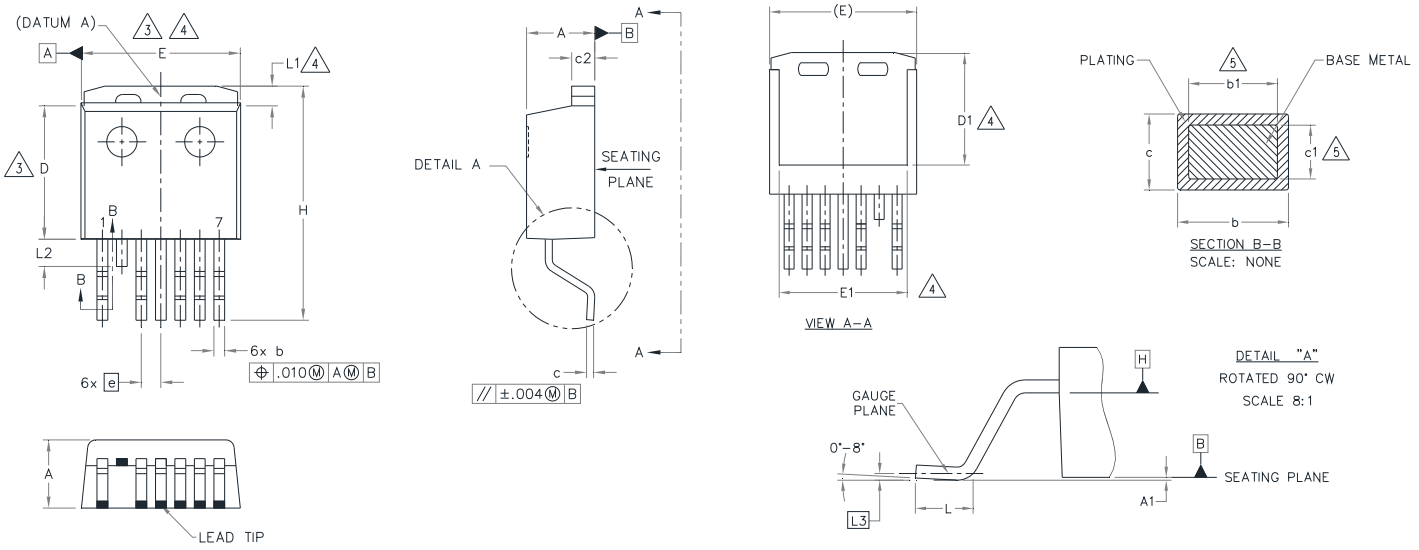


Fig 25b. Gate Charge Waveform

D²PAK-7Pin Package Outline (Dimensions are shown in millimeters (inches))



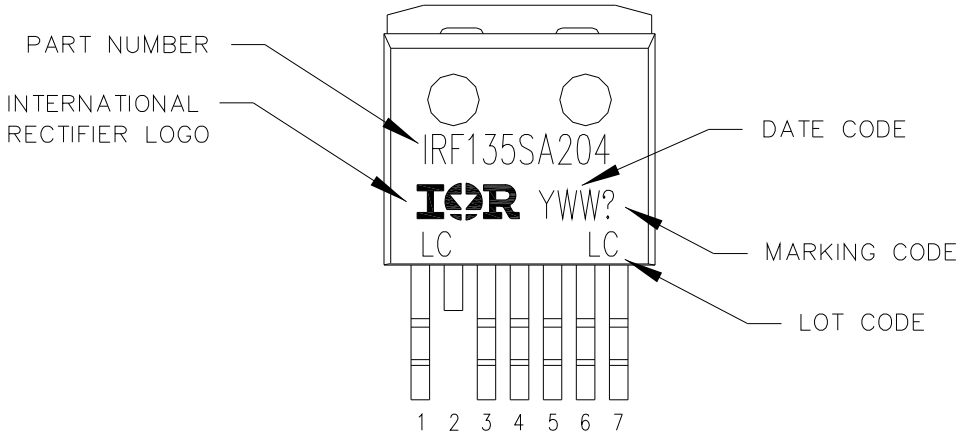
SYMBOL	DIMENSIONS				NOTES
	MILLIMETERS		INCHES		
	MIN.	MAX.	MIN.	MAX.	
A	4.06	4.83	.160	.190	
A1	–	0.254	–	.010	
b	0.51	0.91	.020	.036	
b1	0.51	0.81	.020	.032	5
c	0.38	0.74	.015	.029	
c1	0.38	0.58	.015	.023	5
c2	1.14	1.65	.045	.065	
D	8.38	9.65	.330	.380	3
D1	6.86	7.42	.270	.292	4
E	9.65	10.54	.380	.415	3,4
E1	8.00	9.00	.315	.354	4
e	1.27 BSC		.050 BSC		
H	14.61	15.88	.575	.625	
L	1.78	2.79	.070	.110	
L1	–	1.68	–	.066	4
L2	–	1.78	–	.070	
L3	0.25 BSC		.010 BSC		

NOTES:

1. DIMENSIONING AND TOLERANCING AS PER ASME Y14.5M–1994
2. DIMENSIONS ARE SHOWN IN MILLIMETERS [INCHES].
3. DIMENSION D & E DO NOT INCLUDE MOLD FLASH. MOLD FLASH SHALL NOT EXCEED 0.127 [.005"] PER SIDE. THESE DIMENSIONS ARE MEASURED AT THE OUTMOST EXTREMES OF THE PLASTIC BODY AT DATUM H.
4. THERMAL PAD CONTOUR OPTIONAL WITHIN DIMENSION E, L1, D1 & E1.
5. DIMENSION b1 AND c1 APPLY TO BASE METAL ONLY.
6. DATUM A & B TO BE DETERMINED AT DATUM PLANE H.
7. CONTROLLING DIMENSION: INCH.
8. OUTLINE CONFORMS TO JEDEC OUTLINE TO–263CB. EXCEPT FOR DIMS. E, E1 & D1.

Note: For the most current drawing please refer to IR website at http://www.irf.com/package/

D²Pak-7Pin Part Marking Information

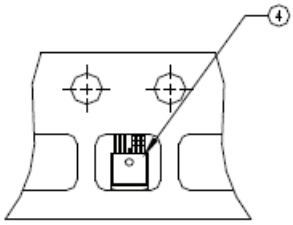


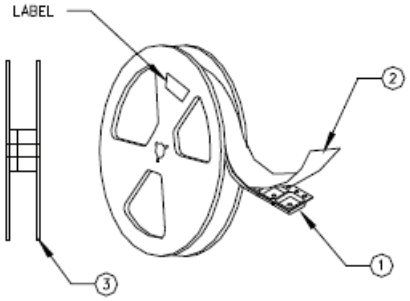
D²PAK-7Pin Tape and Reel

NOTES, TAPE & REEL, LABELLING:

1. TAPE AND REEL.
   - 1.1 REEL SIZE 13 INCH DIAMETER.
   - 1.2 EACH REEL CONTAINING 800 DEVICES.
   - 1.3 THERE SHALL BE A MINIMUM OF 42 SEALED POCKETS CONTAINED IN THE LEADER AND A MINIMUM OF 15 SEALED POCKETS IN THE TRAILER.
   - 1.4 PEEL STRENGTH MUST CONFORM TO THE SPEC. NO. 71-9667.
   - 1.5 PART ORIENTATION SHALL BE AS SHOWN BELOW.
   - 1.6 REEL MAY CONTAIN A MAXIMUM OF TWO UNIQUE LOT CODE/DATE CODE COMBINATIONS. REWORKED REELS MAY CONTAIN A MAXIMUM OF THREE UNIQUE LOT CODE/DATE CODE COMBINATIONS. HOWEVER, THE LOT CODES AND DATE CODES WITH THEIR RESPECTIVE QUANTITIES SHALL APPEAR ON THE BAR CODE LABEL FOR THE AFFECTED REEL.

2. LABELLING (REEL AND SHIPPING BAG).
   - 2.1 CUST. PART NUMBER (BAR CODE): IRFXXXXSTRL-7P
   - 2.2 CUST. PART NUMBER (TEXT CODE): IRFXXXXSTRL-7P
   - 2.3 I.R. PART NUMBER: IRFXXXXSTRL-7P
   - 2.4 QUANTITY:
   - 2.5 VENDOR CODE: IR
   - 2.6 LOT CODE:
   - 2.7 DATE CODE:





Note: For the most current drawing please refer to IR website at http://www.irf.com/package/

Qualification Information†

Qualification Level	Industrial (per JEDEC JESD47F) ††	
Moisture Sensitivity Level	D^2PAK-7Pin	MSL1
RoHS Compliant	Yes	

† Qualification standards can be found at International Rectifier's web site: http://www.irf.com/product-info/reliability/

†† Applicable version of JEDEC standard at the time of product release.

Revision History

Date	Comments
05/12/2017	• Corrected package picture added "s" on pin number 2 - page 1. • Changed datasheet with Infineon logo - all pages. • Added disclaimer on last page

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