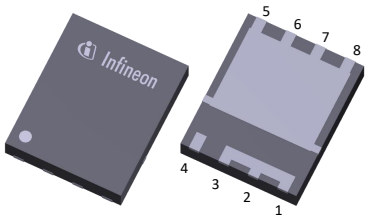
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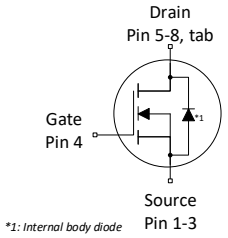
OptiMOS™ 6 Power-Transistor, 60 V

PG-TSON-8



Features

- Optimized for high performance SMPS
- Optimized for Synchronous rectification
- N-channel, logic level
- Very low on-resistance $R_{DS(on)}$
- Superior thermal resistance
- 100% avalanche tested
- Pb-free lead plating; RoHS compliant
- Halogen-free according to IEC61249-2-21



Product validation

Fully qualified according to JEDEC for Industrial Applications

Table 1 Key performance parameters

Parameter	Value	Unit
V_{DS}	60	V
$R_{DS(on),max}$	0.7	mΩ
I_D	440	A
Q_{oss}	190	nC
Q_G	85	nC
Q_{rr} (1000A/µs)	361	nC

Part number	Package	Marking	Related links
ISC007N06LM6	PG-TSON-8	007N6L6	-

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1 Maximum ratings

at T_A=25 °C, unless otherwise specified

Table 2 Maximum ratings

Parameter	Symbol	Values			Unit	Note / Test condition
		Min.	Typ.	Max.		
Continuous drain current [1]	I_D	-	-	440	A	V_{GS}=10 V, T_C=25 °C
				312		V_{GS}=10 V, T_C=100 °C
				278		V_{GS}=4.5 V, T_C=100 °C
				48		V_{GS}=10V, T_A=25°C, R_{thJA}=50°C/W [2]
Pulsed drain current [3]	$I_{D,pulse}$	-	-	1760	A	T_A=25 °C
Avalanche energy, single pulse [4]	E_{AS}	-	-	929	mJ	I_D=50 A, R_{GS}=25 Ω
Gate source voltage	V_{GS}	-20	-	20	V	-
Power dissipation	P_{tot}	-	-	259	W	T_C=25 °C
				3.0		T_A=25 °C, R_{thJA}=50 °C/W [2]
Operating and storage temperature	T_j, T_{stg}	-55	-	175	°C	-

[1] Rating refers to the product only with datasheet specified absolute maximum values, maintaining case temperature as specified. For other case temperatures please refer to Diagram 2. De-rating will be required based on the actual environmental conditions.

[2] Device on 40 mm x 40 mm x 1.5 mm epoxy PCB FR4 with 6 cm^2 (one layer, 70 µm thick) copper area for drain connection. PCB is vertical in still air.

[3] See Diagram 3 for more detailed information

[4] See Diagram 13 for more detailed information

2 Thermal characteristics

Table 3 Thermal characteristics

Parameter	Symbol	Values			Unit	Note / Test condition
		Min.	Typ.	Max.		
Thermal resistance, junction - case, bottom	R_{thJC}	-	0.29	0.58	°C/W	-
Thermal resistance, junction - case, top	R_{thJC}		-	20		
Thermal resistance, junction - ambient, 6 cm^2 cooling area [5)]	R_{thJA}		-	50		

[5)] Device on 40 mm x 40 mm x 1.5 mm epoxy PCB FR4 with 6 cm^2 (one layer, 70 µm thick) copper area for drain connection. PCB is vertical in still air.

3 Electrical characteristics

at T_j=25 °C, unless otherwise specified

Table 4 Static characteristics

Parameter	Symbol	Values			Unit	Note / Test condition
		Min.	Typ.	Max.		
Drain-source breakdown voltage	$V_{(BR)DSS}$	60	-	-	V	V_{GS}=0 V, I_D=1 mA
Gate threshold voltage	$V_{GS(th)}$	1.1	1.7	2.3	V	V_{DS}=V_{GS}, I_D=149 µA
Zero gate voltage drain current	I_{DSS}	-	0.1	1.0	µA	V_{DS}=48 V, V_{GS}=0 V, T_j=25 °C
			10	100		V_{DS}=48 V, V_{GS}=0 V, T_j=125 °C
Gate-source leakage current	I_{GSS}	-	10	100	nA	V_{GS}=20 V, V_{DS}=0 V
Drain-source on-state resistance	$R_{DS(on)}$	-	0.62	0.7	mΩ	V_{GS}=10 V, I_D=50 A
			0.76	0.88		V_{GS}=4.5 V, I_D=25 A
Gate resistance	R_G	-	0.9	-	Ω	-
Transconductance [6]	g_{fs}	170	340	-	S	$\|V_{DS}\|\geq 2\|I_D\|R_{DS(on)max}$, I_D=50 A

[6] Defined by design. Not subject to production test.

Table 5 Dynamic characteristics

Parameter	Symbol	Values			Unit	Note / Test condition
		Min.	Typ.	Max.		
Input capacitance [7]	C_{iss}	-	13000	17000	pF	V_{GS}=0 V, V_{DS}=30 V, f=1 MHz
Output capacitance [7]	C_{oss}		3300	4300		
Reverse transfer capacitance [7]	C_{rss}		60	100		
Turn-on delay time	$t_{d(on)}$	-	13.5	-	ns	V_{DD}=30 V, V_{GS}=10 V, I_D=50 A, $R_{G,ext}$=1.6 Ω
Rise time	t_r		6.0			
Turn-off delay time	$t_{d(off)}$		32.9			
Fall time	t_f		8.5			

[7] Defined by design. Not subject to production test.

Table 6 Gate charge characteristics [8)]

Parameter	Symbol	Values			Unit	Note / Test condition
		Min.	Typ.	Max.		
Gate to source charge	Q_{gs}	-	33	-	nC	V_{DD}=30 V, I_D=50 A, V_{GS}=0 to 4.5 V
Gate charge at threshold	$Q_{g(th)}$		21	-	nC	
Gate to drain charge [9)]	Q_{gd}		21	32	nC	
Switching charge	Q_{sw}		32	-	nC	
Gate charge total [9)]	Q_g		85	106	nC	
Gate plateau voltage	$V_{plateau}$		2.6	-	V	
Gate charge total [9)]	Q_g	-	177	235	nC	V_{DD}=30 V, I_D=50 A, V_{GS}=0 to 10 V
Output charge [9)]	Q_{oss}	-	190	253	nC	V_{DS}=30 V, V_{GS}=0 V

8) See "Gate charge waveforms" for parameter definition

9) Defined by design. Not subject to production test.

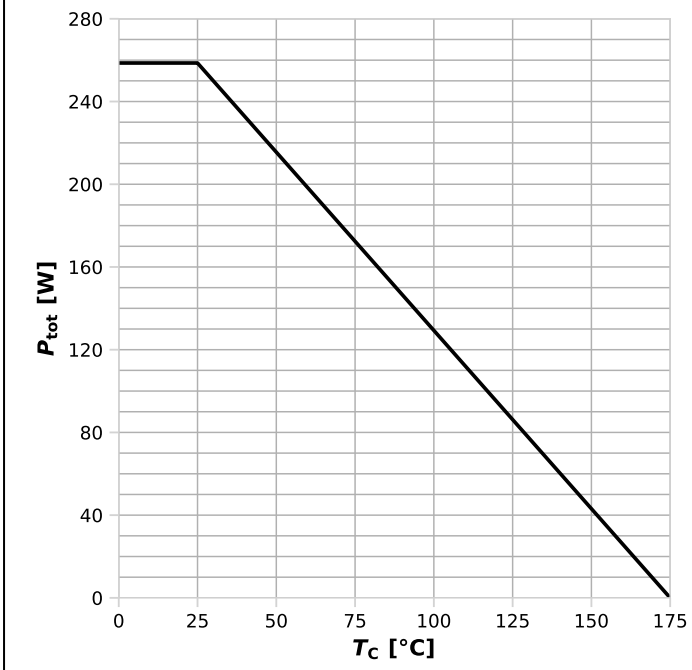
Table 7 Reverse diode

Parameter	Symbol	Values			Unit	Note / Test condition
		Min.	Typ.	Max.		
Diode continuous forward current	I_S	-	-	231	A	T_C=25 °C
Diode pulse current	$I_{S,pulse}$			1760		
Diode forward voltage	V_{SD}	-	0.79	1.0	V	V_{GS}=0 V, I_F=50 A, T_j=25 °C
Reverse recovery time [10)]	t_{rr}	-	68	136	ns	V_R=30 V, I_F=50 A, di_F/dt=100 A/µs
Reverse recovery charge [10)]	Q_{rr}		110	220	nC	
Reverse recovery time [10)]	t_{rr}	-	33	66	ns	V_R=30 V, I_F=50 A, di_F/dt=1000 A/µs
Reverse recovery charge [10)]	Q_{rr}		361	722	nC	

10) Defined by design. Not subject to production test.

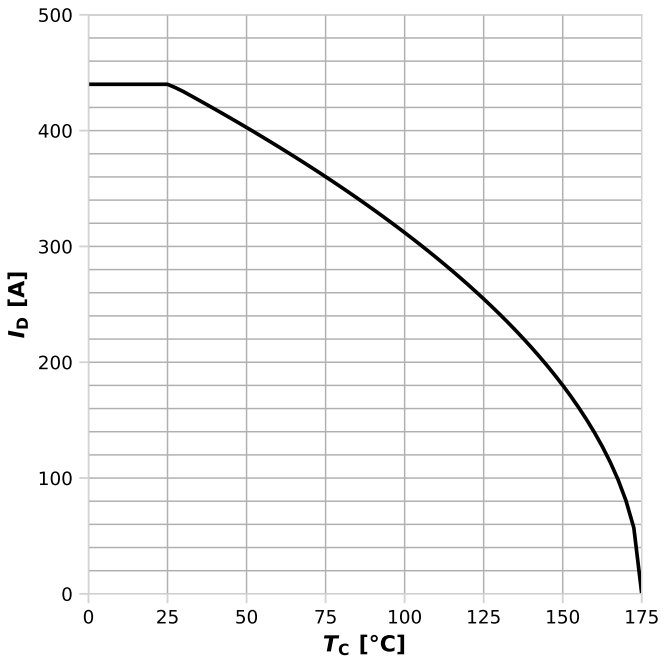
4 Electrical characteristics diagrams

Diagram 1: Power dissipation



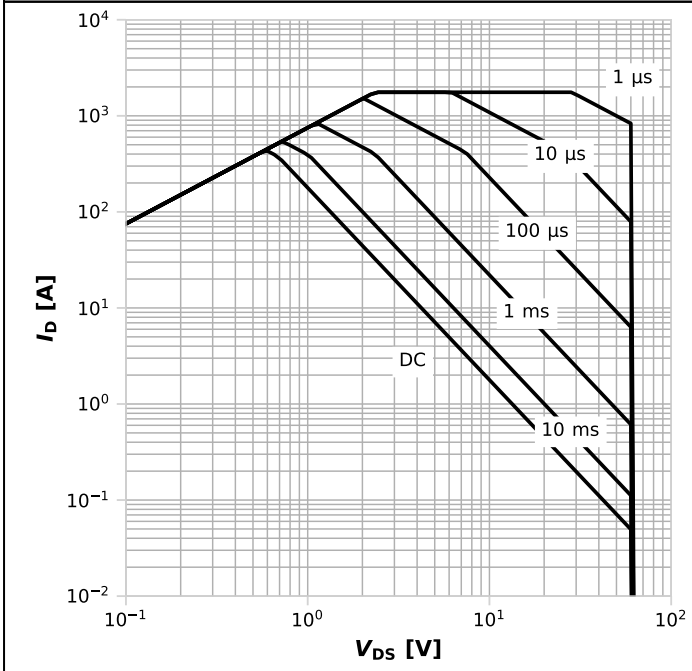
P_{tot}=f(T_C)

Diagram 2: Drain current



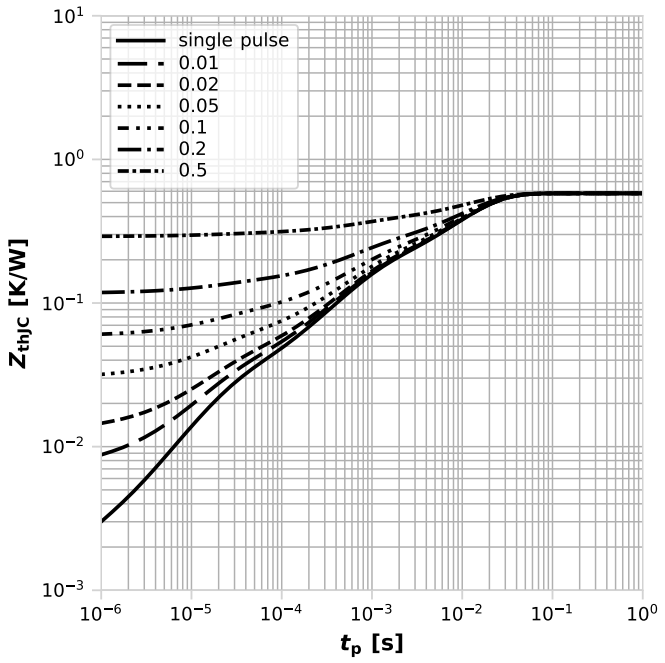
I_D=f(T_C); V_{GS}≥10 V

Diagram 3: Safe operating area



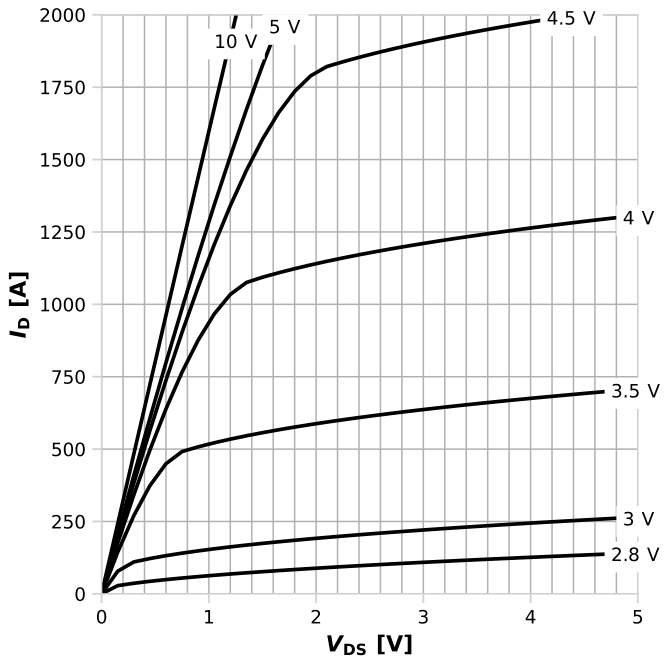
I_D=f(V_{DS}); T_C=25 °C; D=0; parameter: t_p

Diagram 4: Max. transient thermal impedance



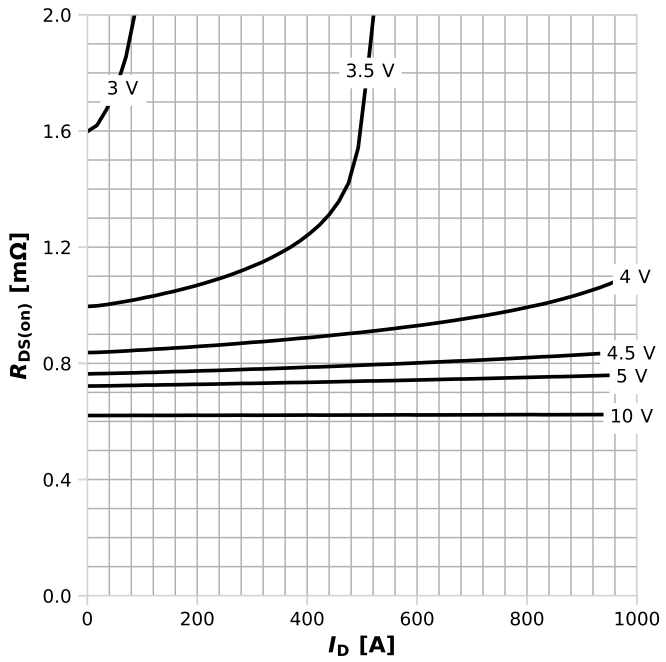
Z_{thJC}=f(t_p); parameter: D=t_p/T

Diagram 5: Typ. output characteristics



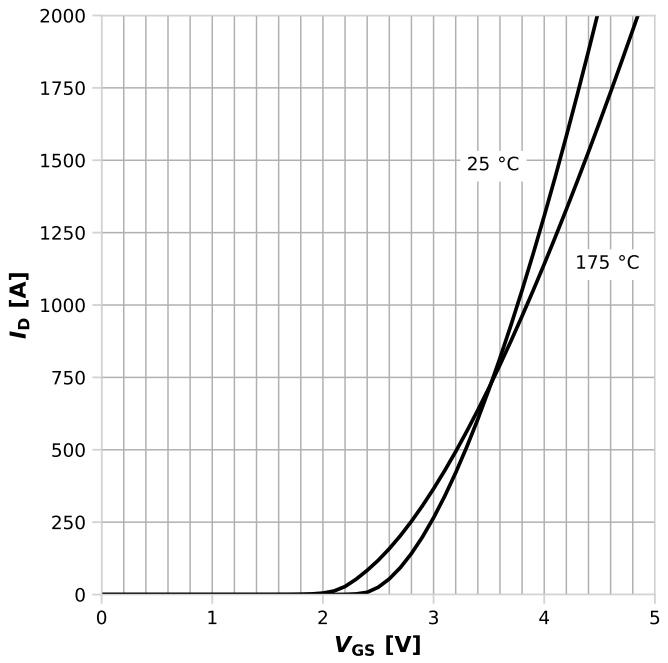
I_D=f(V_{DS}), T_j=25 °C; parameter: V_{GS}

Diagram 6: Typ. drain-source on resistance



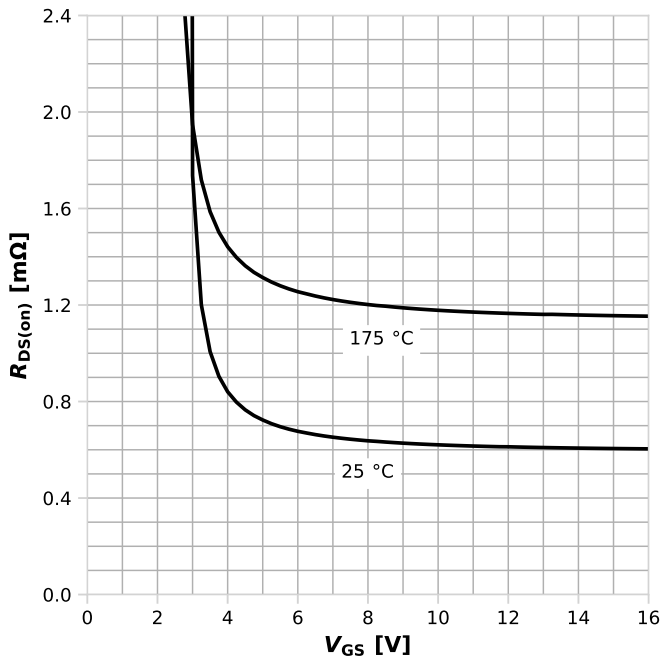
$R_{DS(on)}$=f(I_D), T_j=25 °C; parameter: V_{GS}

Diagram 7: Typ. transfer characteristics



I_D=f(V_{GS}), |V_{DS}|>2|I_D|$R_{DS(on)max}$; parameter: T_j

Diagram 8: Typ. drain-source on resistance



$R_{DS(on)}$=f(V_{GS}), I_D=50 A; parameter: T_j

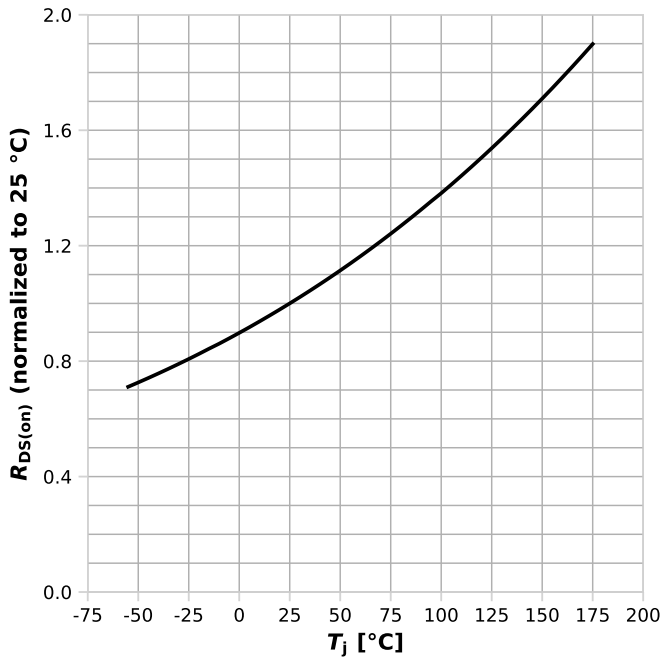
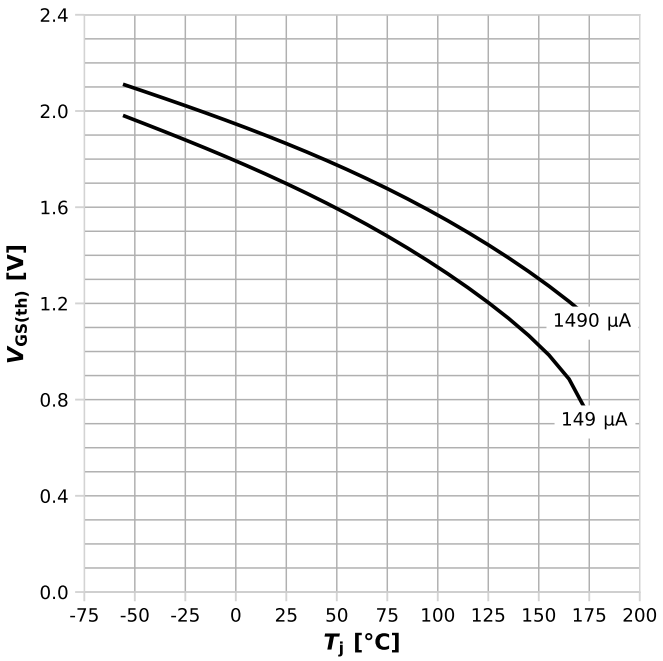
Diagram 9: Normalized drain-source on resistance	Diagram 10: Typ. gate threshold voltage
	
$R_{DS(on)}$=f(T_j), I_D=50 A, V_{GS}=10 V	$V_{GS(th)}$=f(T_j), V_{GS}=V_{DS}; parameter: I_D

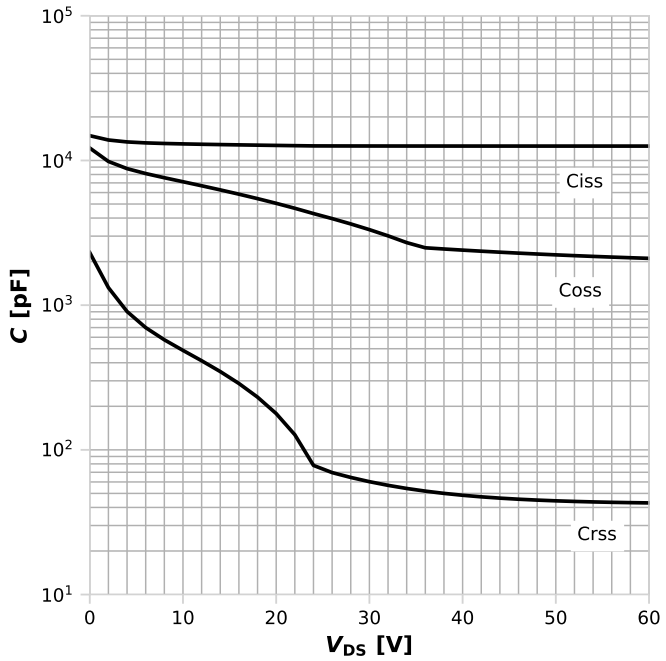
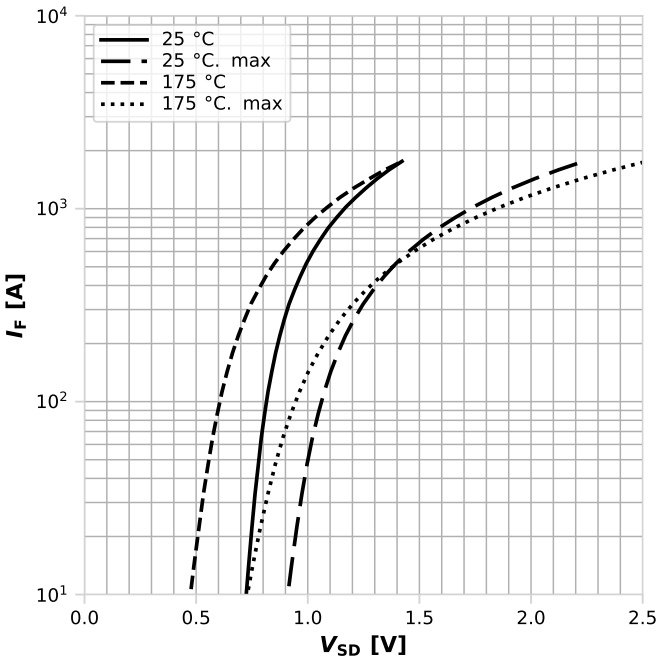
Diagram 11: Typ. capacitances	Diagram 12: Forward characteristics of reverse diode
	
C=f(V_{DS}); V_{GS}=0 V; f=1 MHz	I_F=f(V_{SD}); parameter: T_j

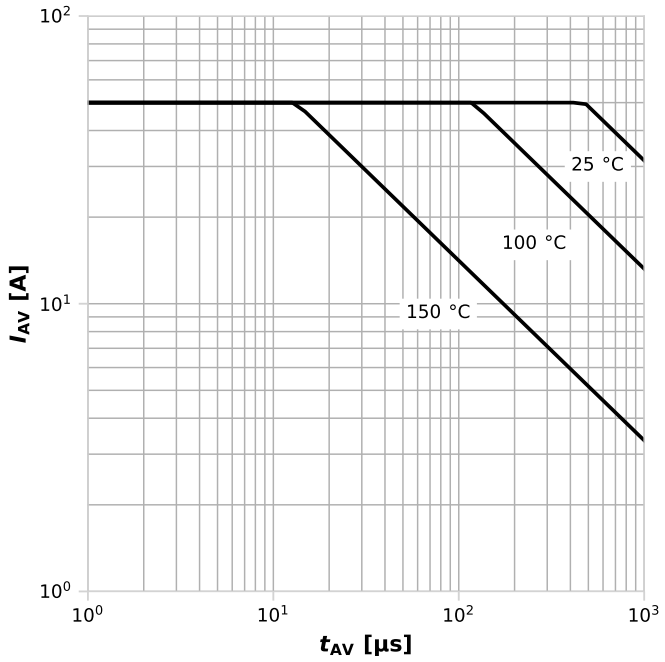
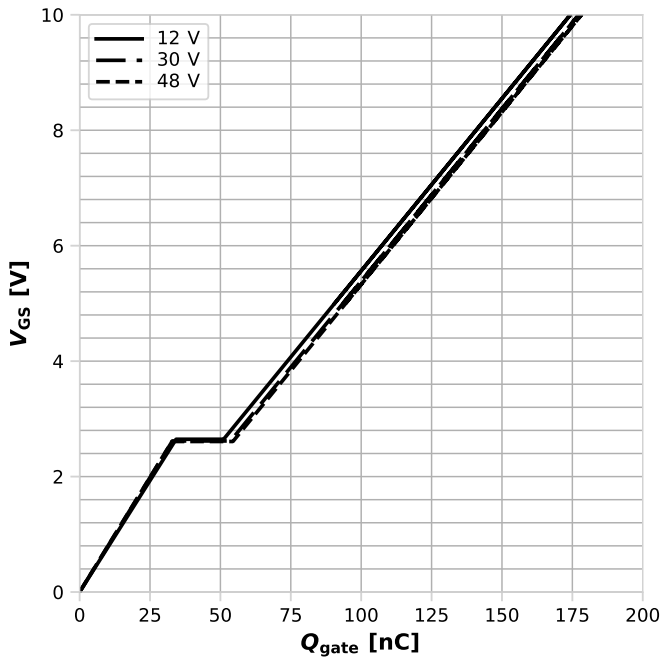
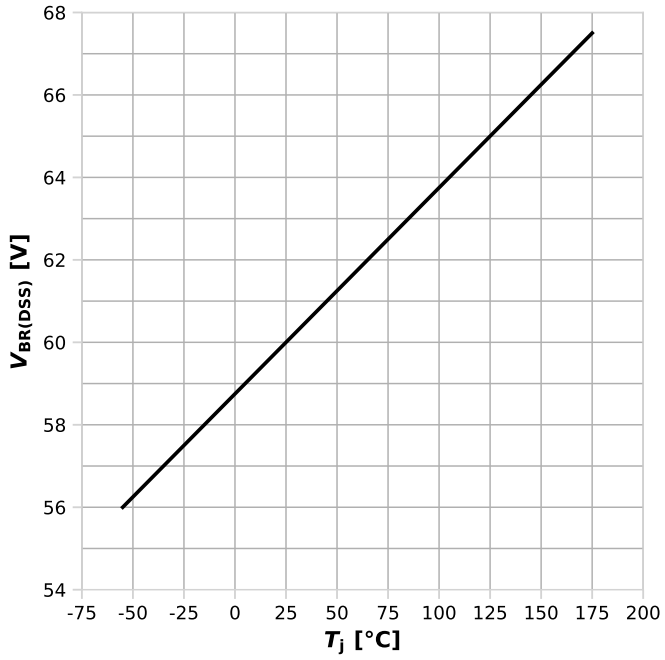
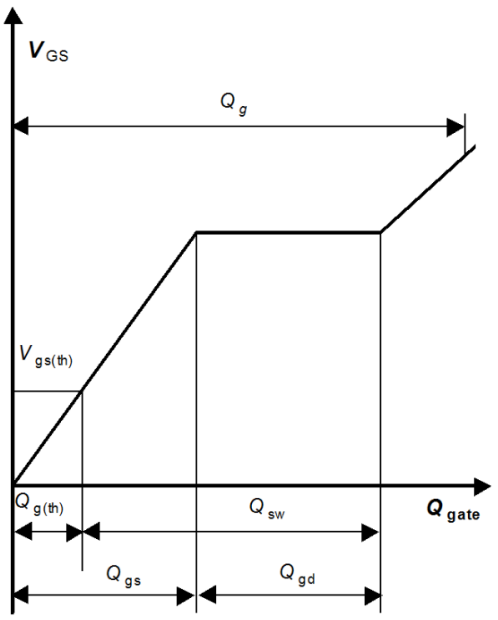
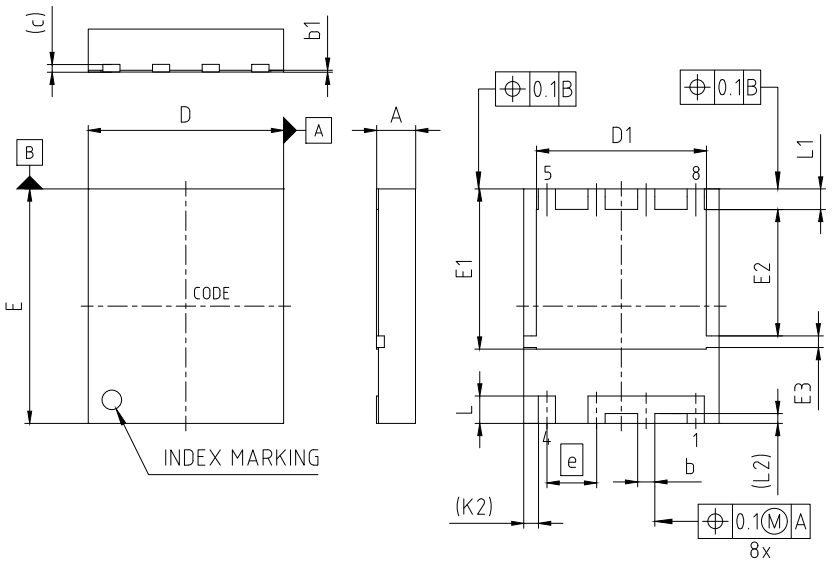
Diagram 13: Avalanche characteristics	Diagram 14: Typ. gate charge
	
I_{AS}=f(t_{AV}); R_{GS}=25 Ω; parameter: $T_{j,start}$	V_{GS}=f(Q_{gate}), I_D=50 A pulsed, T_j=25 °C; parameter: V_{DD}

Diagram 15: Min. drain-source breakdown voltage	Gate charge waveforms
	
$V_{BR(DSS)}$=f(T_j); I_D=10 mA	-

5 Package outlines



PACKAGE - GROUP NUMBER:	PG-TSON-8-U05	
DIMENSION	MILLIMETERS	
	MIN.	MAX.
A	0.90	1.10
b	0.34	0.54
b1	0.00	0.05
c	0.20	
D	4.90	5.10
D1	4.25	4.45
E	5.90	6.10
E1	4.00	4.20
E2	3.14	3.34
E3	0.20	0.40
e	1.27	
K2	0.38	
L	0.60	0.80
L1	0.43	0.63
L2	0.25	

NOTE: DIMENSIONS DO NOT INCLUDE MOLD FLASH, PROTRUSION OR GATE BURRS

Figure 1 Outline PG-TSON-8, dimensions in mm

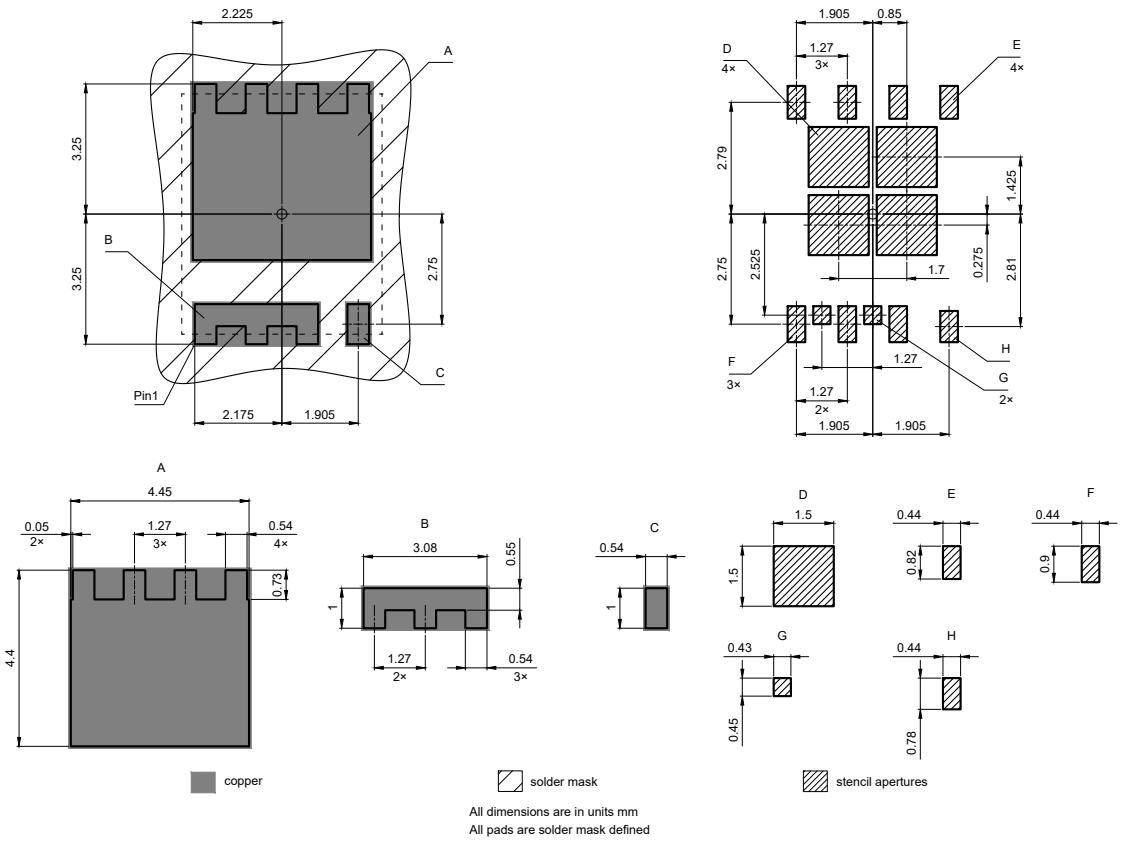


Figure 2 Footprint drawing PG-TSON-8, dimensions in mm

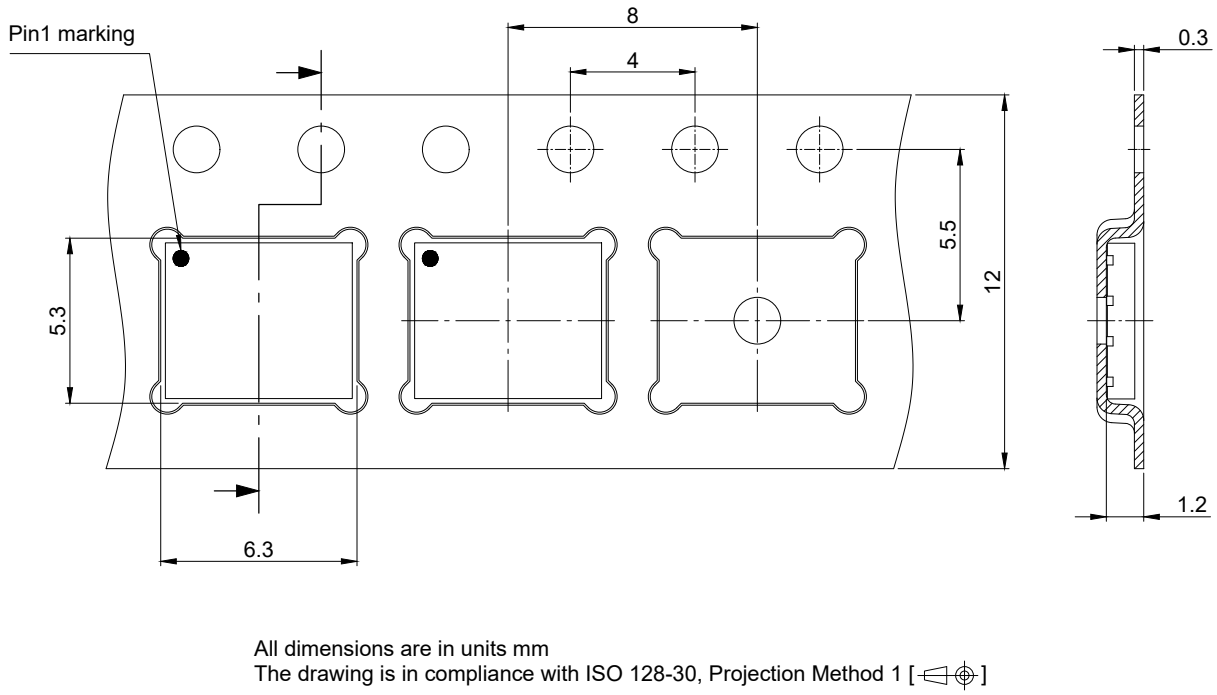


Figure 3 Packaging variant PG-TSON-8, dimensions in mm

Revision history

ISC007N06LM6

Revision 2025-03-24, Rev. 2.1

Previous revisions

Revision	Date	Subjects (major changes since last revision)
2.0	2024-05-07	Release of final
2.1	2025-03-24	Updated POD index misalignment against outline

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