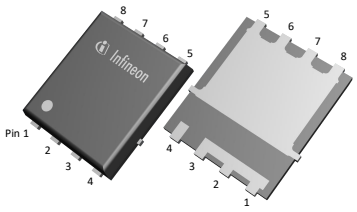
MOSFET

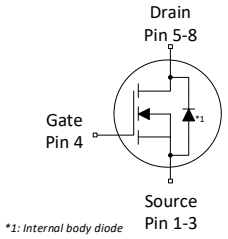
PG-TDSON-8

OptiMOS™ 6 Power-Transistor, 60 V



Features

- Optimized for high performance SMPS
- Optimized for Synchronous rectification
- N-channel, logic level
- Very low on-resistance $R_{DS(on)}$
- Superior thermal resistance
- 100% avalanche tested
- Pb-free lead plating; RoHS compliant
- Halogen-free according to IEC61249-2-21



Product validation

Fully qualified according to JEDEC for Industrial Applications

Table 1 Key Performance Parameters

Parameter	Value	Unit
V_{DS}	60	V
$R_{DS(on),max}$	0.8	mΩ
I_D	378	A
Q_{oss}	151	nC
Q_G	68	nC
Q_{rr} (1000A/µs)	277	nC

Type/Ordering Code	Package	Marking	Related Links
ISC008N06LM6	PG-TDSON-8	008N06L6	-

Table of Contents

Description 1
Maximum ratings 3
Thermal characteristics 3
Electrical characteristics 4
Electrical characteristics diagrams 6
Package Outlines 10
Revision History 14
Trademarks 14
Disclaimer 14

1 Maximum ratings

unless otherwise specified

Table 2 Maximum ratings

Parameter	Symbol	Values			Unit	Note/ Test Condition
		Min.	Typ.	Max.		
Continuous drain current [1]	I_D	-	-	378 268 229 44	A	V_{GS}=10 V, T_C=25 °C V_{GS}=10 V, T_C=100 °C V_{GS}=4.5 V, T_C=100 °C V_{GS}=10 V, T_A=25 °C, R_{thJA}=50 °C/W [2]
Pulsed drain current [3]	$I_{D,pulse}$	-	-	1512	A	T_C=25 °C
Avalanche energy, single pulse [4]	E_{AS}	-	-	583	mJ	I_D=50 A, R_{GS}=25 Ω
Gate source voltage	V_{GS}	-20	-	20	V	-
Power dissipation	P_{tot}	-	-	221 3.0	W	T_C=25 °C T_A=25 °C, R_{thJA}=50 °C/W [2]
Operating and storage temperature	T_j, T_{stg}	-55	-	175	°C	-

[1] Rating refers to the product only with datasheet specified absolute maximum values, maintaining case temperature as specified. For other case temperatures please refer to Diagram 2. De-rating will be required based on the actual environmental conditions.

[2] Device on 40 mm x 40 mm x 1.5 mm epoxy PCB FR4 with 6 cm^2 (one layer, 70 µm thick) copper area for drain connection. PCB is vertical in still air.

[3] See Diagram 3 for more detailed information

[4] See Diagram 13 for more detailed information

2 Thermal characteristics

Table 3 Thermal characteristics

Parameter	Symbol	Values			Unit	Note/ Test Condition
		Min.	Typ.	Max.		
Thermal resistance, junction - case, bottom	R_{thJC}	-	0.34	0.68	°C/W	-
Thermal resistance, junction - case, top	R_{thJC}	-	-	20	°C/W	-
Thermal resistance, junction - ambient, 6 cm^2 cooling area [5]	R_{thJA}	-	-	50	°C/W	-

[5] Device on 40 mm x 40 mm x 1.5 mm epoxy PCB FR4 with 6 cm^2 (one layer, 70 µm thick) copper area for drain connection. PCB is vertical in still air.

3 Electrical characteristics

unless otherwise specified

Table 4 Static characteristics

Parameter	Symbol	Values			Unit	Note/ Test Condition
		Min.	Typ.	Max.		
Drain-source breakdown voltage	$V_{(BR)DSS}$	60	-	-	V	V_{GS}=0 V, I_D=1 mA
Gate threshold voltage	$V_{GS(th)}$	1.1	1.7	2.3	V	V_{DS}=V_{GS}, I_D=118 µA
Zero gate voltage drain current	I_{DSS}	-	0.1 10	1.0 100	µA	V_{DS}=48 V, V_{GS}=0 V, T_j=25 °C V_{DS}=48 V, V_{GS}=0 V, T_j=125 °C
Gate-source leakage current	I_{GSS}	-	10	100	nA	V_{GS}=20 V, V_{DS}=0 V
Drain-source on-state resistance	$R_{DS(on)}$	-	0.73 0.92	0.8 1.1	mΩ	V_{GS}=10 V, I_D=50 A V_{GS}=4.5 V, I_D=25 A
Gate resistance	R_G	-	0.84	-	Ω	-
Transconductance [6]	g_{fs}	150	300	-	S	$\|V_{DS}\|\geq 2\|I_D\|R_{DS(on)max}$, I_D=50 A

[6] Defined by design. Not subject to production test.

Table 5 Dynamic characteristics

Parameter	Symbol	Values			Unit	Note/ Test Condition
		Min.	Typ.	Max.		
Input capacitance [7]	C_{iss}	-	10000	13000	pF	V_{GS}=0 V, V_{DS}=30 V, f=1 MHz
Output capacitance [7]	C_{oss}	-	2600	3400	pF	V_{GS}=0 V, V_{DS}=30 V, f=1 MHz
Reverse transfer capacitance [7]	C_{rss}	-	50	88	pF	V_{GS}=0 V, V_{DS}=30 V, f=1 MHz
Turn-on delay time	$t_{d(on)}$	-	12.5	-	ns	V_{DD}=30 V, V_{GS}=10 V, I_D=50 A, $R_{G,ext}$=1.6 Ω
Rise time	t_r	-	4.8	-	ns	V_{DD}=30 V, V_{GS}=10 V, I_D=50 A, $R_{G,ext}$=1.6 Ω
Turn-off delay time	$t_{d(off)}$	-	48.2	-	ns	V_{DD}=30 V, V_{GS}=10 V, I_D=50 A, $R_{G,ext}$=1.6 Ω
Fall time	t_f	-	7.4	-	ns	V_{DD}=30 V, V_{GS}=10 V, I_D=50 A, $R_{G,ext}$=1.6 Ω

[7] Defined by design. Not subject to production test.

Table 6 Gate charge characteristics [8)]

Parameter	Symbol	Values			Unit	Note/ Test Condition
		Min.	Typ.	Max.		
Gate to source charge	Q_{gs}	-	26	-	nC	V_{DD}=30 V, I_D=50 A, V_{GS}=0 to 4.5 V
Gate charge at threshold	$Q_{g(th)}$	-	17	-	nC	V_{DD}=30 V, I_D=50 A, V_{GS}=0 to 4.5 V
Gate to drain charge [9)]	Q_{gd}	-	17	25	nC	V_{DD}=30 V, I_D=50 A, V_{GS}=0 to 4.5 V
Switching charge	Q_{sw}	-	26	-	nC	V_{DD}=30 V, I_D=50 A, V_{GS}=0 to 4.5 V
Gate charge total [9)]	Q_g	-	68	85	nC	V_{DD}=30 V, I_D=50 A, V_{GS}=0 to 4.5 V
Gate plateau voltage	$V_{plateau}$	-	2.7	-	V	V_{DD}=30 V, I_D=50 A, V_{GS}=0 to 4.5 V
Gate charge total [9)]	Q_g	-	141	188	nC	V_{DD}=30 V, I_D=50 A, V_{GS}=0 to 10 V
Output charge [9)]	Q_{oss}	-	151	201	nC	V_{DS}=30 V, V_{GS}=0 V

8) See "Gate charge waveforms" for parameter definition

9) Defined by design. Not subject to production test.

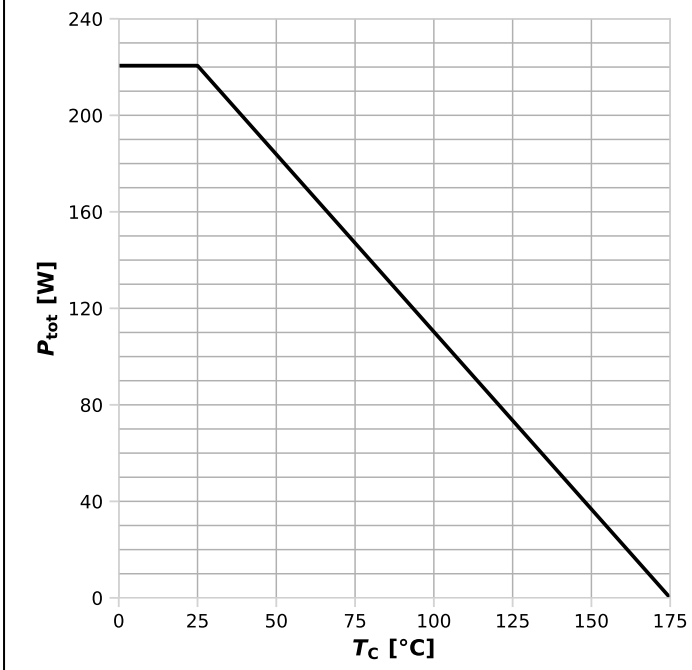
Table 7 Reverse diode

Parameter	Symbol	Values			Unit	Note/ Test Condition
		Min.	Typ.	Max.		
Diode continuous forward current	I_S	-	-	201	A	T_C=25 °C
Diode pulse current	$I_{S,pulse}$	-	-	1512	A	T_C=25 °C
Diode forward voltage	V_{SD}	-	0.79	1.0	V	V_{GS}=0 V, I_F=50 A, T_j=25 °C
Reverse recovery time [10)]	t_{rr}	-	60	120	ns	V_R=30 V, I_F=50 A, di_F/dt=100 A/µs
Reverse recovery charge [10)]	Q_{rr}	-	90	180	nC	V_R=30 V, I_F=50 A, di_F/dt=100 A/µs
Reverse recovery time [10)]	t_{rr}	-	30	60	ns	V_R=30 V, I_F=50 A, di_F/dt=1000 A/µs
Reverse recovery charge [10)]	Q_{rr}	-	277	554	nC	V_R=30 V, I_F=50 A, di_F/dt=1000 A/µs

10) Defined by design. Not subject to production test.

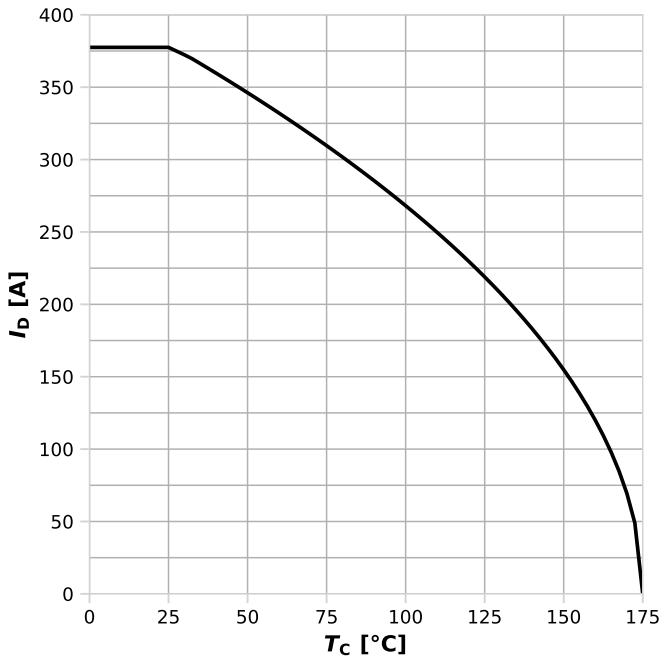
4 Electrical characteristics diagrams

Diagram 1: Power dissipation



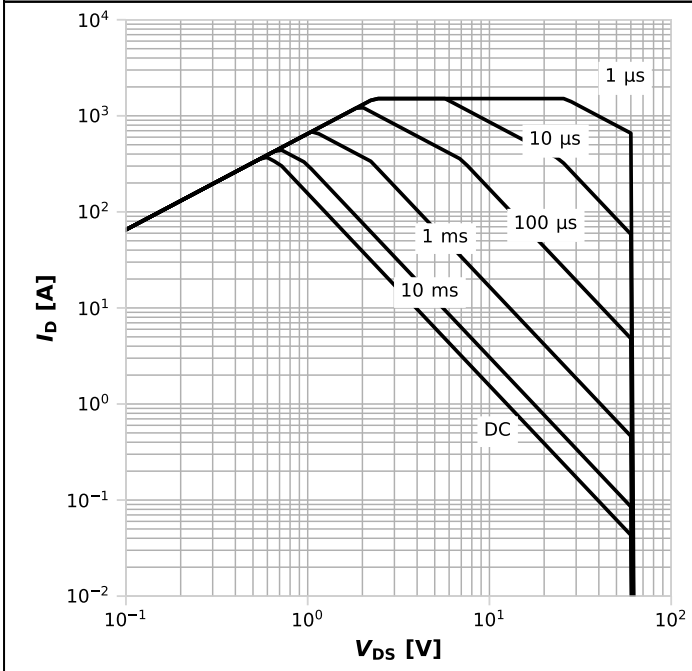
P_{tot}=f(T_C)

Diagram 2: Drain current



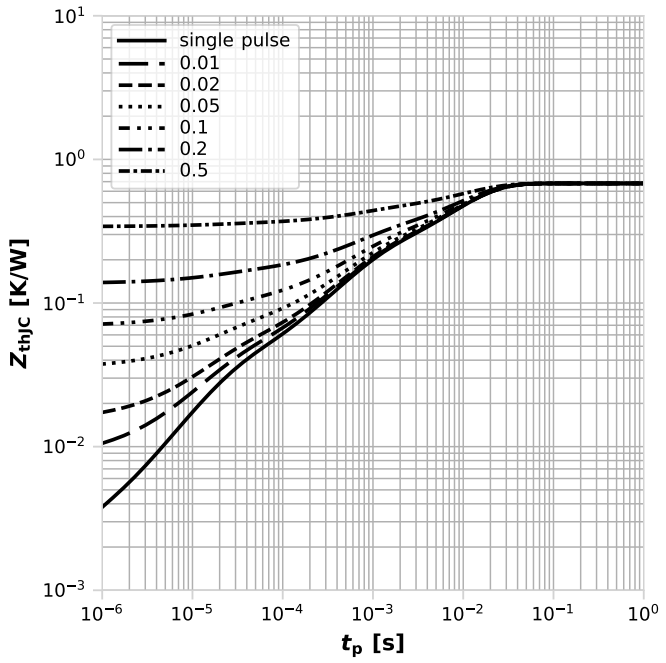
I_D=f(T_C); V_{GS}≥10 V

Diagram 3: Safe operating area



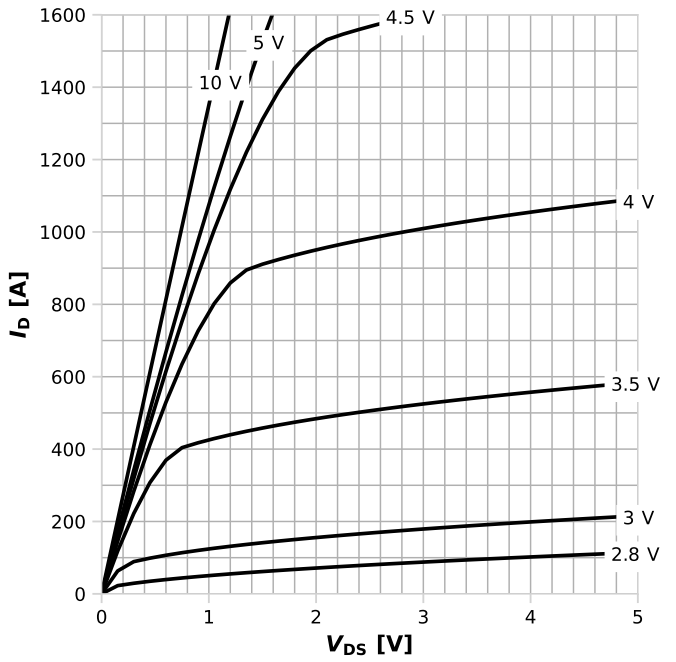
I_D=f(V_{DS}); T_C=25 °C; D=0; parameter: t_p

Diagram 4: Max. transient thermal impedance



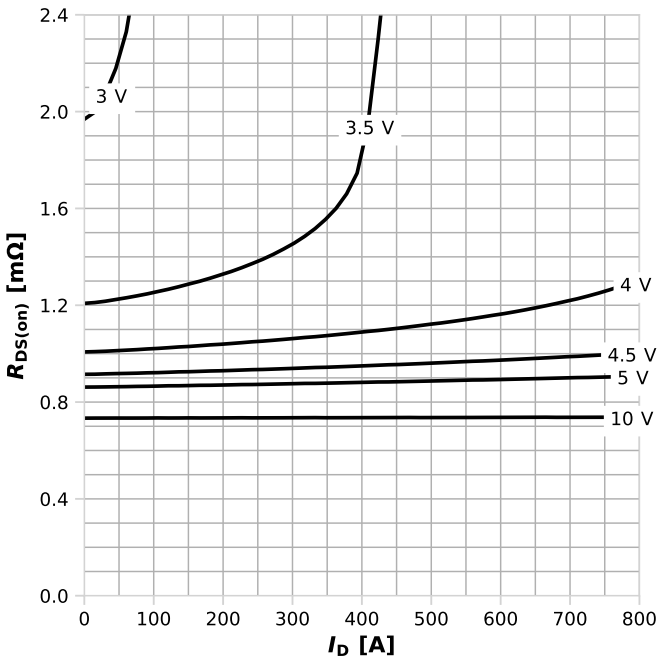
Z_{thJC}=f(t_p); parameter: D=t_p/T

Diagram 5: Typ. output characteristics



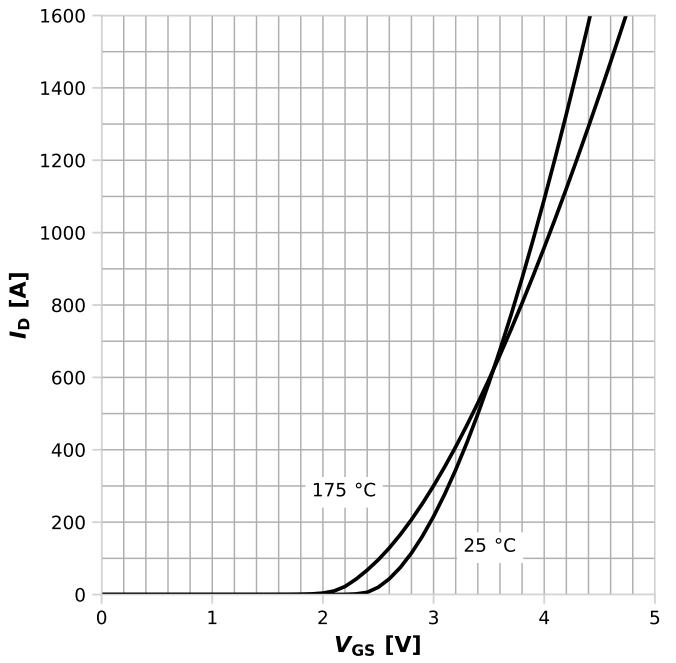
I_D=f(V_{DS}), T_j=25 °C; parameter: V_{GS}

Diagram 6: Typ. drain-source on resistance



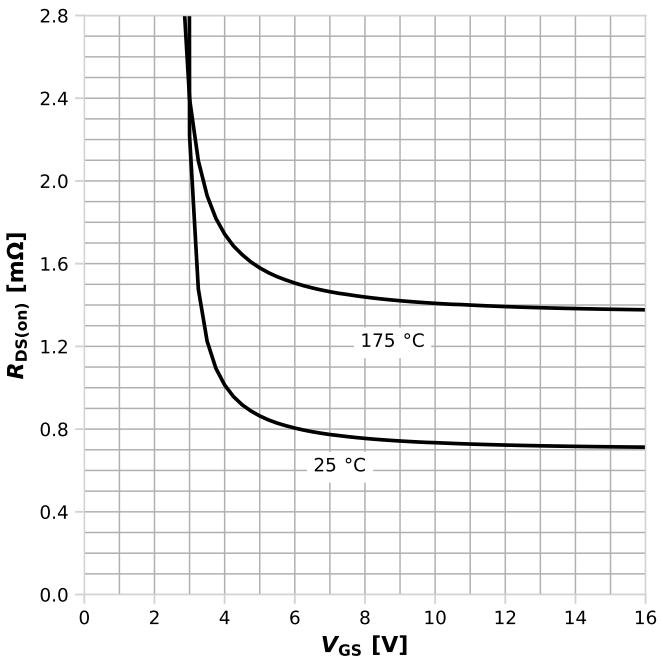
$R_{DS(on)}$=f(I_D), T_j=25 °C; parameter: V_{GS}

Diagram 7: Typ. transfer characteristics



I_D=f(V_{GS}), $|V_{DS}|>2|I_D|R_{DS(on)max}$; parameter: T_j

Diagram 8: Typ. drain-source on resistance



$R_{DS(on)}$=f(V_{GS}), I_D=50 A; parameter: T_j

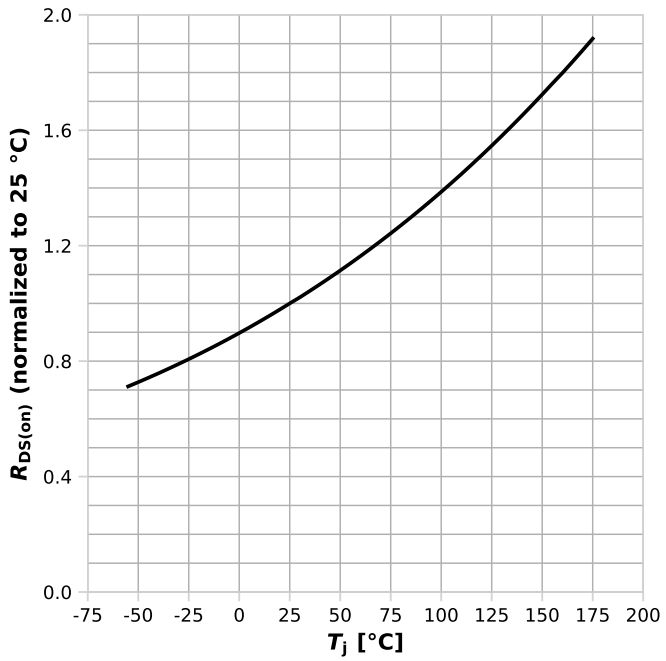
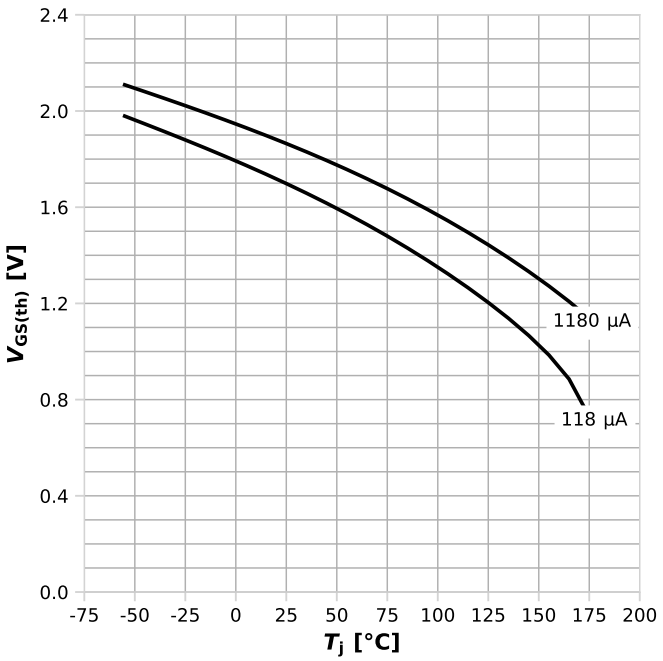
Diagram 9: Normalized drain-source on resistance	Diagram 10: Typ. gate threshold voltage
	
$R_{DS(on)}$=f(T_j), I_D=50 A, V_{GS}=10 V	$V_{GS(th)}$=f(T_j), V_{GS}=V_{DS}; parameter: I_D

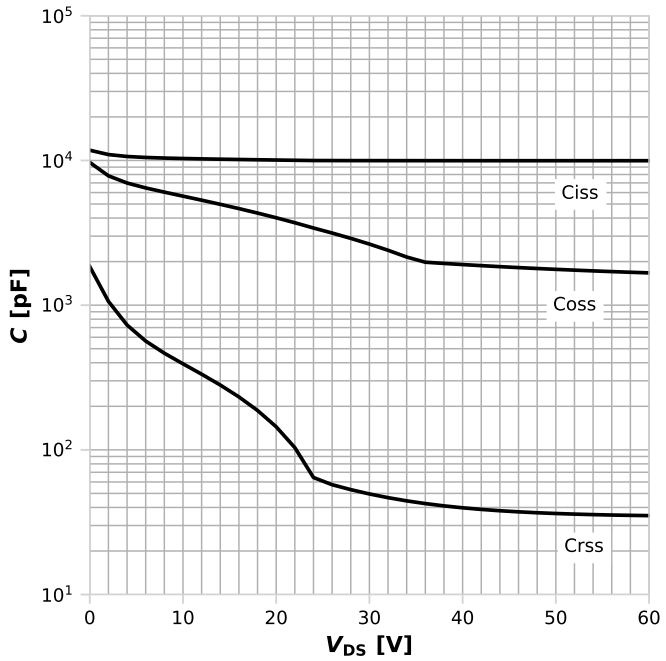
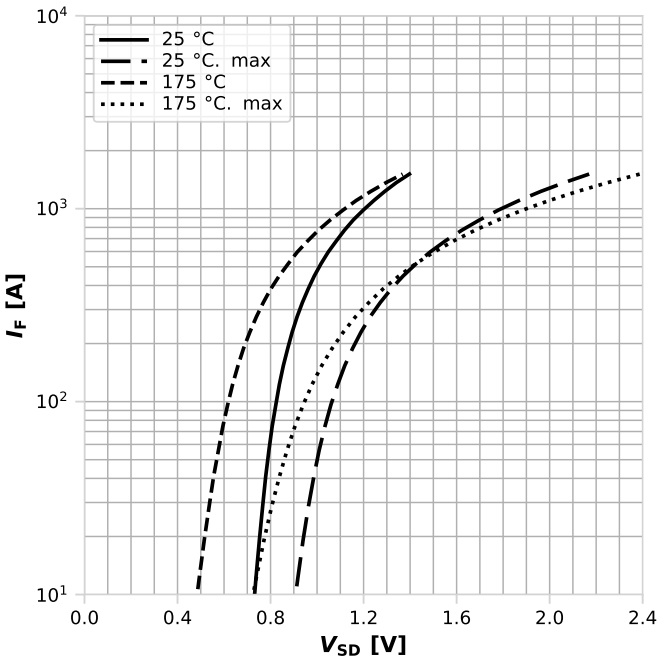
Diagram 11: Typ. capacitances	Diagram 12: Forward characteristics of reverse diode
	
C=f(V_{DS}); V_{GS}=0 V; f=1 MHz	I_F=f(V_{SD}); parameter: T_j

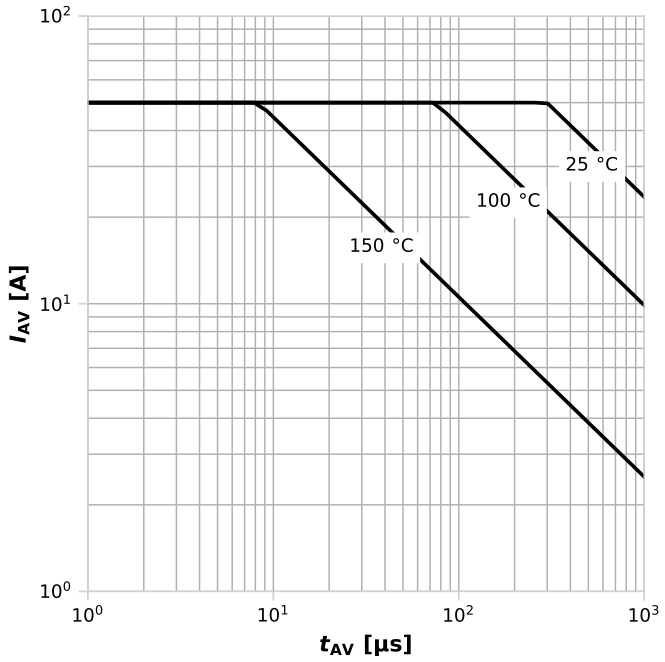
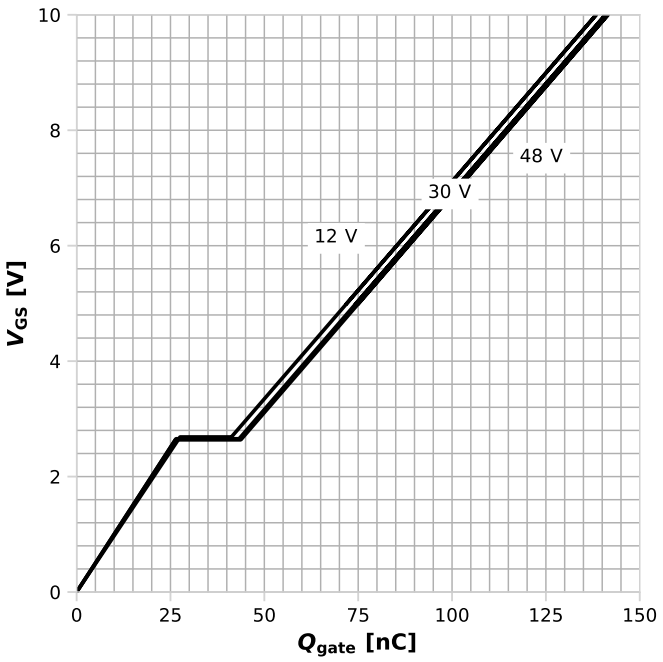
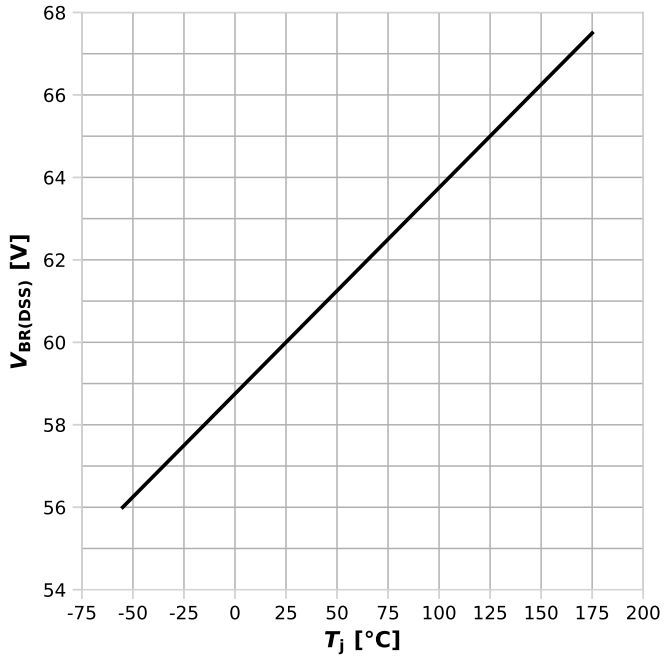
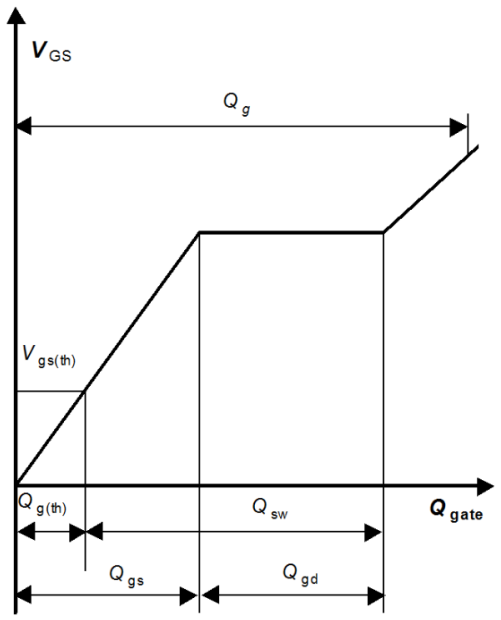
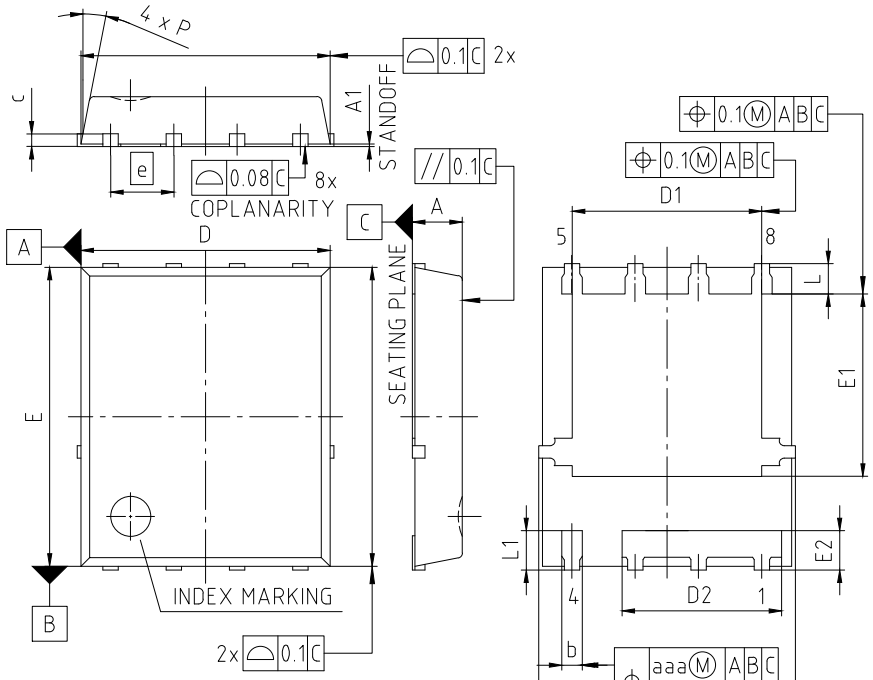
Diagram 13: Avalanche characteristics	Diagram 14: Typ. gate charge
	
I_{AS}=f(t_{AV}); R_{GS}=25 Ω; parameter: $T_{j,start}$	V_{GS}=f(Q_{gate}), I_D=50 A pulsed, T_j=25 °C; parameter: V_{DD}

Diagram 15: Min. drain-source breakdown voltage	Gate charge waveforms
	
$V_{BR(DSS)}$=f(T_j); I_D=10 mA	-

5 Package Outlines



PACKAGE - GROUP NUMBER:	PG-TDSON-8-U04	
DIMENSIONS	MILLIMETERS	
	MIN.	MAX.
A	0.90	1.20
A1	0	0.05
b	0.26	0.54
c	0.15	0.35
D	4.80	5.35
D1	3.70	4.40
D2	2.94	3.25
D3	4.80	5.15
E	5.70	6.10
E1	3.40	3.76
E2	0.69	0.90
e	1.27	
L	0.45	0.72
L1	0.69	0.90
aaa	0.10	0.25
P	8°	12°

1) EXCLUDING MOLD FLASH
2) REMOVAL ON MOLD GATE
   INTRUSION 0.1 MM
   PROTRUSION 0.1 MM
3) LEAD LENGTH UP TO ANTI FLASH LINE
4) ALL METAL SURFACES ARE PLATED,
   EXCEPT AREA OF CUT

Figure 1 Outline PG-TDSON-8, dimensions in mm

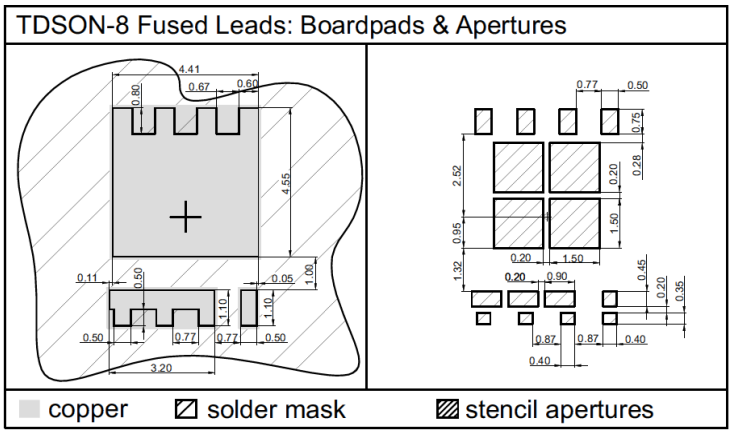


Figure 2 Outline PG-TDSON-8, dimensions in mm

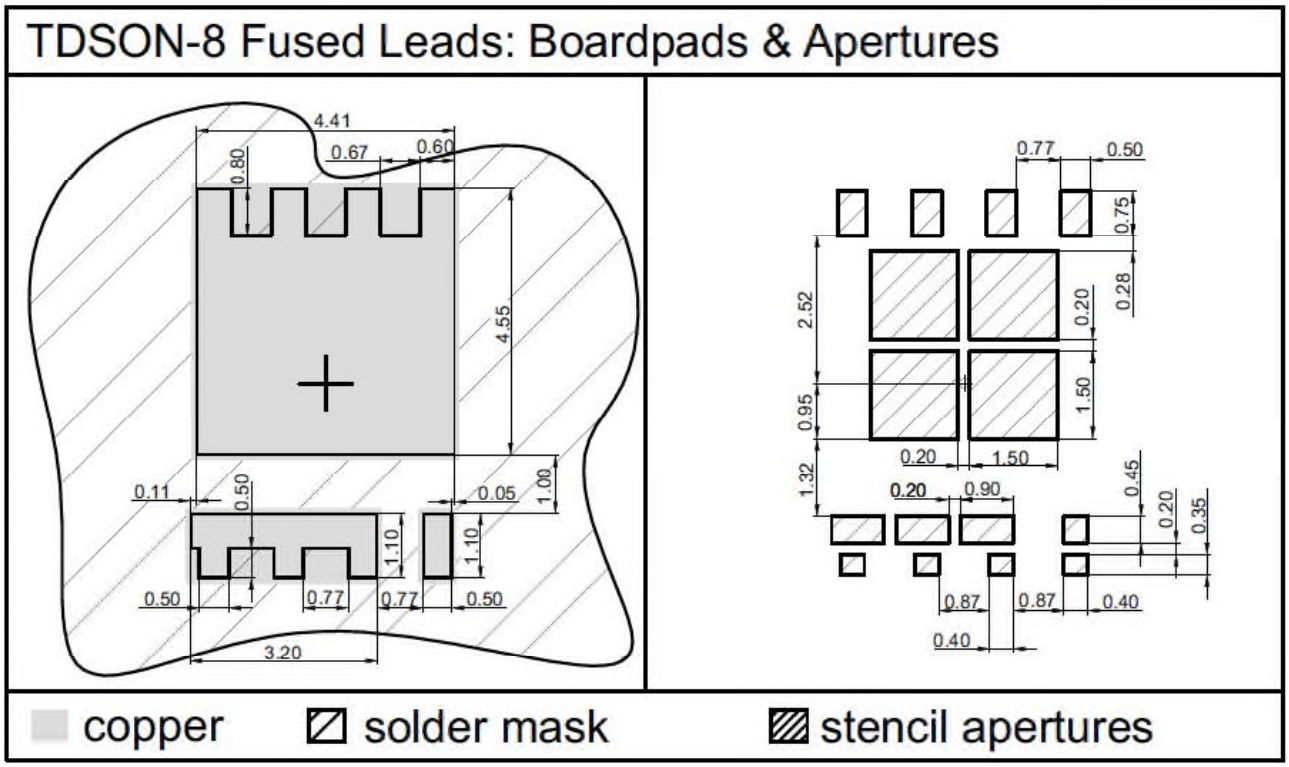


Figure 3 Outline PG-TDSON-8, dimensions in mm

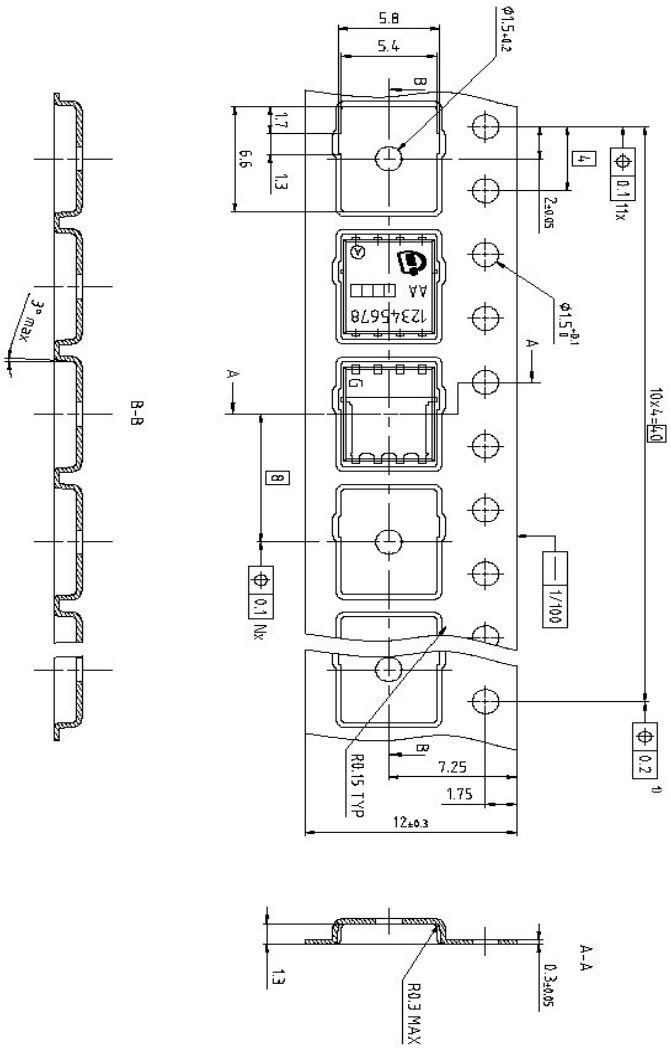


Figure 4 Outline PG-TDSON-8, dimensions in mm

Revision History

ISC008N06LM6

Revision 2024-05-07, Rev. 2.0

Previous Revision

Revision	Date	Subjects (major changes since last revision)
2.0	2024-05-07	Release of final

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