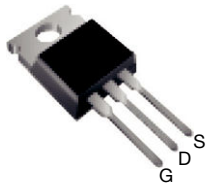
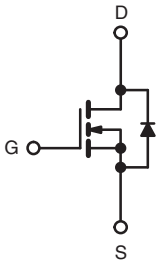
D Series Power MOSFET

PRODUCT SUMMARY		
V_{DS} (V) at T_J max.	450	
$R_{DS(on)}$ max. at 25 °C (Ω)	V_{GS} = 10 V	1.0
Q_g max. (nC)	18	
Q_{gs} (nC)	3	
Q_{gd} (nC)	4	
Configuration	Single	

TO-220AB





N-Channel MOSFET

FEATURES

- Optimal Design
  - Low Area Specific On-Resistance
  - Low Input Capacitance (C_{iss})
  - Reduced Capacitive Switching Losses
  - High Body Diode Ruggedness
  - Avalanche Energy Rated (UIS)
- Optimal Efficiency and Operation
  - Low Cost
  - Simple Gate Drive Circuitry
  - Low Figure-of-Merit (FOM): R_{on} x Q_g
  - Fast Switching
- Material categorization: For definitions of compliance please see www.vishay.com/doc?99912

RoHS* COMPLIANT

Note

* Lead (Pb)-containing terminations are not RoHS-compliant. Exemptions may apply.

APPLICATIONS

- Consumer Electronics
  - Displays (LCD or Plasma TV)
- Server and Telecom Power Supplies
  - SMPS
- Industrial
  - Welding
  - Induction Heating
- Motor Drives
- Battery Chargers

ORDERING INFORMATION	
Package	TO-220AB
Lead (Pb)-free	IRF730BPbF

ABSOLUTE MAXIMUM RATINGS (T_C = 25 °C, unless otherwise noted)

PARAMETER			SYMBOL	LIMIT	UNIT
Drain-Source Voltage			V_{DS}	400	V
Gate-Source Voltage			V_{GS}	± 30	
Gate-Source Voltage AC (f > 1 Hz)				30	
Continuous Drain Current (T_J = 150 °C)	V_{GS} at 10 V	T_C = 25 °C	I_D	6	A
		T_C = 100 °C		4	
Pulsed Drain Current[a]			I_{DM}	13	
Linear Derating Factor				0.8	W/°C
Single Pulse Avalanche Energy[b]			E_{AS}	104	mJ
Maximum Power Dissipation			P_D	104	W
Operating Junction and Storage Temperature Range			T_J, T_{stg}	- 55 to + 150	°C
Drain-Source Voltage Slope	T_J = 125 °C		dV/dt	24	V/ns
Reverse Diode dV/dt[d]				0.48	
Soldering Recommendations (Peak Temperature)	for 10 s			300[c]	°C

Notes

a. Repetitive rating; pulse width limited by maximum junction temperature.
b. V_{DD} = 50 V, starting T_J = 25 °C, L = 2.3 mH, R_g = 25 Ω, I_{AS} = 9.5 A.
c. 1.6 mm from case.
d. $I_{SD} \leq I_D$, starting T_J = 25 °C.

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THERMAL RESISTANCE RATINGS

PARAMETER	SYMBOL	TYP.	MAX.	UNIT
Maximum Junction-to-Ambient	R_{thJA}	-	62	°C/W
Maximum Junction-to-Case (Drain)	R_{thJC}	-	1.2	

SPECIFICATIONS (T_J = 25 °C, unless otherwise noted)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT
Static						
Drain-Source Breakdown Voltage	V_{DS}	V_{GS} = 0 V, I_D = 250 µA	400	-	-	V
V_{DS} Temperature Coefficient	$\Delta V_{DS}/T_J$	Reference to 25 °C, I_D = 250 µA	-	0.53	-	V/°C
Gate-Source Threshold Voltage (N)	$V_{GS(th)}$	V_{DS} = V_{GS}, I_D = 250 µA	3	-	5	V
Gate-Source Leakage	I_{GSS}	V_{GS} = ± 30 V	-	-	± 100	nA
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = 400 V, V_{GS} = 0 V	-	-	1	µA
		V_{DS} = 320 V, V_{GS} = 0 V, T_J = 125 °C	-	-	10	
Drain-Source On-State Resistance	$R_{DS(on)}$	V_{GS} = 10 V, I_D = 3 A	-	0.85	1.0	Ω
Forward Transconductance	g_{fs}	V_{DS} = 50 V, I_D = 3 A	-	1.7	-	S
Dynamic						
Input Capacitance	C_{iss}	V_{GS} = 0 V, V_{DS} = 100 V, f = 1 MHz	-	311	-	pF
Output Capacitance	C_{oss}		-	38	-	
Reverse Transfer Capacitance	C_{rss}		-	7	-	
Effective output capacitance, energy related[a]	$C_{o(er)}$	V_{GS} = 0 V, V_{DS} = 0 V to 320 V	-	44	-	
Effective output capacitance, time related[b]	$C_{o(tr)}$		-	54	-	
Total Gate Charge	Q_g	V_{GS} = 10 V, I_D = 3 A, V_{DS} = 320 V	-	9	18	nC
Gate-Source Charge	Q_{gs}		-	3	-	
Gate-Drain Charge	Q_{gd}		-	4	-	
Turn-On Delay Time	$t_{d(on)}$	V_{DD} = 400 V, I_D = 3 A, V_{GS} = 10 V, R_g = 9.1 Ω	-	12	24	ns
Rise Time	t_r		-	11	22	
Turn-Off Delay Time	$t_{d(off)}$		-	14	28	
Fall Time	t_f		-	8	16	
Gate Input Resistance	R_g	f = 1 MHz, open drain	-	1.9	-	Ω
Drain-Source Body Diode Characteristics						
Continuous Source-Drain Diode Current	I_S	MOSFET symbol showing the integral reverse p - n junction diode 	-	-	6	A
Pulsed Diode Forward Current	I_{SM}		-	-	24	
Diode Forward Voltage	V_{SD}	T_J = 25 °C, I_S = 3 A, V_{GS} = 0 V	-	-	1.2	V
Reverse Recovery Time	t_{rr}	T_J = 25 °C, I_F = I_S = 3 A, dI/dt = 100 A/µs, V_R = 20 V	-	236	-	ns
Reverse Recovery Charge	Q_{rr}		-	1.1	-	µC
Reverse Recovery Current	I_{RRM}		-	9	-	A

Notes

a. $C_{oss(er)}$ is a fixed capacitance that gives the same energy as C_{oss} while V_{DS} is rising from 0 % to 80 % V_{DS}.

b. $C_{oss(tr)}$ is a fixed capacitance that gives the same charging time as C_{oss} while V_{DS} is rising from 0 % to 80 % V_{DS}.

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TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)

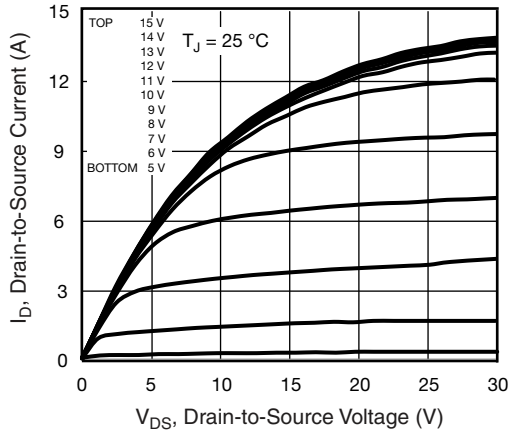


Fig. 1 - Typical Output Characteristics

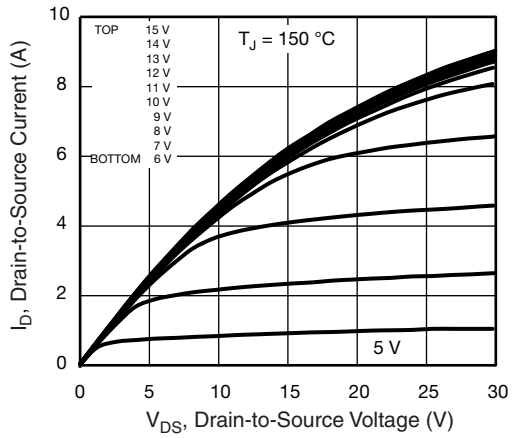


Fig. 2 - Typical Output Characteristics

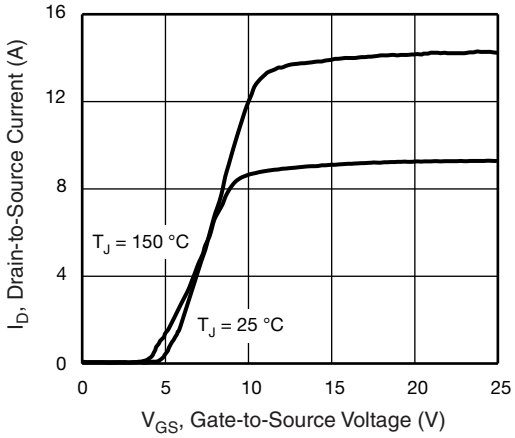


Fig. 3 - Typical Transfer Characteristics

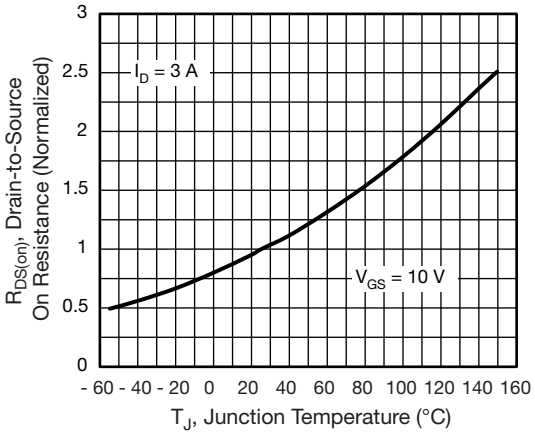


Fig. 4 - Normalized On-Resistance vs. Temperature

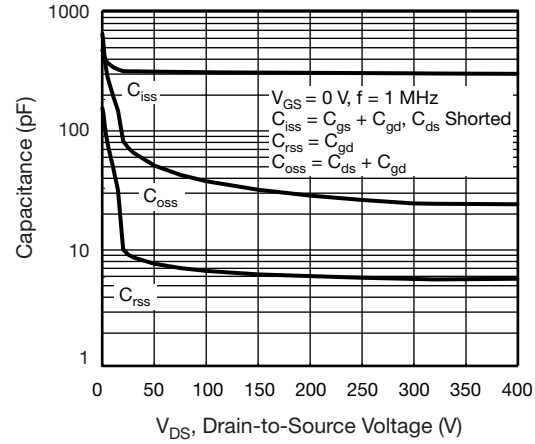


Fig. 5 - Typical Capacitance vs. Drain-to-Source Voltage

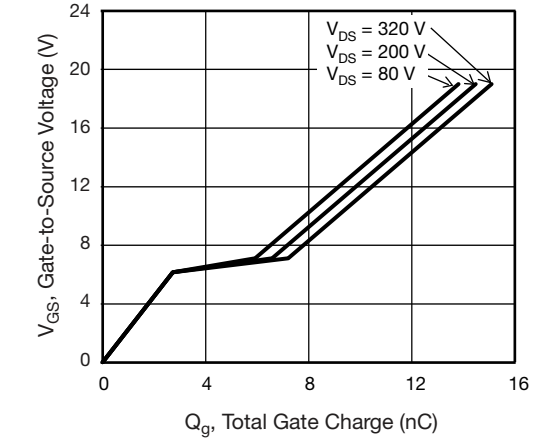


Fig. 6 - Typical Gate Charge vs. Gate-to-Source Voltage

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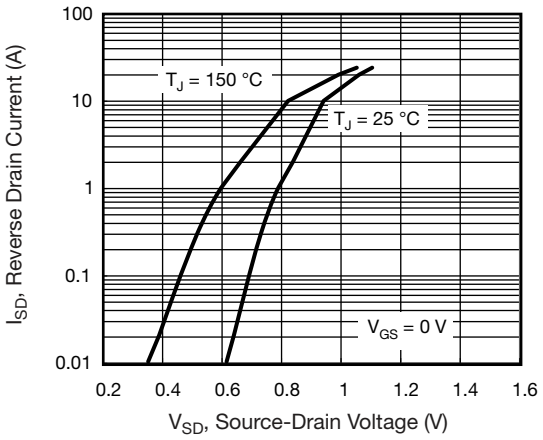


Fig. 7 - Typical Source-Drain Diode Forward Voltage

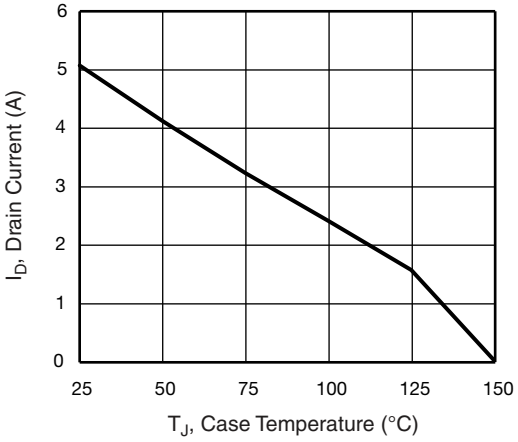


Fig. 9 - Maximum Drain Current vs. Case Temperature

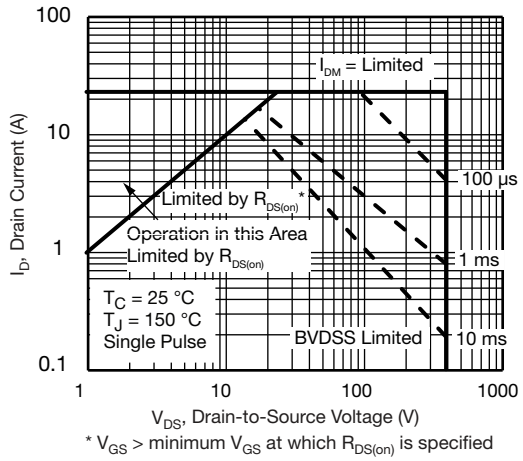


Fig. 8 - Maximum Safe Operating Area

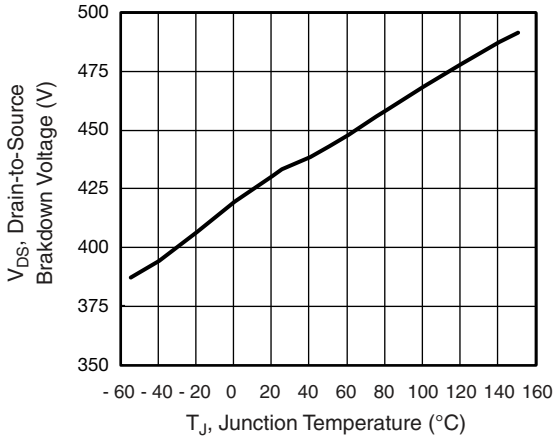


Fig. 10 - Temperature vs. Drain-to-Source Voltage

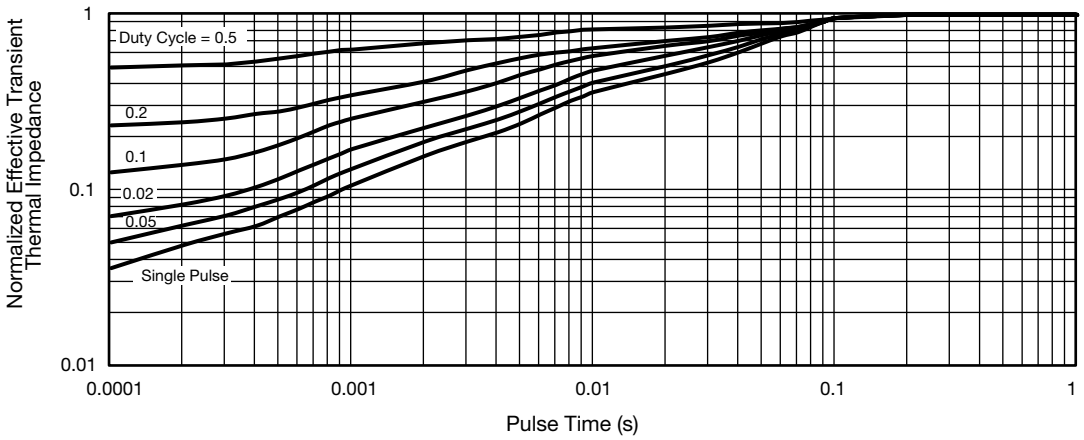


Fig. 11 - Normalized Thermal Transient Impedance, Junction-to-Case

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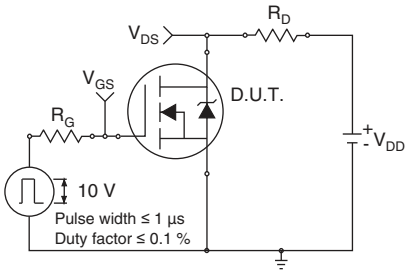


Fig. 12 - Switching Time Test Circuit

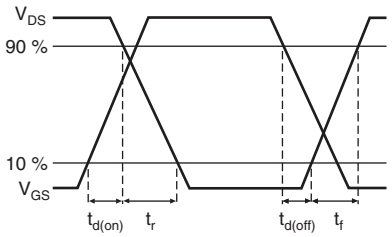


Fig. 13 - Switching Time Waveforms

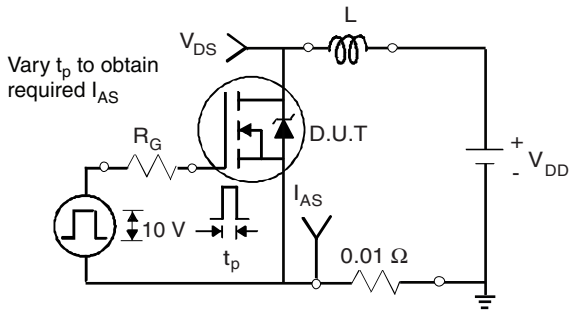


Fig. 14 - Unclamped Inductive Test Circuit

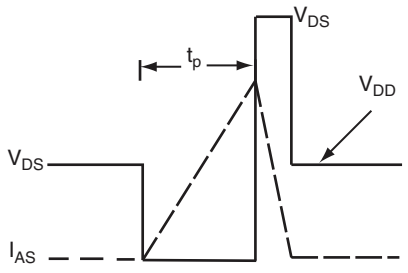


Fig. 15 - Unclamped Inductive Waveforms

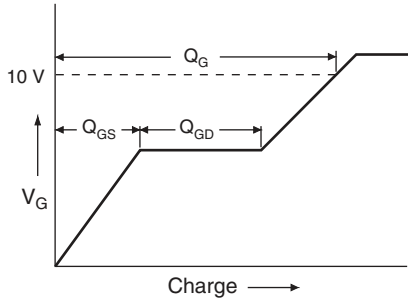


Fig. 16 - Basic Gate Charge Waveform

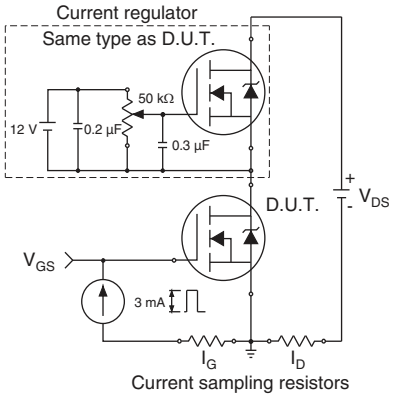
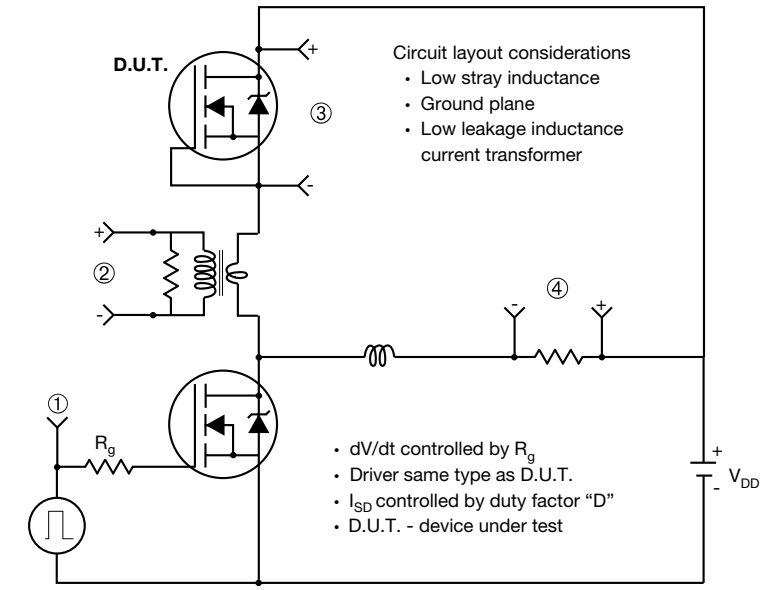
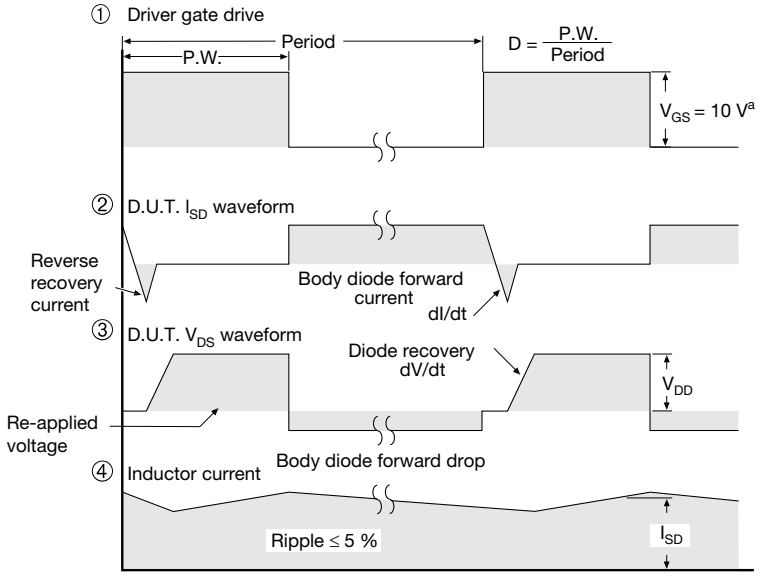


Fig. 17 - Gate Charge Test Circuit

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Peak Diode Recovery dV/dt Test Circuit





Note

a. V_{GS} = 5 V for logic level devices

Fig. 18 - For N-Channel

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