ISL78310

High Performance 1A LDO

FN7810
Rev 2.00
November 7, 2014

The ISL78310 is a low dropout voltage, high-current, single output LDO specified for 1A output current. This part operates from input voltages down to 2.2V and up to 6V. The part offers fixed and external resistor adjustable output voltages from 0.8V to 5V. Custom voltage options are available upon request.

For applications that desire to set the in-rush current to less than the current limit of the part, or for applications that require turn-on time control, an external capacitor can be placed on the soft-start pin for maximum control. A supply-independent ENABLE signal allows the part to be placed into a low quiescent current shutdown mode. Sub-micron CMOS process is used for this product family to deliver best-in-class analog performance and overall value.

This CMOS LDO consumes significant lower quiescent (ground pin) current as a function of load over bipolar LDOs, which translates into higher efficiency and packages with smaller footprints. Quiescent current is optimized to achieve a very fast load transient response.

The ISL78310 is AEC-Q100 rated. The ISL78310 is rated for the automotive temperature range (-40°C to +125°C).

Applications

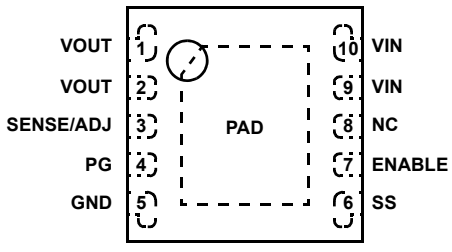
- Core & I/O power
- Camera modules
- Post regulation of switched supplies
- Radio systems
- Infotainment systems

Features

- 2.2V to 6V input supply
- 130mV dropout voltage typical (at 1A)
- Fast load transient response
- ±0.2% initial V_{OUT} accuracy
- Adjustable in-rush current limiting
- 58dB typical PSRR
- 63µV_{RMS} output noise at V_{OUT} = 1.8V
- Power-good feature
- 500mV feedback voltage
- Supply-independent 1V enable input threshold
- Short-circuit current protection
- 1A peak reverse current
- Over-temperature shutdown
- Any cap stable with minimum 10µF ceramic
- ±1.8% guaranteed V_{OUT} accuracy for junction temperature range from -40°C to +125°C
- Available in a 10 Lead DFN package
- Pb-free (RoHS compliant)
- AEC-Q100 qualified

Pin Configuration

ISL78310
(10 LD 3x3 DFN)
TOP VIEW



Pin Descriptions

PIN #	PIN NAME	DESCRIPTION
1, 2	VOUT	Regulated output voltage. A minimum 10µF X5R/X7R output capacitor is required for stability. See "External Capacitor Requirements" on page 9 for more details.
3	SENSE/ADJ	For internally fixed VOUT option, this pin provides output voltage feedback. By connecting this pin to the output rail at the load, small voltage drops caused by PCB trace resistance can be eliminated. For the adjustable output voltage option, this pin is connected to the feedback resistor divider and provides voltage feedback signals for the LDO to set the output voltage.
4	PG	This is an open drain logic output used to indicate the status of the output voltage. Logic low indicates VOUT is not in regulation. Must be grounded if not used.
5	GND	Ground.
6	SS	External capacitor on this pin adjusts start-up ramp and controls in-rush current.
7	ENABLE	VIN independent chip enable. TTL and CMOS compatible.
8	NC	Do not connect this pin to ground or supply. Leave floating.
9, 10	VIN	Input supply pin. A minimum 10µF X5R/X7R input capacitor is required for stability. See "External Capacitor Requirements" on page 9 for more details.
	EPAD	EPAD at ground potential. Soldering it directly to GND plane is required for thermal considerations. See "Heatsinking the DFN Package" on page 12 for more details.

Ordering Information

PART NUMBER (Notes 1, 3, 4)	PART MARKING	V_{OUT} VOLTAGE (Note 2)	TEMP RANGE (°C)	PACKAGE (Pb-Free)	PKG DWG. #
ISL78310ARAJZ	DZAE	ADJ	-40 to +125	10 Ld 3x3 DFN	L10.3x3

NOTES:

1. Add "-T*" suffix for tape and reel. Please refer to TB347 for details on reel specifications.
2. For other output voltages, contact Intersil Marketing.
3. These Intersil Pb-free plastic packaged products employ special Pb-free material sets, molding compounds/die attach materials, and 100% matte tin plate plus anneal (e3 termination finish, which is RoHS compliant and compatible with both SnPb and Pb-free soldering operations). Intersil Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J STD-020.
4. For Moisture Sensitivity Level (MSL), please see device information page for ISL78310. For more information on MSL please see techbrief TB363.

Typical Application Diagrams

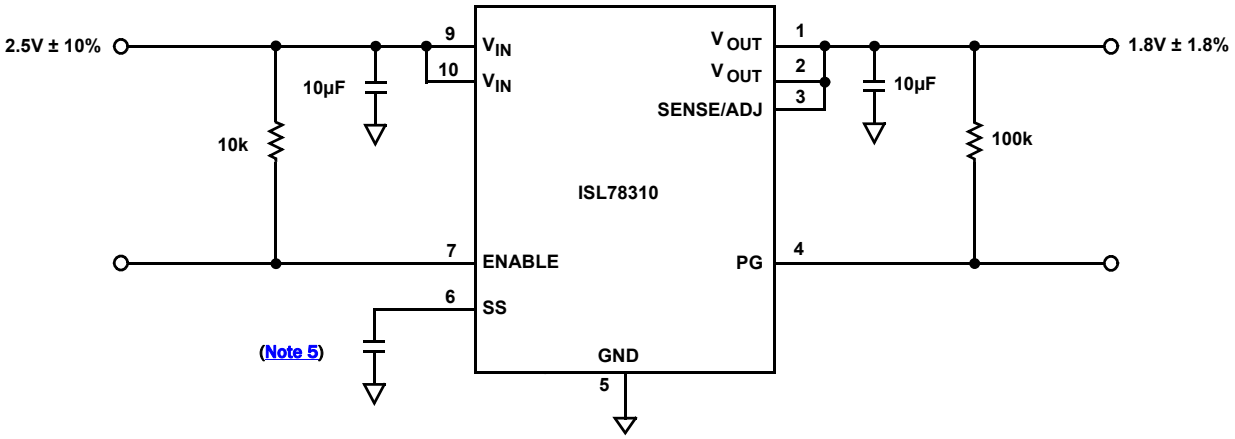


FIGURE 1. FIXED TYPICAL APPLICATION DIAGRAM

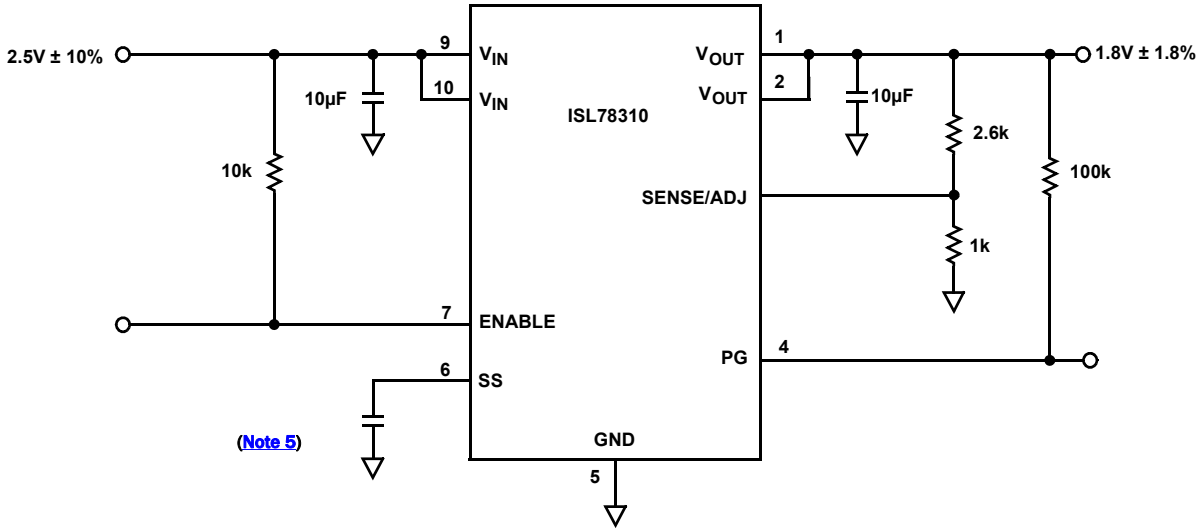
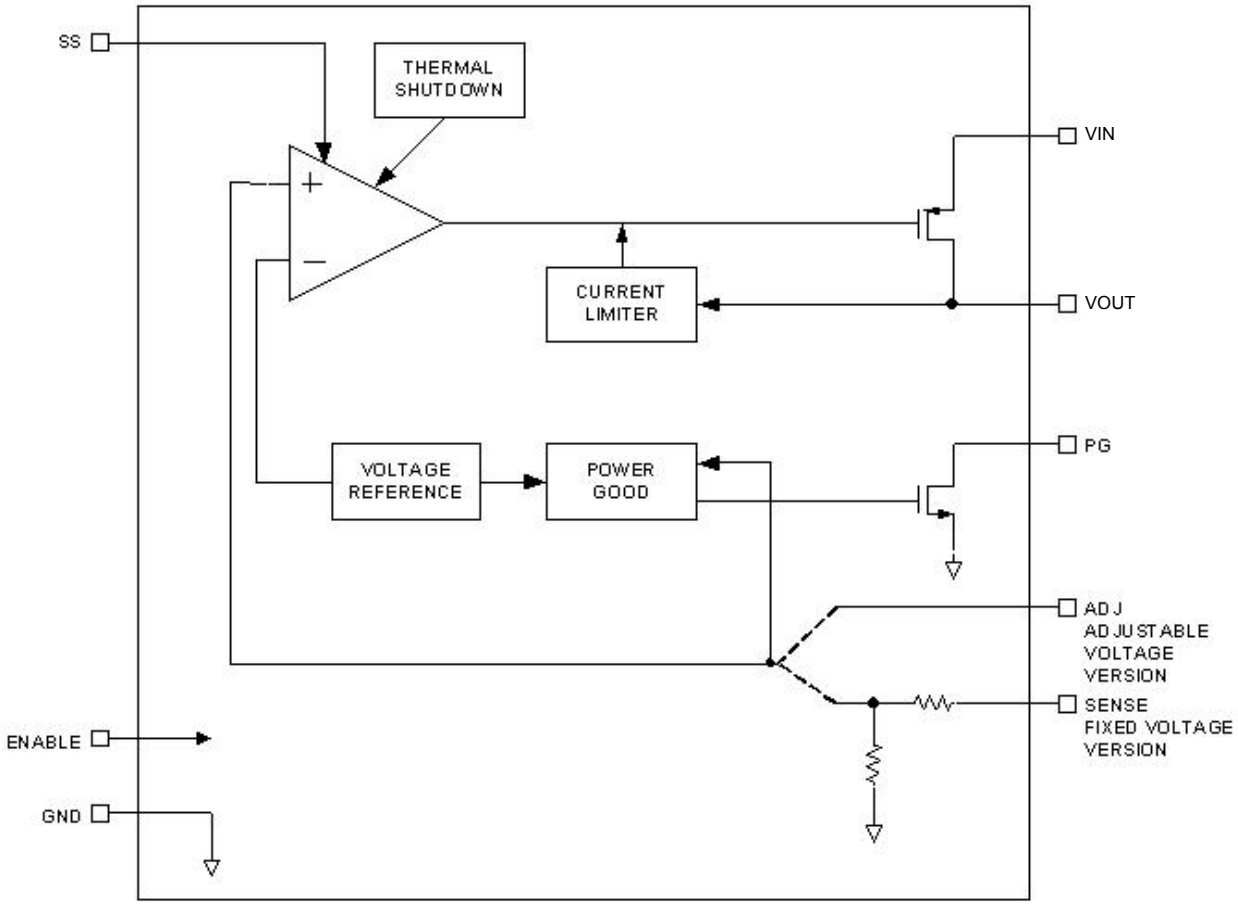


FIGURE 2. ADJUSTABLE TYPICAL APPLICATION DIAGRAM

NOTE:

5. Used when large bulk capacitance required on V_{OUT} for application.

ISL78310 Schematic Block Diagram



Absolute Maximum Ratings

VIN relative to GND (Note 6) . . . . . -0.3V to + 6.5V
VOUT relative to GND (Note 6). . . . . -0.3V to + 6.5V
PG, ENABLE, SENSE/ADJ, SS
Relative to GND (Note 6) . . . . . -0.3V to + 6.5V

Recommended Operating Conditions (Notes 9, 10)

Junction Temperature Range (T_J) (Note 9) . . . . . -40°C to +125°C
VIN relative to GND. . . . . 2.2V to 6V
VOUT range . . . . . 800mV to 5V
PG, ENABLE, SENSE/ADJ, SS relative to GND . . . . . 0V to + 6V
PG Sink Current . . . . . <10mA

Thermal Information

Thermal Resistance	θ_{JA} (°C/W)	θ_{JC} (°C/W)
10 Ld DFN Package (Notes 7, 8)	48	7

Storage Temperature Range. . . . . -65°C to +150°C
Junction Temperature . . . . . +150°C
Pb-Free Reflow Profile . . . . . see TB493

ESD Rating

Human Body Model (Tested per JESD22-A114E). 2.5kV
Machine Model (Tested per JESD-A115-A) 250V
Charge Device Model (Tested per AEC-Q100-011). 1kV

CAUTION: Do not operate at or near the maximum ratings listed for extended periods of time. Exposure to such conditions may adversely impact product reliability and result in failures not covered by warranty.

NOTES:

6. Absolute maximum voltage rating is defined as the voltage applied for a lifetime average duty cycle above 6V of 1%.
7. θ_{JA} is measured in free air with the component mounted on a high effective thermal conductivity test board with “direct attach” features. See Tech Brief TB379.
8. For θ_{JC}, the “case temp” location is the center of the exposed metal pad on the package underside.
9. Extended operation at these conditions may compromise reliability. Exceeding these limits will result in damage. Recommended operating conditions define limits where specifications are guaranteed.
10. Electromigration specification defined as lifetime average junction temperature of +110°C where max rated DC current = lifetime average current.

Electrical Specifications

Unless otherwise noted, $V_{IN} = V_{OUT} + 0.4V$, $V_{OUT} = 1.8V$, $C_{IN} = C_{OUT} = 10\mu F$, $T_J = +25°C$, $I_{LOAD} = 0A$. Applications must follow thermal guidelines of the package to determine worst case junction temperature. Please refer to “ISL78310 Schematic Block Diagram” on page 4 and Tech Brief TB379. **Boldface limits apply across the operating temperature range, -40°C to +125°C.**

PARAMETER	SYMBOL	TEST CONDITIONS	MIN (Note 11)	TYP	MAX (Note 11)	UNITS
DC CHARACTERISTICS						
DC Output Voltage Accuracy	V_{OUT}	V_{OUT} Options: 0.8V, 1.2V, 1.5V and 1.8V				
		$2.2V \le V_{IN} < 3.6V$; $0A < I_{LOAD} \le 1A$	**-1.8**	0.2	**1.8**	%
		V_{OUT} Options: 2.5V, 3.3V and 5.0V				
		$V_{OUT} + 0.4V \le V_{IN} \le 6V$; $0A < I_{LOAD} < 1A$	**-1.8**	0.2	**1.8**	%
Feedback Pin (ADJ Option Only)	V_{ADJ}	$2.2V \le V_{IN} \le 6V$, $0A < I_{LOAD} < 1A$	**491**	500	**509**	mV
DC Input Line Regulation	$\Delta V_{OUT}/\Delta V_{IN}$	$V_{OUT} + 0.5V < V_{IN} < 5V$			**1**	%
DC Output Load Regulation	$\Delta V_{OUT}/\Delta I_{OUT}$	$0A < I_{LOAD} < 1A$, All voltage options	**-1**			%
Feedback Input Current		$V_{ADJ} = 0.5V$		0.01	**1**	µA
Ground Pin Current	I_Q	$I_{LOAD} = 0A$, $2.2V < V_{IN} < 6V$		3	**5**	mA
		$I_{LOAD} = 1A$, $2.2V < V_{IN} < 6V$		5	**7**	mA
Ground Pin Current in Shutdown	I_{SHDN}	ENABLE Pin = 0V, $V_{IN} = 6V$		0.2	**12**	µA
Dropout Voltage (Note 12)	V_{DO}	$I_{LOAD} = 1A$, $V_{OUT} = 2.5V$		130	**212**	mV
Output Short Circuit Current	OCP	$V_{OUT} = 0V$, $2.2V < V_{IN} < 6V$		1.75		A
Thermal Shutdown Temperature	TSD	$2.2V < V_{IN} < 6V$		160		°C
Thermal Shutdown Hysteresis (Rising Threshold)	TSDn	$2.2V < V_{IN} < 6V$		30		°C
AC CHARACTERISTICS						
Input Supply Ripple Rejection	PSRR	f = 1kHz, $I_{LOAD} = 1A$; $V_{IN} = 2.2V$		58		dB
		f = 120Hz, $I_{LOAD} = 1A$; $V_{IN} = 2.2V$		72		dB
Output Noise Voltage		$I_{LOAD} = 1A$, BW = 10Hz < f < 100kHz		63		μV_{RMS}

Electrical Specifications Unless otherwise noted, $V_{IN} = V_{OUT} + 0.4V$, $V_{OUT} = 1.8V$, $C_{IN} = C_{OUT} = 10\mu F$, $T_J = +25°C$, $I_{LOAD} = 0A$. Applications must follow thermal guidelines of the package to determine worst case junction temperature. Please refer to "ISL78310 Schematic Block Diagram" on page 4 and Tech Brief TB379. **Boldface limits apply across the operating temperature range, -40°C to +125°C. (Continued)**

PARAMETER	SYMBOL	TEST CONDITIONS	MIN (Note 11)	TYP	MAX (Note 11)	UNITS
ENABLE PIN CHARACTERISTICS						
Turn-on Threshold		$2.2V < V_{IN} < 6V$	**0.3**	0.8	**1**	V
Hysteresis (Rising Threshold)		$2.2V < V_{OUT} + 0.4V < 6V$	**10**	80	**200**	mV
Enable Pin Turn-on Delay		$C_{OUT} = 10\mu F$, $I_{LOAD} = 1A$		100		µs
Enable Pin Leakage Current		$V_{IN} = 6V$, EN = 3V			**1**	µA
ADJUSTABLE INRUSH CURRENT LIMIT CHARACTERISTICS						
Current limit adjust	I_{PD}	$V_{IN} = 3.5V$, EN = 0V, SS = 1V	**0.5**	1	**1.3**	mA
	I_{CHG}		**-3.3**	-2	**-0.8**	µA
PG PIN CHARACTERISTICS						
V_{OUT} PG Flag Threshold			**75**	85	**92**	$\%V_{OUT}$
V_{OUT} PG Flag Hysteresis				4		%
PG Flag Low Voltage		$V_{IN} = 2.5V$, $I_{SINK} = 500\mu A$			**100**	mV
PG Flag Leakage Current		$V_{IN} = 6V$, PG = 6V			**1**	µA

NOTES:

11. Compliance to datasheet limits is assured by one or more methods: production test, characterization and/or design.
12. Dropout is defined by the difference in supply V_{IN} and V_{OUT} when the supply produces a 2% drop in V_{OUT} from its nominal value.

Typical Operating Performance

Unless otherwise noted: V_{IN} = 2.2V, V_{OUT} = 1.8V, C_{IN} = C_{OUT} = 10µF, T_J = +25°C, I_L = 0A.

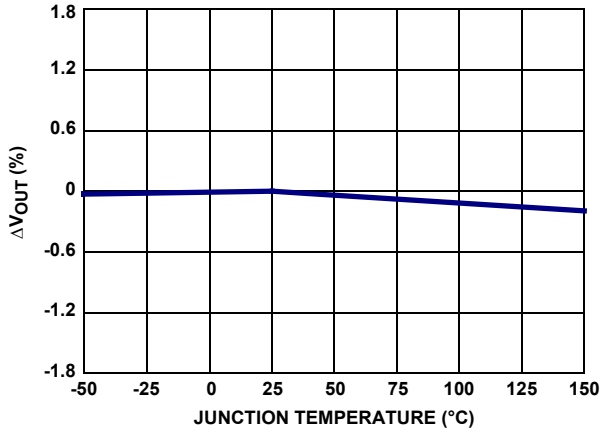


FIGURE 3. V_{OUT} vs TEMPERATURE

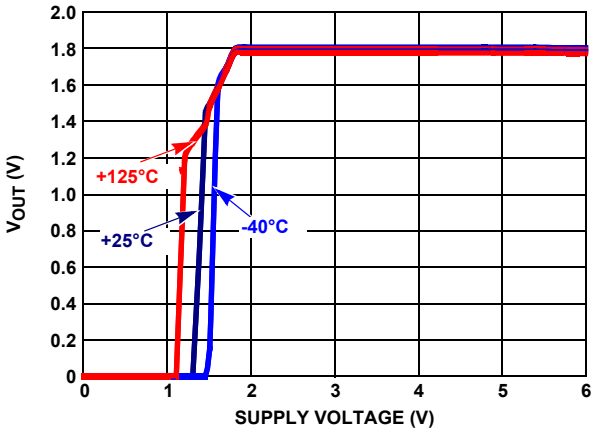


FIGURE 4. V_{OUT} vs SUPPLY VOLTAGE

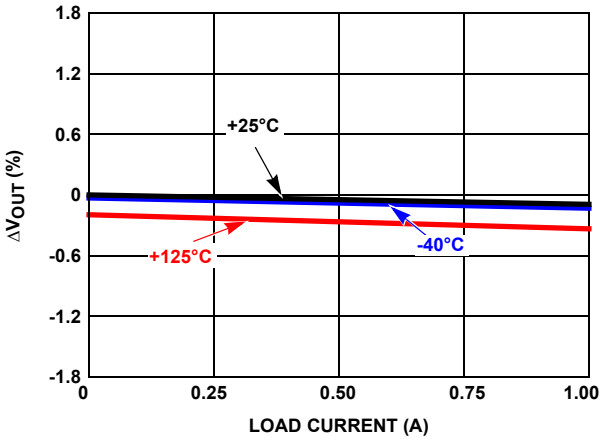


FIGURE 5. V_{OUT} vs LOAD CURRENT

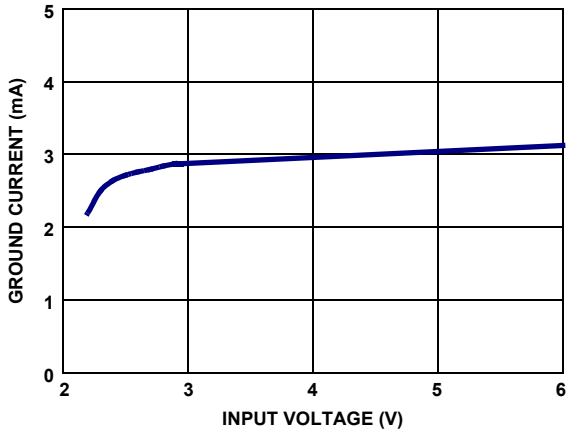


FIGURE 6. GROUND CURRENT vs SUPPLY VOLTAGE

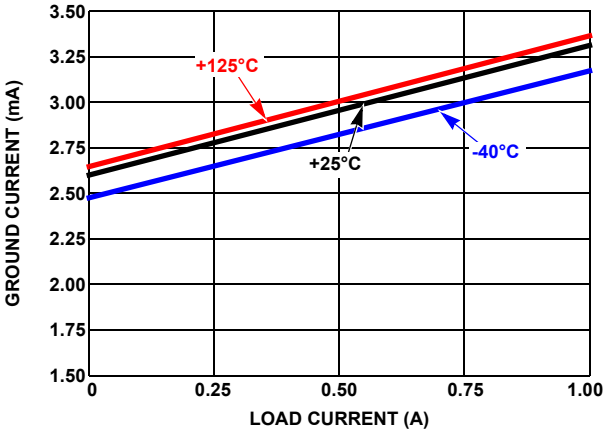


FIGURE 7. GROUND CURRENT vs LOAD CURRENT

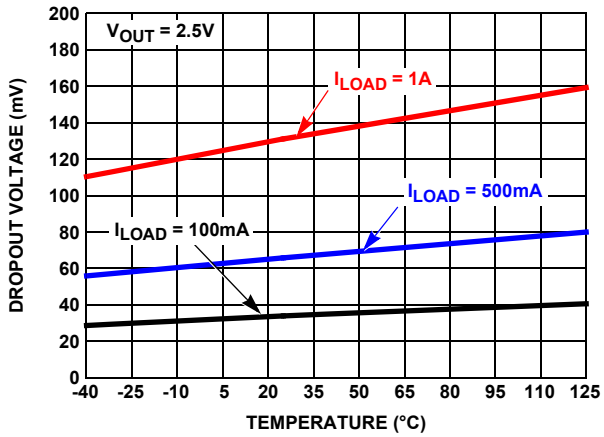


FIGURE 8. DROPOUT VOLTAGE vs TEMPERATURE

Typical Operating Performance

Unless otherwise noted: V_{IN} = 2.2V, V_{OUT} = 1.8V, C_{IN} = C_{OUT} = 10µF, T_J = +25°C, I_L = 0A. **(Continued)**

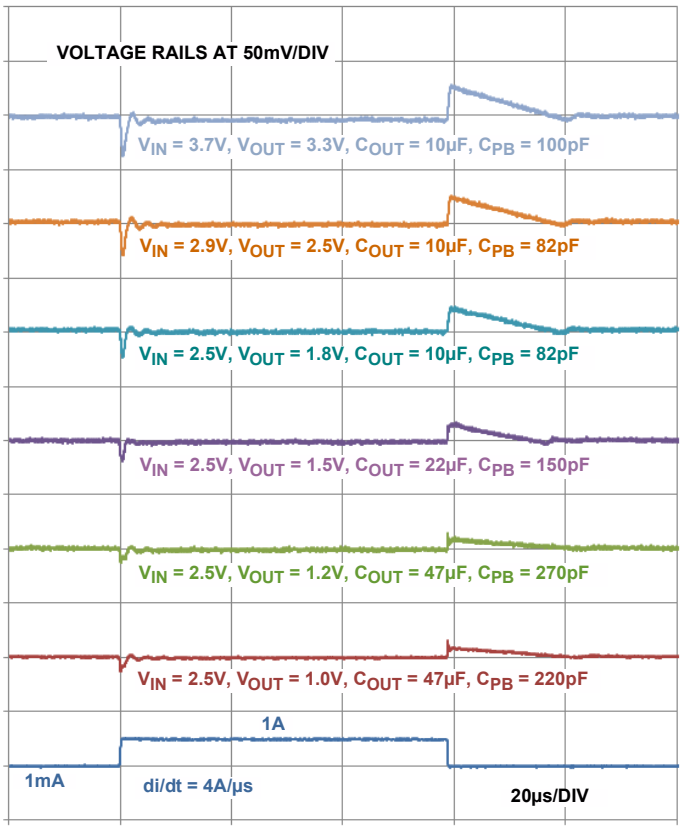


FIGURE 9. LOAD TRANSIENT RESPONSE

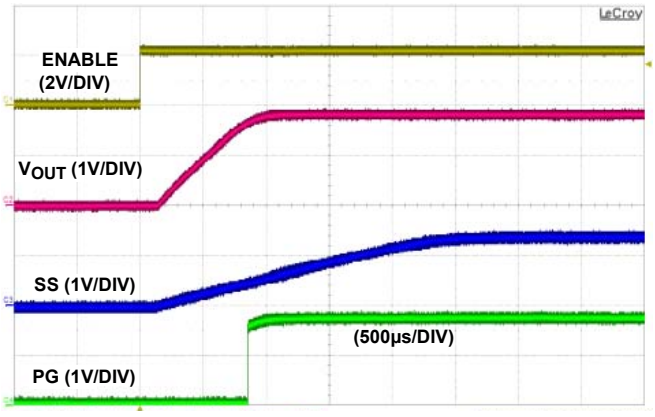


FIGURE 10. ENABLE START-UP

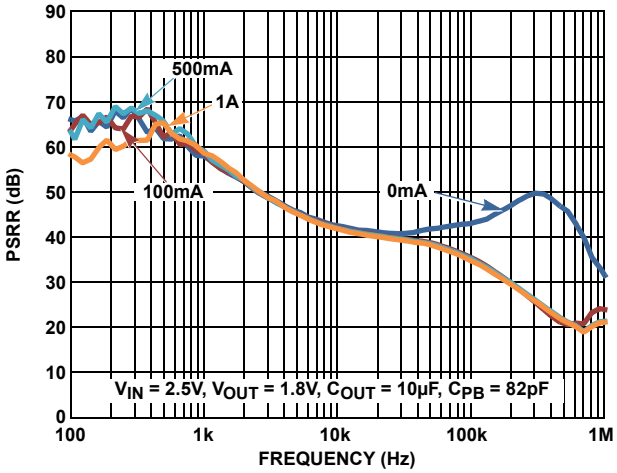


FIGURE 11. PSRR vs FREQUENCY

Typical Operating Performance

Unless otherwise noted: V_{IN} = 2.2V, V_{OUT} = 1.8V, C_{IN} = C_{OUT} = 10µF, T_J = +25°C, I_L = 0A. **(Continued)**

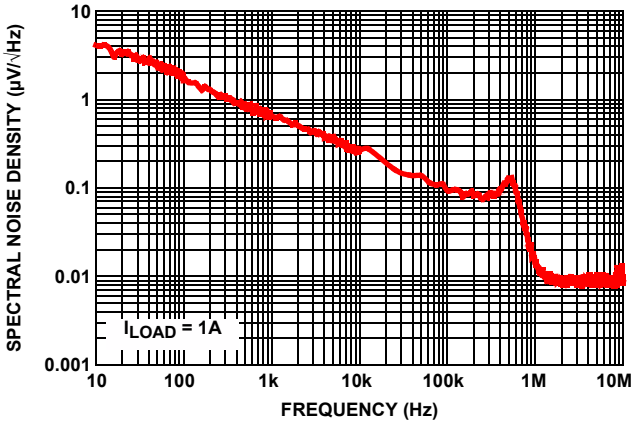


FIGURE 12. SPECTRAL NOISE DENSITY vs FREQUENCY

Applications Information

Input Voltage Requirements

The ISL78310 is capable of delivering output voltages from 0.8V to 5.0V. Due to the nature of an LDO, V_{IN} must be some margin higher than the output voltage plus dropout at the maximum rated current of the application if active filtering (PSRR) is expected from V_{IN} to V_{OUT}. The generous dropout specification of this family of LDOs allows applications to design for a level of efficiency that can accommodate profiles smaller than the TO220/263.

External Capacitor Requirements

GENERAL GUIDELINE

External capacitors are required for proper operation. Careful attention must be paid to layout guidelines and selection of capacitor type and value to ensure optimal performance.

OUTPUT CAPACITOR

The ISL78310 applies state of the art internal compensation to keep the selection of the output capacitor simple for the customer. Stable operation over full temperation, V_{IN} range, V_{OUT} range and load extremes are guaranteed for all capacitor types and values assuming a minimum of 10µF X5R/X7R is used for local bypass on V_{OUT}. This output capacitor must be connected to the V_{OUT} and GND pins of the LDO with PCB traces no longer than 0.5cm. Additional capacitors of any value in ceramic, POSCAP, alum/tantalum electrolytic types may be placed in parallel to improve PSRR at higher frequencies and/or load transient AC output voltage tolerances.

INPUT CAPACITOR

For proper operation, a minimum capacitance of 10µF X5R/X7R is required at the input. This ceramic input capacitor must be connected to V_{IN} and GND pins of the LDO with PCB traces no longer than 0.5cm.

Phase Boost Capacitor (C_{PB})

A small phase boost capacitor, CPB, can be placed across the top resistor in the feedback resistor divider network (Figure 13) in order to place a zero at:

$$F_Z = 1/(2 \bullet pi \bullet R_{TOP} \bullet C_{PB}) \quad \text{(EQ. 1)}$$

This zero increases the crossover frequency of the LDO and provides additional phase resulting in faster load transient response.

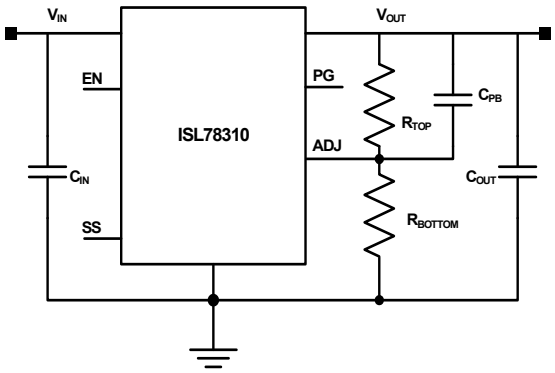


FIGURE 13.

It is also important to note that the LDO stability and load transient are affected by the type of output capacitor used. For optimal result, empirical tuning of C_{PB} is suggested for each specific application. It is recommended to not use C_{PB} when high ESR capacitors such as aluminum electrolytic or tantalum are used.

Table 1 shows the recommended C_{PB}, R_{TOP}, R_{BOTTOM} and C_{PB} values for different output voltage rails.

TABLE 1.

V_{OUT} (V)	R_{TOP} (kΩ)	R_{BOTTOM} (Ω)	C_{PB} (pF)	C_{OUT} (µF)
5.0	2.61	287	100	10
3.3	2.61	464	100	10
2.5	2.61	649	82	10
1.8	2.61	1.0k	82	10
1.5*	2.61	1.3k	68	10
1.5	2.61	1.3k	150	22
1.2*	2.61	1.87k	120	22
1.2*	2.61	1.87k	270	47
1.0	2.61	2.61k	220	47
0.8	2.61	4.32k	220	47

*Either option could be used, depending on cost/performance requirements.

Thermal Fault Protection

In the event the die temperature exceeds typically +160°C, then the output of the LDO shuts down until the die temperature cools down to typically +130°C. The level of power, combined with the thermal resistance of the package (+48°C/W for DFN), determines whether the junction temperature exceeds the thermal shutdown temperature specified in the "Electrical Specifications" on page 5 (see thermal packaging guidelines).

Current Limit Protection

The ISL78310 LDO incorporates protection against overcurrent due to any short or overload condition applied to the output pin. The current limit circuit performs as a constant current source when the output current exceeds the current limit threshold noted in the "Electrical Specifications" on page 5. If the short or overload condition is removed from V_{OUT}, then the output returns to normal voltage mode regulation. In the event of an overload condition on the DFN package, the LDO will begin to cycle on and off due to the die temperature exceeding thermal fault condition.

Functional Description

Enable Operation

The Enable turn-on threshold is typically 0.8V with a hysteresis of 80mV. The Enable pin does not have an internal pull-up or pull-down resistor. As a result, this pin must not be left floating. This pin must be tied to VIN if it is not used. A pull-up resistor (typically 1kΩ to 10kΩ) will be required for applications that use open collector or open drain outputs to control the Enable pin. The Enable pin may be connected directly to VIN for applications that are always on.

Soft-Start Operation

The soft-start circuit controls the rate at which the output voltage rises up to regulation at power-up or LDO enable. This start-up ramp time can be set by adding an external capacitor from the SS pin to GND. An internal 2µA current source charges up this C_{SS} and the feedback reference voltage is clamped to the voltage across it. The start-up time of the regulator output voltage for a given C_{SS} value can be calculated using Equation 2.

$$t_{RAMP} = \frac{C_{SS} x 0.5V}{2\mu A} \quad \text{(EQ. 2)}$$

The soft-start function also effectively limits the amount of in-rush current to less than the programmed current limit during start-up or an enable sequence, to avoid an overcurrent fault condition. This can be an issue for applications that require large, external bulk capacitances on V_{OUT} where high levels of charging current can be seen for a significant period of time. High in-rush currents can cause V_{IN} to drop below minimum, which could cause V_{OUT} to shutdown.

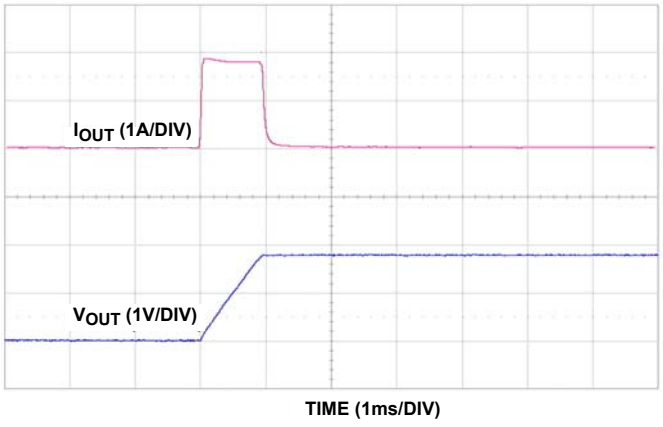


FIGURE 14. IN-RUSH CURRENT WITH NO C_{SS}, C_{OUT} = 1000µF, IN-RUSH CURRENT = 1.8A

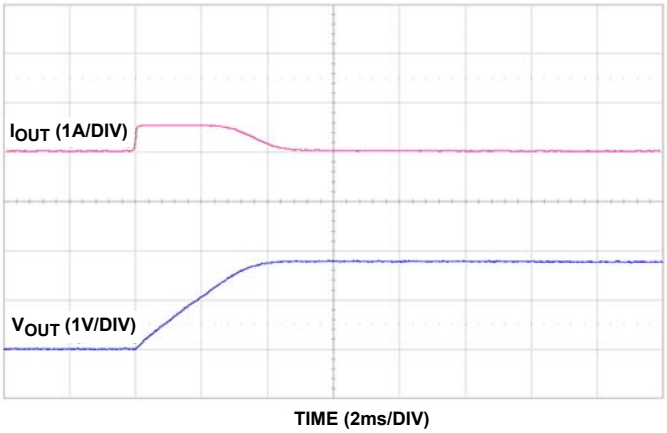


FIGURE 15. IN-RUSH CURRENT WITH C_{SS} = 15nF, C_{OUT} = 1000µF, IN-RUSH CURRENT = 0.5A

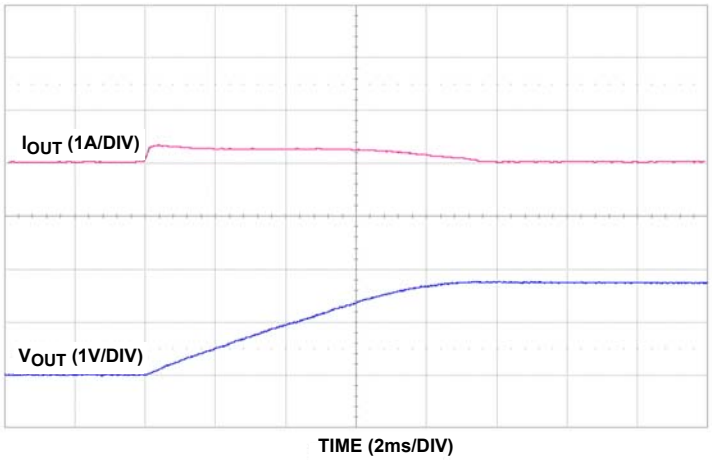


FIGURE 16. IN-RUSH CURRENT WITH C_{SS} = 33nF, C_{OUT} = 1000µF, IN-RUSH CURRENT = 0.2A

Equation 3 can be used to calculate C_{SS} for a desired in-rush current, where V_{OUT} is the output voltage, C_{OUT} is the total capacitance on the output, and I_{INRUSH} is the desired in-rush current.

$$C_{SS} = \frac{(V_{OUT} \times C_{OUT} \times 2\mu A)}{I_{INRUSH} \times 0.5V} \quad \text{(EQ. 3)}$$

The scopes in Figures 14, 15 and 16 capture the response for the soft-start function. The output voltage is set to 1.8V.

The external capacitor is always discharged to ground at the beginning of start-up or enabling.

Power-Good Operation

The PGOOD is a logic output that indicates the status of V_{OUT}. The PGOOD flag is an open-drain NMOS that can sink 10mA during a fault condition. The PGOOD pin requires an external pull-up resistor, which is typically connected to the VOUT pin. The PGOOD pin should not be pulled up to a voltage source greater than V_{IN}. The PGOOD goes low when the output voltage drops below 84% of the nominal output voltage or if the part is disabled. The PGOOD comparator functions during current limit and thermal shutdown. For applications not using this feature, connect this pin to ground.

Output Voltage Selection

An external resistor divider is used to scale the output voltage relative to the internal reference voltage. This voltage is then fed back to the error amplifier. The output voltage can be programmed to any level between 0.8V and 5V. An external resistor divider, R_1 and R_2, is used to set the output voltage as shown in Equation 4. The recommended value for R_2 is 500Ω to 1kΩ. R_1 is then chosen according to Equation 5.

$$V_{OUT} = 0.5V \times \left(\frac{R_1}{R_2} + 1\right) \quad \text{(EQ. 4)}$$

$$R_1 = R_2 \times \left(\frac{V_{OUT}}{0.5V} - 1\right) \quad \text{(EQ. 5)}$$

Power Dissipation

The junction temperature must not exceed the range specified in the "Recommended Operating Conditions" on page 5. The power dissipation can be calculated by using Equation 6:

$$P_D = (V_{IN} - V_{OUT}) \times I_{OUT} + V_{IN} \times I_{GND} \quad \text{(EQ. 6)}$$

The maximum allowed junction temperature, $T_{J(MAX)}$, and the maximum expected ambient temperature, $T_{A(MAX)}$, will determine the maximum allowable power dissipation, as shown in Equation 7:

$$P_{D(MAX)} = (T_{J(MAX)} - T_A)/\theta_{JA} \quad \text{(EQ. 7)}$$

θ_{JA} is the junction-to-ambient thermal resistance.

For safe operation, ensure that the power dissipation P_D, calculated from Equation 6, is less than the maximum allowable power dissipation $P_{D(MAX)}$.

Heatsinking the DFN Package

The DFN package uses the copper area on the PCB as a heat-sink. The EPAD of this package must be soldered to the copper plane (GND plane) for heat sinking. Figure 17 shows a curve for the θ_{JA} of the DFN package for different copper area sizes.

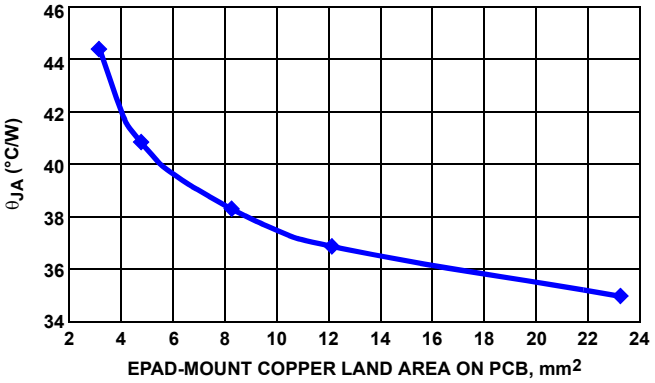


FIGURE 17. 3mmx3mm 10 LD DFN ON 4-LAYER PCB WITH THERMAL VIAS θ_{JA} vs EPAD-MOUNT COPPER LAND AREA ON PCB

General Power PAD Design Considerations

Figure 18 shows the recommended use of vias on the thermal pad to remove heat from the IC. This typical array populates the thermal pad footprint with vias spaced three times the radius distance from the center of each via. Small via size is advisable, but not to the extent that solder reflow becomes difficult.

All vias should be connected to the pad potential, with low thermal resistance for efficient heat transfer. Complete connection of the plated-through hole to each plane is important. It is not recommended to use "thermal relief" patterns to connect the vias.

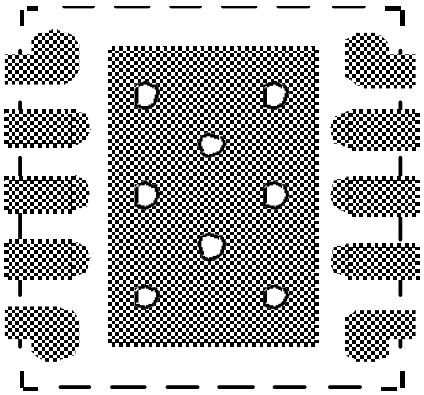


FIGURE 18. PCB VIA PATTERN

Revision History

The revision history provided is for informational purposes only and is believed to be accurate, but not warranted. Please go to web to make sure you have the latest Rev.

DATE	REVISION	CHANGE
November 7, 2014	FN7810.2	"Absolute Maximum Ratings" on page 5: Updated CDM testing from: Charged Device Model (Tested per JESD22-C101E) to Charged Device Model (Tested per AEC Q100-011). On page 2: Removed part number ISL78310ARAJZ-TR5303 from ordering information table. Updated POD from rev 6 to rev 9.
December 23, 2013	FN7810.1	Page 12 - 2nd line of the disclaimer changed from: "Intersil products are manufactured, assembled and tested utilizing ISO9001 quality systems as noted" to: "Intersil Automotive Qualified products are manufactured, assembled and tested utilizing TS16949 quality systems as noted".
February 17, 2011	FN7810.0	Initial Release.

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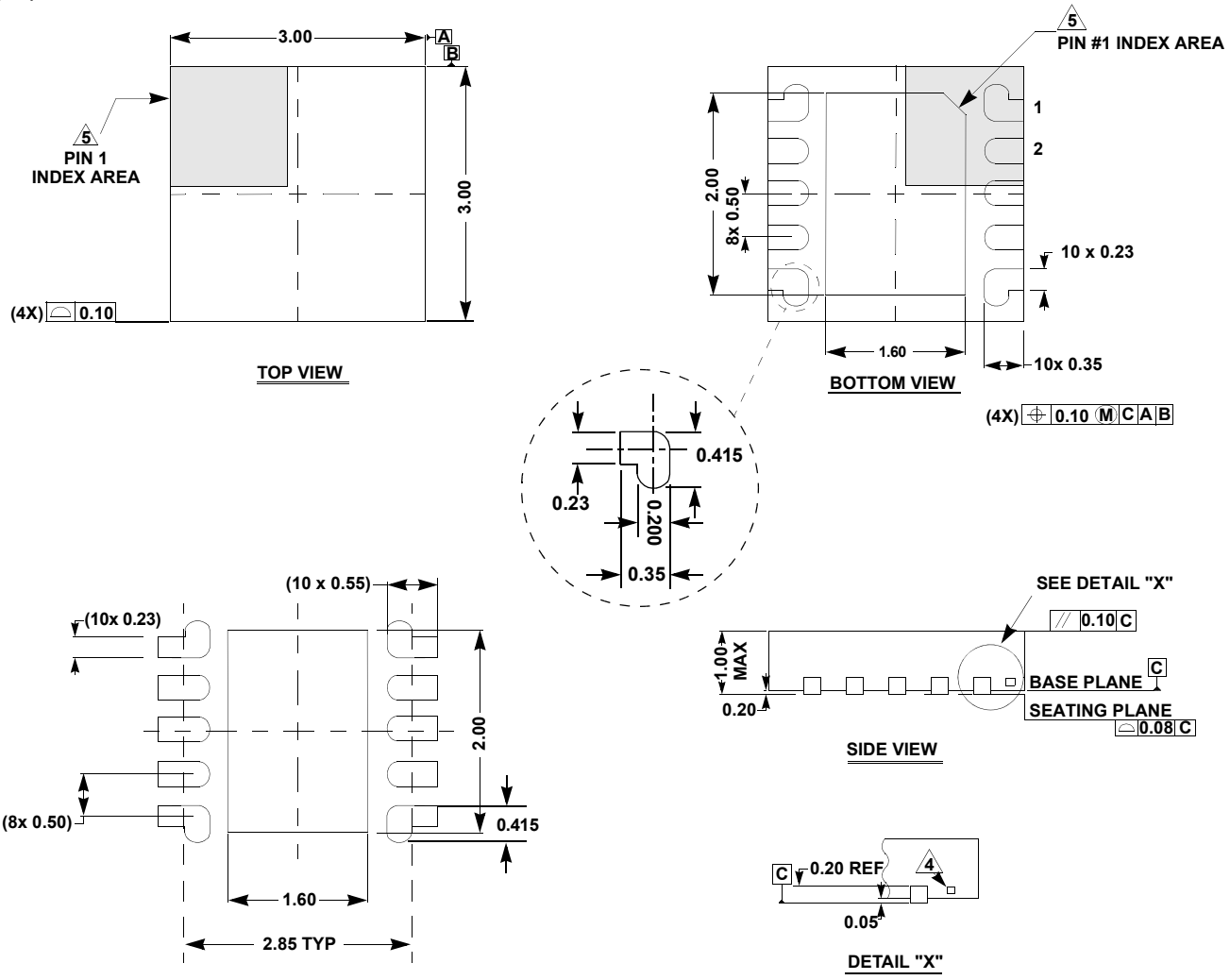
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Package Outline Drawing

L10.3x3

10 LEAD DUAL FLAT PACKAGE (DFN)

Rev 9, 10/13



NOTES:

1. Dimensions are in millimeters.
   Dimensions in ( ) for Reference Only.
2. Dimensioning and tolerancing conform to ASME Y14.5m-1994.
3. Unless otherwise specified, tolerance : Decimal ± 0.05
4. Tiebar shown (if present) is a non-functional feature.
5. The configuration of the pin #1 identifier is optional, but must be located within the zone indicated. The pin #1 identifier may be either a mold or mark feature.

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