ISL80136

40V, Low Quiescent Current, High Accuracy, 50mA Linear Regulator

The ISL80136 is a high voltage, low quiescent current linear regulator ideally suited for “always-on” and “keep alive” applications. The ISL80136 operates from an input voltage of +6V to +40V under normal operating conditions, consuming only 18µA of quiescent current at no load.

The ISL80136 offers adjustable output voltages from 2.5V to 12V. It features an EN pin that can be used to put the device into a low-quiescent current shutdown mode where it draws only 1.8µA of supply current. The device features over-temperature shutdown and current limit protection.

The ISL80136 is rated across the -40°C to +125°C temperature range and is available in an 8 lead EPSOIC with an exposed pad package.

Applications

- Industrial
- Networking
- Telecom

Features

- Wide V_{IN} range of 6V to 40V
- Adjustable output voltage from 2.5V to 12V
- Ensured 50mA output current
- Ultra low 18µA typical quiescent current
- Low 1.8µA of typical shutdown current
- ±1% accurate voltage reference (over temperature, load)
- Low dropout voltage of 120mV at 50mA
- Low 26µV_{RMS} noise
- 40V tolerant logic level (TTL/CMOS) enable input
- Stable operation with 10µF output capacitor
- 5kV ESD HBM rated
- Thermal shutdown and current limit protection

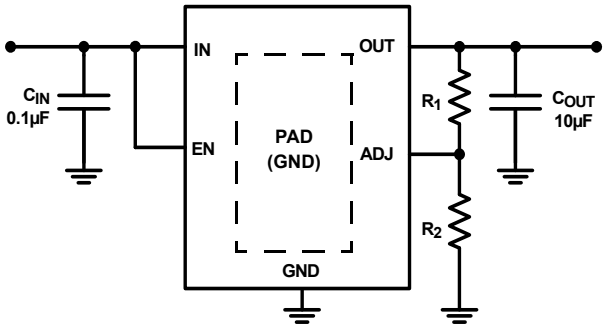

FIGURE 1. TYPICAL APPLICATION

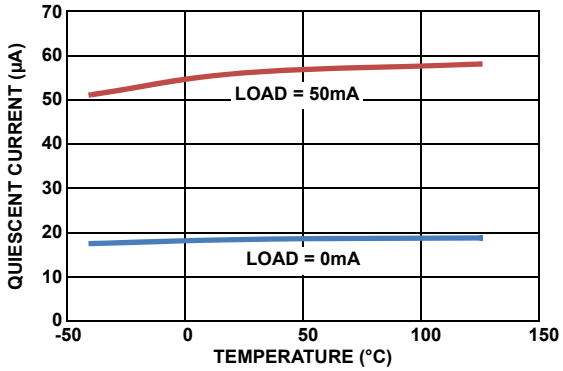

FIGURE 2. QUIESCENT CURRENT vs LOAD CURRENT (AT UNITY GAIN), V_{IN} = 14V

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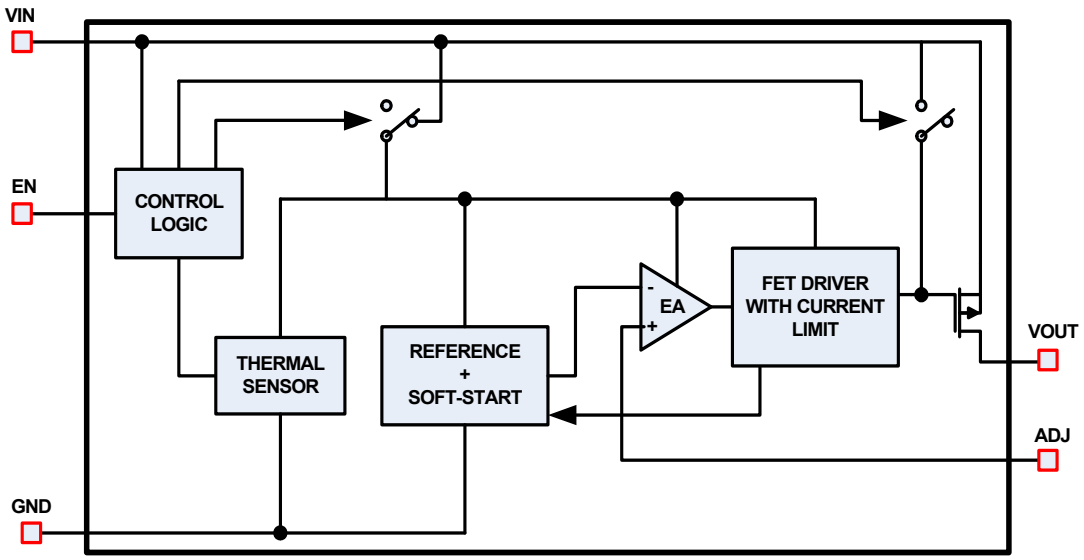
Block Diagram



Ordering Information

PART NUMBER (Notes 2, 3)	PART MARKING	ENABLE PIN	OUTPUT VOLTAGE (V)	PACKAGE DESCRIPTION (RoHS Compliant)	PKG. DWG. #	CARRIER TYPE (Note 1)	TEMP. RANGE (°C)
ISL80136IBEAJZ	80136 IBEAJZ	Yes	ADJ	8 Ld EPSOIC	M8.15B	Tube	-40 to +125
ISL80136IBEAJZ-T						Reel, 2.5k	
ISL80136IBEAJZ-T7A						Reel, 250	
ISL80136EVAL1Z	Evaluation Platform						

NOTES:

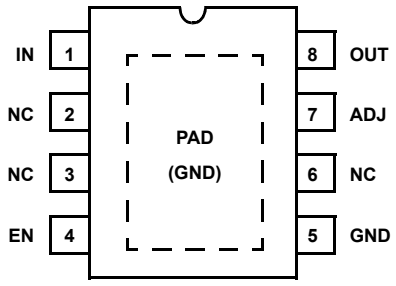
1. See TB347 for details about reel specifications.
2. These Pb-free plastic packaged products employ special Pb-free material sets, molding compounds/die attach materials, and 100% matte tin plate plus anneal (e3 termination finish, which is RoHS compliant and compatible with both SnPb and Pb-free soldering operations). Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J STD-020.
3. For Moisture Sensitivity Level (MSL), see the ISL80136 device page. For more information about MSL, see TB363.

TABLE 1. KEY DIFFERENCES IN FAMILY OF 40V LDO PARTS

PART NUMBER	MINIMUM I_{OUT}	IC PACKAGE
ISL80410	150mA	8 Ld EPSOIC
ISL80136	50mA	8 Ld EPSOIC
ISL80138	150mA	14 LD HTSSOP

Pin Configuration

8 LD EPSOIC
TOP VIEW



Pin Descriptions

PIN #	PIN NAME	DESCRIPTION
1	IN	Input voltage pin. A minimum 0.1µF X5R/X7R capacitor is required for proper operation. Range: 6V to 40V
2, 3, 6	NC	Pins have internal termination and can be left unconnected. Connection to ground is optional.
4	EN	High on this pin enables the device. Range: 0V to V_{IN}
5	GND	Ground pin.
7	ADJ	This pin is connected to the external feedback resistor divider, which sets the LDO output voltage.
8	OUT	Regulated output voltage. A 10µF X5R/X7R output capacitor is required for stability. Range: 0V to 12V
-	PAD	It is recommended to solder the PAD to the ground plane.

Absolute Maximum Ratings

IN Pin to GND Voltage . . . . . GND - 0.3V to +45V
OUT Pin to GND Voltage . . . . . GND - 0.3V to 16V
EN Pin to GND Voltage . . . . . GND - 0.3V to IN
ADJ Pin to GND Voltage . . . . . GND - 0.3V to3V
Output Short-circuit Duration . . . . . Indefinite
ESD Rating
Human Body Model (Tested per JESD22-A114E) 5kV
Machine Model (Tested per JESD-A115-A) 200V
Charge Device Model (Tested per JESD22-C101C) 2.2kV
Latch-Up (Tested per JESD78B; Class II, Level A) 100mA

Thermal Information

Thermal Resistance (Typical)	θ_{JA} (°C/W)	θ_{JC} (°C/W)
8 Ld EPSOIC Package (Notes 4, 5)	50	9

Maximum Junction Temperature . . . . . +150°C
Maximum Storage Temperature Range . . . . . -65°C to +175°C
Pb-Free Reflow Profile . . . . . see TB493

Recommended Operating Conditions

Ambient Temperature Range . . . . . -40°C to +125°C
IN Pin to GND Voltage . . . . . +6V to +40V
OUT Pin to GND Voltage . . . . . +2.5V to +12V
EN Pin to GND Voltage . . . . . 0V to +40V

CAUTION: Do not operate at or near the maximum ratings listed for extended periods of time. Exposure to such conditions can adversely impact product reliability and result in failures not covered by warranty.

NOTES:

4. θ_{JA} is measured in free air with the component mounted on a high-effective thermal conductivity test board with "direct attach" features. See TB379.
5. For θ_{JC}, the "case temp" location is the center of the exposed metal pad on the package underside.

Electrical Specifications

Recommended operating conditions, unless otherwise noted. V_{IN} = 14V, I_{OUT} = 1mA, T_A = T_J = -40°C to +125°C, unless otherwise noted. Typical specifications are at T_A = +25°C. **Boldface limits apply across the operating temperature range, -40°C to +125°C.**

PARAMETER	SYMBOL	TEST CONDITIONS	MIN (Note 8)	TYP	MAX (Note 8)	UNIT
Input Voltage Range	V_{IN}		**6**		**40**	V
Guaranteed Output Current	I_{OUT}	V_{IN} = V_{OUT} + VDO	**50**			mA
ADJ Reference Voltage	V_{REF}	EN = High, V_{IN} = 14V, I_{OUT} = 0.1mA to 50mA	**1.211**	1.223	**1.235**	V
Line Regulation	(V_{OUT} low line - V_{OUT} high line)/V_{OUT} low line	6V < V_{IN} < 40V, I_{OUT} = 1mA		0.04	**0.115**	%
Load Regulation	(V_{OUT} no load - V_{OUT} high load)/V_{OUT} no load	V_{IN} = 14V, I_{OUT} = 100µA to 50mA		0.25	**0.5**	%
Dropout Voltage (Note 6)	ΔV_{DO}	I_{OUT} = 1mA, V_{OUT} = 2.5V		10	**38**	mV
		I_{OUT} = 50mA, V_{OUT} = 2.5V		130	**340**	mV
		I_{OUT} = 1mA, V_{OUT} = 5V		10	**48**	mV
		I_{OUT} = 50mA, V_{OUT} = 5V		120	**350**	mV
Shutdown Current	I_{SHDN}	EN = LOW		1.8	**3.64**	µA
Quiescent Current	IQ	EN = HIGH, I_{OUT} = 0mA		18	**24**	µA
		EN = HIGH, I_{OUT} = 1mA		22	**42**	µA
		EN = HIGH, I_{OUT} = 10mA		34	**60**	µA
		EN = HIGH, I_{OUT} = 50mA		56	**82**	µA
Power Supply Rejection Ratio	PSRR	f = 100Hz; VIN_RIPPLE = 500mV_{P-P}; Load = 50mA		58		dB
Output Voltage Noise		V_{IN} = 14V, V_{OUT} = 3.3V, C_{OUT} = 10µF, I_{OUT} = 10mA, BW = 100Hz to 100kHz		26		μV_{RMS}
EN FUNCTION						
EN Threshold Voltage	V_{EN_H}	V_{OUT} = Off to On			**1.485**	V
	V_{EN_L}	V_{OUT} = On to Off	**0.935**			V
EN Pin Current	I_{EN}	V_{OUT} = 0V		0.026		µA
EN to Regulation Time (Note 7)	t_{EN}			1.65	**1.93**	ms

Electrical Specifications Recommended operating conditions, unless otherwise noted. V_{IN} = 14V, I_{OUT} = 1mA, T_A = T_J = -40°C to +125°C, unless otherwise noted. Typical specifications are at T_A = +25°C. **Boldface limits apply across the operating temperature range, -40°C to +125°C. (Continued)**

PARAMETER	SYMBOL	TEST CONDITIONS	MIN (Note 8)	TYP	MAX (Note 8)	UNIT
PROTECTION FEATURES						
Output Current Limit	I_{LIMIT}	V_{OUT} = 0V	**60**	118		mA
Thermal Shutdown	T_{SHDN}	Junction Temperature Rising		+165		°C
Thermal Shutdown Hysteresis	T_{HYST}			+20		°C

NOTES:

6. Dropout voltage is defined as (V_{IN} - V_{OUT}) when V_{OUT} is 2% below the value of V_{OUT}.
7. Enable to Regulation Time is the time the output takes to reach 95% of its final value with V_{IN} = 14V and EN is taken from V_{IL} to V_{IH} in 5ns. The output voltage is set at 5V.
8. Parameters with MIN and/or MAX limits are 100% tested at +25°C, unless otherwise specified. Temperature limits established by characterization and are not production tested.

Typical Performance Curves

V_{IN} = 14V, I_{OUT} = 1mA, V_{OUT} = 5V, T_J = +25 °C unless otherwise specified.

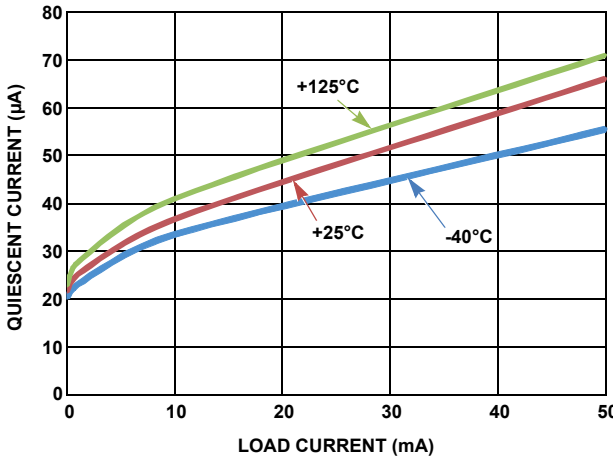


FIGURE 3. QUIESCENT CURRENT vs LOAD CURRENT

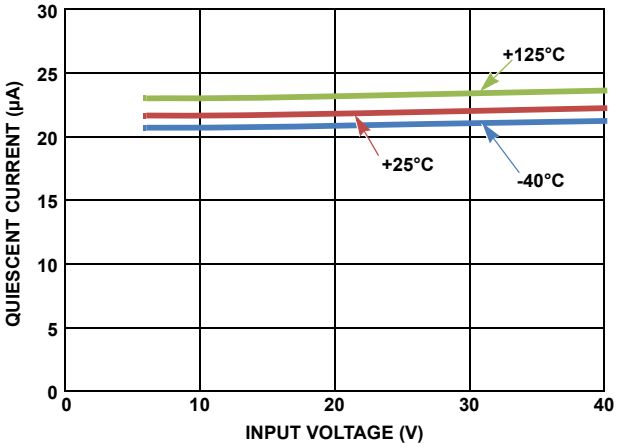


FIGURE 4. QUIESCENT CURRENT vs INPUT VOLTAGE (NO LOAD)

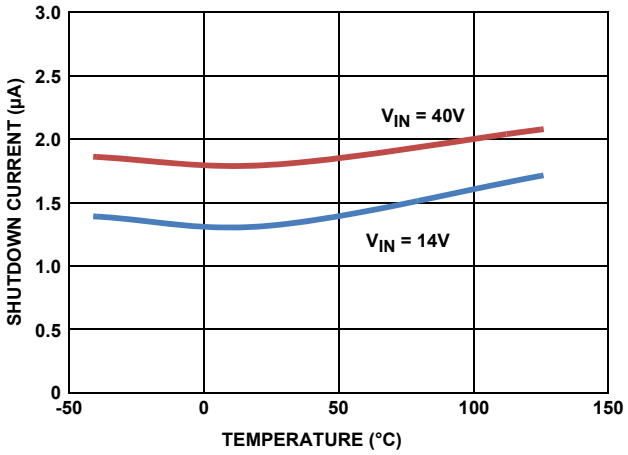


FIGURE 5. SHUTDOWN CURRENT vs TEMPERATURE (EN = 0)

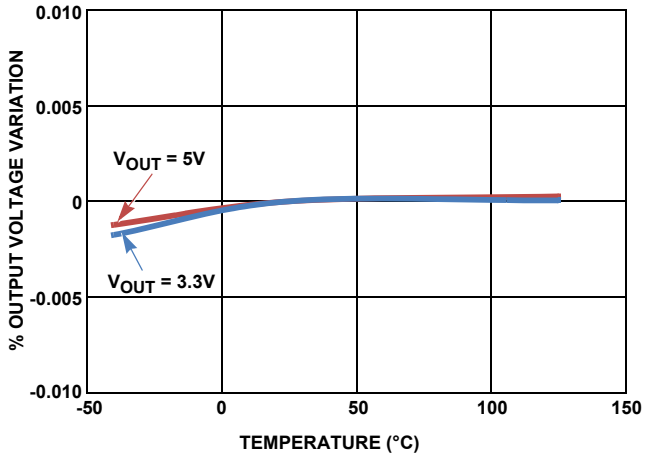


FIGURE 6. OUTPUT VOLTAGE vs TEMPERATURE (LOAD = 50mA)

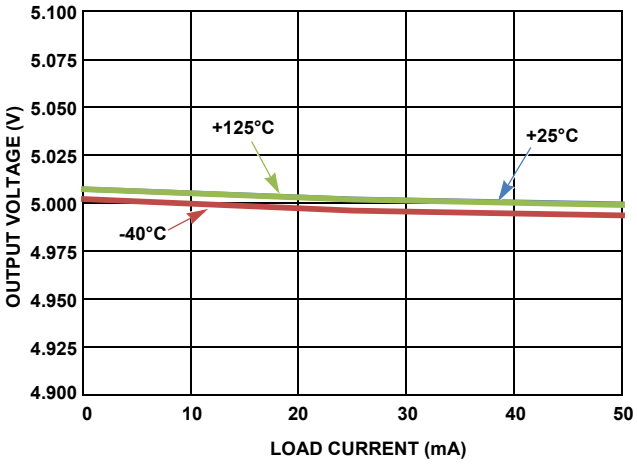


FIGURE 7. OUTPUT VOLTAGE vs LOAD CURRENT

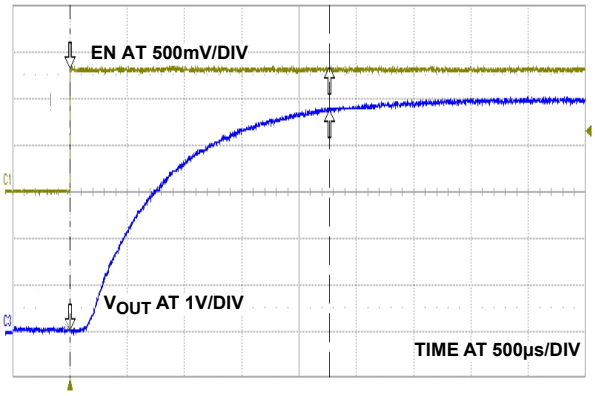


FIGURE 8. START-UP WAVEFORM

Typical Performance Curves V_{IN} = 14V, I_{OUT} = 1mA, V_{OUT} = 5V, T_J = +25 °C unless otherwise specified. **(Continued)**

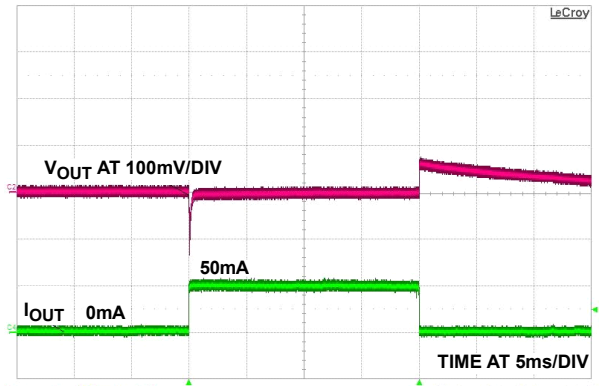


FIGURE 9. LOAD TRANSIENT RESPONSE

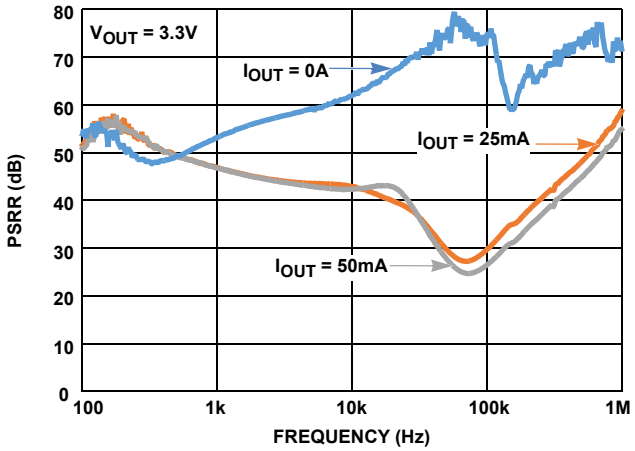


FIGURE 10. PSRR vs FREQUENCY FOR VARIOUS LOAD CURRENT, V_{OUT} = 3.3V

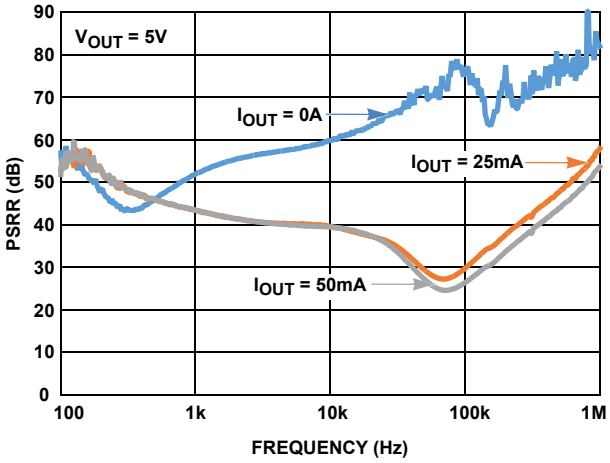
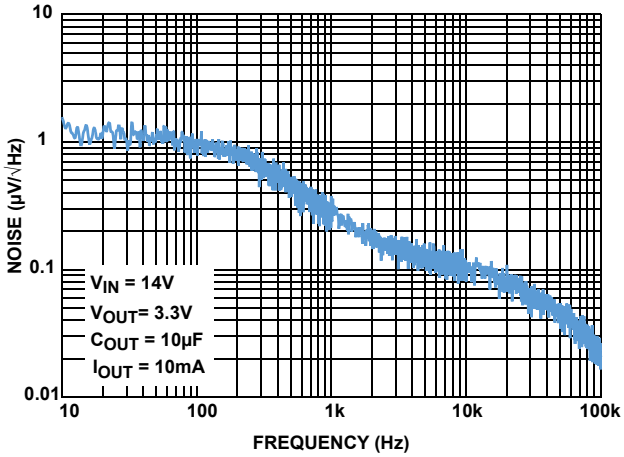
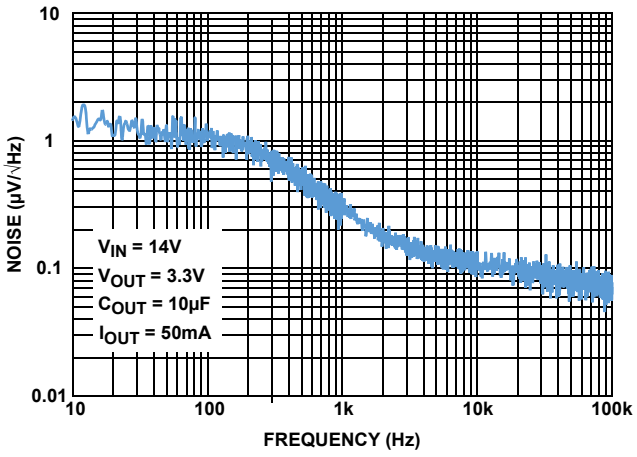


FIGURE 11. PSRR vs FREQUENCY FOR VARIOUS LOAD CURRENT, V_{OUT} = 5V



BW = 100<f<100kHz output noise voltage ~26 μV_{RMS}

FIGURE 12. OUTPUT NOISE SPECTRAL DENSITY, I_{OUT} = 10mA



BW = 100<f<100kHz output noise voltage ~33 μV_{RMS}

FIGURE 13. OUTPUT NOISE SPECTRAL DENSITY, I_{OUT} = 50mA

Functional Description

Functional Overview

The ISL80136 is a high performance, high voltage, low-dropout regulator (LDO) with 50mA sourcing capability. The part is rated to operate across the -40°C to +125°C temperature range. Featuring ultra-low quiescent current, it makes an ideal choice for “always-on” applications. It works well under a “load dump condition” where the input voltage could rise up to 40V. The device also features current limit and thermal shutdown protection.

Enable Control

When the ISL80136's Enable pin is pulled low, the IC goes into shutdown mode. In this condition, the device draws less than 2µA of current. Driving the pin high turns the device on. Tie the EN pin directly to IN for “always on” operation.

Current Limit Protection

The ISL80136 has internal current limit functionality to protect the regulator during fault conditions. During current limit, the output sources a fixed amount of current largely independent of the output voltage. If the short or overload is removed from V_{OUT}, the output returns to normal voltage regulation mode.

Thermal Fault Protection

If the die temperature exceeds typically +165°C, the output of the LDO shuts down until the die temperature cools down to typically +145°C. The level of power dissipated, combined with the ambient temperature and the thermal impedance of the package, determine if the junction temperature exceeds the thermal shutdown temperature. Also see the section on “Power Dissipation”.

Application Information

Input and Output Capacitors

Renesas recommends placing a ceramic capacitor (X5R or X7R) at the ISL80136's output to maintain stability. Route the ground connection of the output capacitor directly to the GND pin of the device and place it close to the IC. A minimum 0.1µF (X5R or X7R) capacitor is recommended at the input.

Output Voltage Setting

The output voltage is programmed using an external resistor divider, as shown in Figure 14.

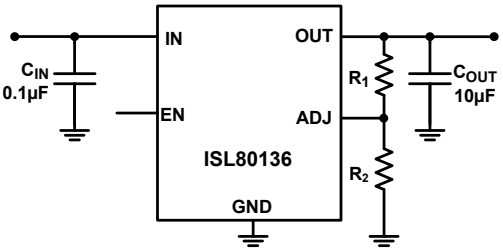


FIGURE 14. SETTING OUTPUT VOLTAGE

The output voltage is calculated using Equation 1:

$$V_{OUT} = 1.223V \times \left(\frac{R_1}{R_2} + 1\right) \quad \text{(EQ. 1)}$$

Power Dissipation

The junction temperature must not exceed the range specified in “Recommended Operating Conditions” on page 4. The power dissipation can be calculated using Equation 2:

$$P_D = (V_{IN} - V_{OUT}) \times I_{OUT} + V_{IN} \times I_{GND} \quad \text{(EQ. 2)}$$

The maximum allowable junction temperature, $T_{J(MAX)}$ and the maximum expected ambient temperature, $T_{A(MAX)}$ determine the maximum allowable junction temperature rise (ΔT_J), as shown in Equation 3:

$$\Delta T_J = T_{J(MAX)} - T_{A(MAX)} \quad \text{(EQ. 3)}$$

To calculate the maximum ambient operating temperature, use the junction-to-ambient thermal resistance (θ_{JA}), as shown in Equation 4:

$$T_{J(MAX)} = P_{D(MAX)} \times \theta_{JA} + T_A \quad \text{(EQ. 4)}$$

Board Layout Recommendations

A good PCB layout is important to achieve expected performance. When placing the components and routing the trace, minimize the ground impedance and keep the parasitic inductance low. The input and output capacitors should have a good ground connection and be placed as close to the IC as possible. The ADJ feedback trace should be away from other noisy traces. Connect the exposed pad to the ground plane using as many vias as possible within the pad for the best thermal relief.

Revision History

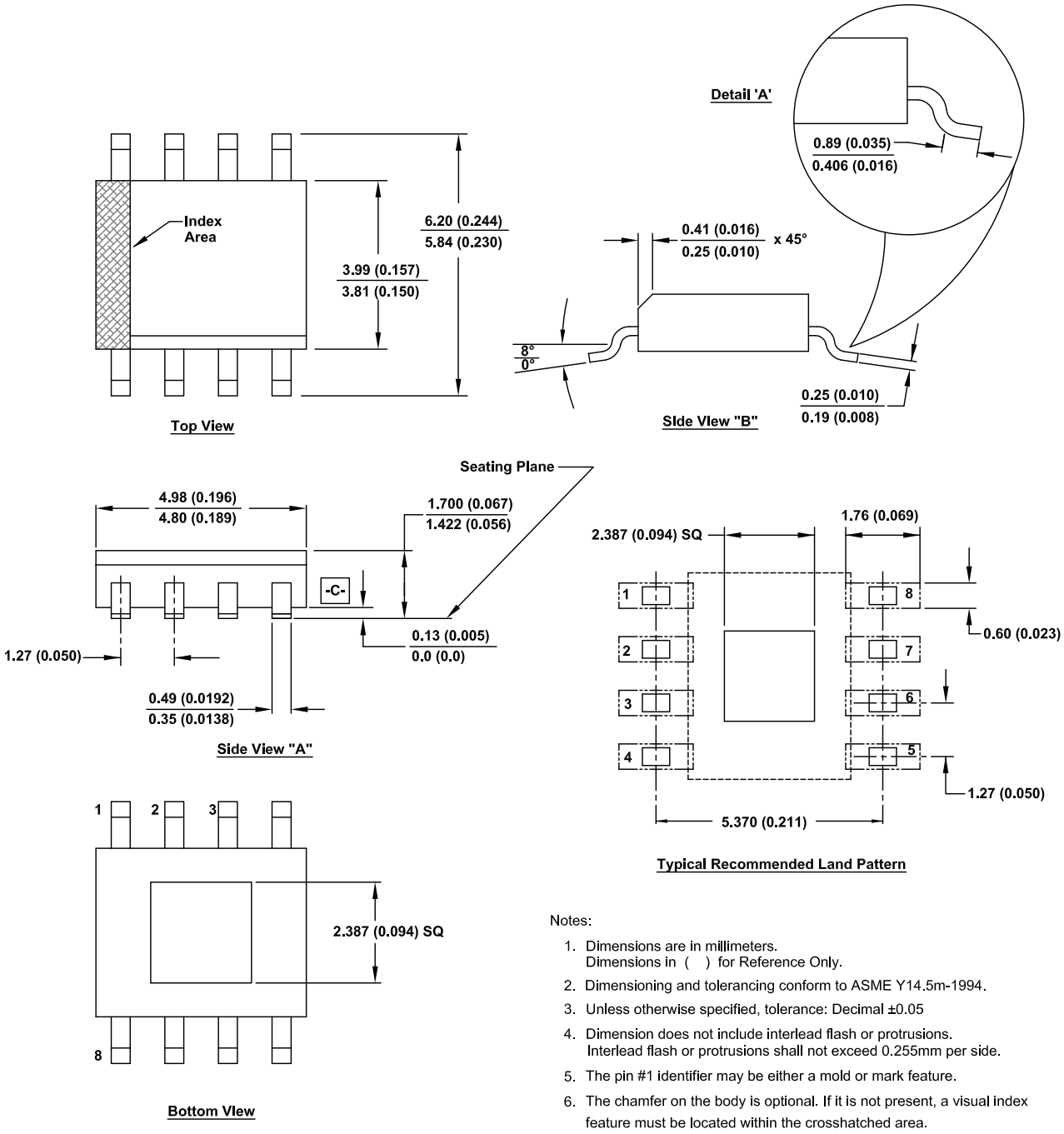
The revision history provided is for informational purposes only and is believed to be accurate, but not warranted. Please go to web to make sure you have the latest Rev.

DATE	REVISION	CHANGE
Oct 2, 2023	4.01	Updated M8.15B POD to the latest revision (corrected typo).
Aug 8, 2019	4.0	Updated POD to the latest revision. Changes are as follows: -Updated L Millimeter minimum in detail A from 0.41 to 0.406. -Updated the following in the Side View: -Changed total package height Millimeter MIN and MAX values from: 1.43 MIN and 1.68 MAX to: 1.422 MIN and 1.700 MAX and Inches max from 0.066 to 0.067. -Changed A1 Inches MIN from: 0.001 to 0.0, and A1 Millimeters MIN from 0.03 to 0.0
Feb 20, 2019	3.0	Updated title Updated Table 1 and moved to page 2. Updated the 6th bullet and added the 8th bullet in the features list. Updated Related Literature section. Updated ordering information table with tape and reel information to table and updated notes. Added Output Voltage Noise specification. Removed About Intersil section. Updated POD to the latest revision. Changes to POD are as follows: -Replace the graphics with a standard format (removing the dimension table). Updated disclaimer.
Aug 11, 2015	2.0	Removed DFN package option throughout the datasheet. On page 1, updated Key Differences Table, Replaced “ADJ OR FIXED VOUT” Column with “IC PACKAGE” column. On page 2, updated Block Diagram, removed two resistors and switched polarity of EA. Electrical spec table on page 4: -Removed “C_{IN} = 0.1µF, C_{OUT} = 10µF” from the Electrical Specification heading. -Updated the ADJ Reference Voltage Test Condition IOUT value from “IOUT = 0.1mA” to “IOUT = 0.1mA to 50mA” -Updated the Line Regulation *Symbol, from “$\Delta V_{OUT}/\Delta V_{IN}$” to “($V_{OUT}$ low line - V_{OUT} high line)/V_{OUT} low line”. *Test Conditions, from “3V ≤ V_{IN} ≤ 40V, I_{OUT} = 1mA” to “6V < V_{IN} < 40V, I_{OUT} = 1mA” -Updated the Load Regulation *Symbol, from “$\Delta V_{OUT}/\Delta I_{OUT}$” to “($V_{OUT}$ no load - V_{OUT} high load)/V_{OUT} no load” *Test Conditions from “V_{IN} = V_{OUT} +V_{DO}” to “V_{IN} = 14V” -Updated Dropout Voltage Test Condition VOUT value (First two rows only) from “VOUT = 3.3V” to “VOUT = 2.5V”. Updated Note 6 from “Dropout voltage is defined as (V_{IN} - V_{OUT}) when V_{OUT} is 2% below the value of V_{OUT} when V_{IN} = V_{OUT} + 3V.” to “Dropout voltage is defined as (V_{IN} - V_{OUT}) when V_{OUT} is 2% below the value of V_{OUT}.” Removed Figure 9, “POWER SUPPLY REJECTION RATIO (LOAD = 50mA)” Added figures 10 through 13 on page 7.
Jan 31, 2012	1.0	Added DFN package option throughout the datasheet.
Dec 15, 2011	0.0	Initial Release.

Package Outline Drawing

For the most recent package outline drawing, see M8.15B.

M8.15B
8 Lead Narrow Body Small Outline Exposed Pad Plastic Package
Rev 8, 9/2023



Notes:

1. Dimensions are in millimeters.
   Dimensions in ( ) for Reference Only.
2. Dimensioning and tolerancing conform to ASME Y14.5m-1994.
3. Unless otherwise specified, tolerance: Decimal ±0.05
4. Dimension does not include interlead flash or protrusions.
   Interlead flash or protrusions shall not exceed 0.255mm per side.
5. The pin #1 identifier may be either a mold or mark feature.
6. The chamfer on the body is optional. If it is not present, a visual index feature must be located within the crosshatched area.

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Parça koduyla arama

Üretici parça numarasını yazın; stok ve fiyatı hemen görün.

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Entegreden kapasitöre tüm elektronik komponent kategorileri.

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Üreticileri görün

Toplu alım ve teklif

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Teklif isteyin

www.entegreci.com | **destek@entegreci.com** | **0850 305 90 34**

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