ISL9000A

Dual LDO with Low Noise, Very High PSRR and Low IQ

FN6391
Rev 3.00
October 15, 2015

ISL9000A is a high performance dual LDO capable of sourcing 300mA current from each output. It has a low standby current and very high PSRR and is stable with output capacitance of 1µF to 10µF with ESR of up to 200mΩ.

The device integrates an individual Power-On-Reset (POR) function for each output. The POR delay for VO2 can be externally programmed by connecting a timing capacitor to the CPOR pin. The POR delay for VO1 is internally fixed at approximately 2ms. A reference bypass pin is also provided for connecting a noise filtering capacitor for low noise and high-PSRR applications.

The quiescent current is typically only 42µA with both LDO's enabled and active. Separate enable pins control each individual LDO output. When both enable pins are low, the device is in shutdown, typically drawing less than 0.1µA.

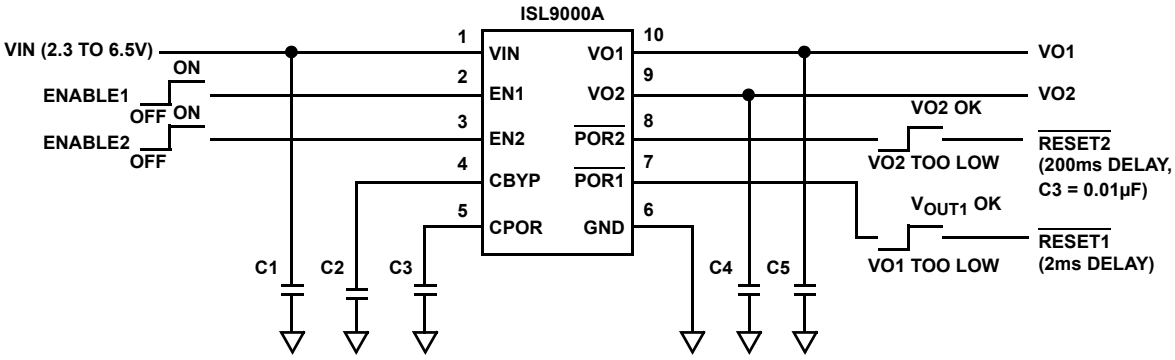
Several combinations of voltage outputs are standard. Output voltage options for each LDO range from 1.5V to 3.3V. Other output voltage options may be available upon request.

Features

- Integrates two 300mA high performance LDOs
- Excellent transient response to large current steps
- ±1.8% accuracy over all operating conditions
- Excellent load regulation: < 0.1% voltage change across full range of load current
- Low output noise: typically 30µV_{RMS} @ 100µA (1.5V)
- Very high PSRR: 90dB @ 1kHz
- Extremely low quiescent current: 42µA (both LDOs active)
- Wide input voltage capability: 2.3V to 6.5V
- Low dropout voltage: typically 200mV @ 300mA
- Stable with 1µF to 10µF ceramic capacitors
- Separate enable and POR pins for each LDO
- Soft-start and staged turn-on to limit input current surge during enable
- Current limit and overheat protection
- Tiny 10 Ld 3mmx3mm DFN package
- -40°C to +85°C operating temperature range
- Pb-free (RoHS compliant)

Applications

- PDAs, Cell Phones and Smart Phones
- Portable Instruments, MP3 Players
- Handheld Devices including Medical Handheld



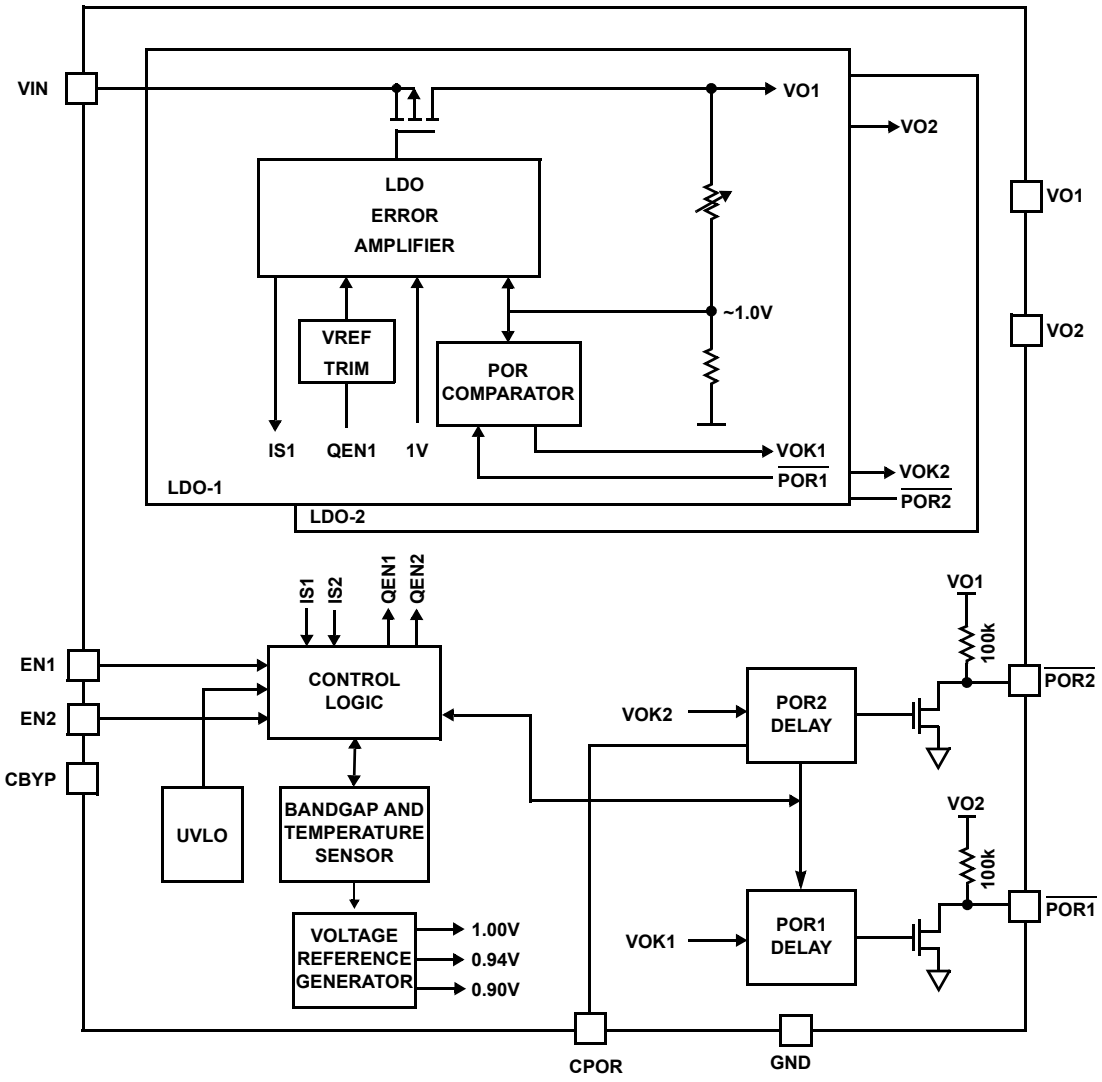
C1, C4, C5: 1µF X5R CERAMIC CAPACITOR

C2: 0.1µF X7R CERAMIC CAPACITOR

C3: 0.01µF X7R CERAMIC CAPACITOR

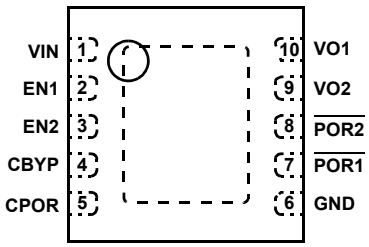
FIGURE 1. TYPICAL APPLICATION

Block Diagram



Pin Configuration

ISL9000A
(10 LD 3X3 DFN)
TOP VIEW



Pin Descriptions

PIN NUMBER	PIN NAME	TYPE	DESCRIPTION
1	VIN	Analog I/O	Supply Voltage/LDO Input: Connect a 1µF, X5R ceramic capacitor to GND.
2	EN1	Low Voltage Compatible CMOS Input	LDO-1 Enable.
3	EN2	Low Voltage Compatible CMOS Input	LDO-2 Enable.
4	CBYP	Analog I/O	Reference Bypass Capacitor Pin: Optionally connect capacitor of value 0.01µF to 1µF between this pin and GND to tune in the desired noise and PSRR performance.
5	CPOR	Analog I/O	POR2 Delay Setting Capacitor Pin: Connect a capacitor between this pin and GND to delay the $\overline{\text{POR2}}$ output release after LDO-2 output reaches 94% of its specified voltage level. (200ms delay per 0.01µF).
6	GND	Ground	GND is the connection to system ground. Connect to PCB Ground plane.
7	$\overline{\text{POR1}}$	Open Drain Output (1mA)	Open-drain POR Output for LDO-1 (active-low): Internally connected to VO1 through 100kΩ resistor.
8	$\overline{\text{POR2}}$	Open Drain Output (1mA)	Open-drain POR Output for LDO-2 (active-low): Internally connected to VO2 through 100kΩ resistor.
9	VO2	Analog I/O	LDO-2 Output: Connect capacitor of value 1µF to 10µF to GND (1µF recommended).
10	VO1	Analog I/O	LDO-1 Output: Connect capacitor of value 1µF to 10µF to GND (1µF recommended).

Ordering Information

PART NUMBER (Notes 1, 3)	PART MARKING	VO1 VOLTAGE (V) (Note 2)	VO2 VOLTAGE (V) (Note 2)	TEMP RANGE (°C)	PACKAGE (Pb-Free)	PKG DWG. #
ISL9000AIRNNZ	DEYA	3.3	3.3	-40 to +85	10 Ld 3x3 DFN	L10.3x3C
ISL9000AIRNJZ	DEWA	3.3	2.8	-40 to +85	10 Ld 3x3 DFN	L10.3x3C
ISL9000AIRNFZ	DEVA	3.3	2.5	-40 to +85	10 Ld 3x3 DFN	L10.3x3C
ISL9000AIRNCZ (No longer available, recommended replacement: ISL9000AIRNJZ)	DETA	3.3	1.8	-40 to +85	10 Ld 3x3 DFN	L10.3x3C
ISL9000AIRMNZ	DESA	3.0	3.3	-40 to +85	10 Ld 3x3 DFN	L10.3x3C
ISL9000AIRMMZ (No longer available, recommended replacement: ISL9000AIRMGZ-T)	DERA	3.0	3.0	-40 to +85	10 Ld 3x3 DFN	L10.3x3C
ISL9000AIRMGZ	DEPA	3.0	2.7	-40 to +85	10 Ld 3x3 DFN	L10.3x3C
ISL9000AIRLLZ	DENA	2.9	2.9	-40 to +85	10 Ld 3x3 DFN	L10.3x3C
ISL9000AIRKNZ (No longer available, recommended replacement: ISL9000AIRKCZ-T)	DELA	2.85	3.3	-40 to +85	10 Ld 3x3 DFN	L10.3x3C
ISL9000AIRKKZ	DEKA	2.85	2.85	-40 to +85	10 Ld 3x3 DFN	L10.3x3C
ISL9000AIRKJZ	DEJA	2.85	2.8	-40 to +85	10 Ld 3x3 DFN	L10.3x3C
ISL9000AIRKFZ	DEHA	2.85	2.5	-40 to +85	10 Ld 3x3 DFN	L10.3x3C
ISL9000AIRKPZ (No longer available, recommended replacement: ISL9000AIRKCZ-T)	DEMA	2.85	1.85	-40 to +85	10 Ld 3x3 DFN	L10.3x3C
ISL9000AIRKCZ	DEGA	2.85	1.8	-40 to +85	10 Ld 3x3 DFN	L10.3x3C
ISL9000AIRJNZ	DEEA	2.8	3.3	-40 to +85	10 Ld 3x3 DFN	L10.3x3C
ISL9000AIRJMZ (No longer available, recommended replacement: ISL9000AIRJBZ-T)	DEDA	2.8	3.0	-40 to +85	10 Ld 3x3 DFN	L10.3x3C
ISL9000AIRJRZ (No longer available, recommended replacement: ISL9000AIRJNZ-T)	DEFA	2.8	2.6	-40 to +85	10 Ld 3x3 DFN	L10.3x3C
ISL9000AIRJCZ (No longer available, recommended replacement: ISL9000AIRJBZ-T)	DECA	2.8	1.8	-40 to +85	10 Ld 3x3 DFN	L10.3x3C
ISL9000AIRJBZ	DEBA	2.8	1.5	-40 to +85	10 Ld 3x3 DFN	L10.3x3C
ISL9000AIRFJZ	DDVA	2.5	2.8	-40 to +85	10 Ld 3x3 DFN	L10.3x3C
ISL9000AIRFDZ	DDTA	2.5	2.0	-40 to +85	10 Ld 3x3 DFN	L10.3x3C
ISL9000AIRFCZ	DDSA	2.5	1.8	-40 to +85	10 Ld 3x3 DFN	L10.3x3C
ISL9000AIRCJZ	DDRA	1.8	2.8	-40 to +85	10 Ld 3x3 DFN	L10.3x3C
ISL9000AIRCCZ	DDPA	1.8	1.8	-40 to +85	10 Ld 3x3 DFN	L10.3x3C

NOTES:

1. Add "-T*" suffix for tape and reel. Please refer to TB347 for details on reel specifications.
2. For other output voltages, contact Intersil Marketing.
3. These Intersil Pb-free plastic packaged products employ special Pb-free material sets, molding compounds/die attach materials, and 100% matte tin plate plus anneal (e3 termination finish, which is RoHS compliant and compatible with both SnPb and Pb-free soldering operations). Intersil Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J STD-020.

Evaluation Board Ordering Information

PART NUMBER	VO1 VOLTAGE (V)	VO2 VOLTAGE (V)
ISL9000AIRNJZ-EVZ	3.3	2.8
ISL9000AIRNFZ-EVZ	3.3	2.5
ISL9000AIRMNZ-EVZ	3.0	3.3
ISL9000AIRMGZ-EVZ	3.0	2.7
ISL9000AIRKKZ-EVZ	2.85	2.85
ISL9000AIRKJZ-EVZ	2.85	2.8
ISL9000AIRKFZ-EVZ	2.85	2.5
ISL9000AIRKCZ-EVZ	2.85	1.8
ISL9000AIRJNZ-EVZ	2.8	3.3
ISL9000AIRJBZ-EVZ	2.8	1.5
ISL9000AIRFJZ-EVZ	2.5	2.8
ISL9000AIRFDZ-EVZ	2.5	2.0
ISL9000AIRFCZ-EVZ	2.5	1.8
ISL9000AIRCCZ-EVZ	1.8	1.8

Absolute Maximum Ratings

Supply Voltage (VIN) . . . . . +7.1V
VO1, VO2 Pins . . . . . +3.6V
All Other Pins . . . . . -0.3 to (VIN + 0.3)V

Recommended Operating Conditions

Ambient Temperature Range (T_A) . . . . . -40°C to +85°C
Supply Voltage (VIN) . . . . . 2.3V to 6.5V

Thermal Information

Thermal Resistance (Notes 4, 5)	θ_{JA} (°C/W)	θ_{JC} (°C/W)
10 Ld 3x3 DFN Package	52.8	11

Junction Temperature Range . . . . . -40°C to +125°C
Operating Temperature Range . . . . . -40°C to +85°C
Storage Temperature Range . . . . . -65°C to +150°C
Pb-free Reflow Profile . . . . . see link below
http://www.intersil.com/pbfree/Pb-FreeReflow.asp

CAUTION: Do not operate at or near the maximum ratings listed for extended periods of time. Exposure to such conditions may adversely impact product reliability and result in failures not covered by warranty.

NOTES:

4. θ_{JA} is measured in free air with the component mounted on a high effective thermal conductivity test board with "direct attach" features. See Tech Brief TB379.
5. For θ_{JC}, the "case temp" location is the center of the exposed metal pad on the package underside.

Electrical Specifications

Unless otherwise noted, all parameters are guaranteed over the operational supply voltage and temperature range of the device as follows: T_A = -40°C to +85°C; VIN = (V_O + 0.5V) to 6.5V with a minimum VIN of 2.3V; C_{IN} = 1µF; C_O = 1µF; C_{BYP} = 0.01µF; C_{POR} = 0.01µF. **Boldface limits apply over the operating temperature range, -40°C to +85°C.**

PARAMETER	SYMBOL	TEST CONDITIONS	MIN (Note 8)	TYP	MAX (Note 8)	UNITS
DC CHARACTERISTICS						
Supply Voltage	VIN		**2.3**		**6.5**	V
Ground Current		Quiescent condition: I_{O1} = 0µA; I_{O2} = 0µA				
	I_{DD1}	One LDO active		25	**32**	µA
	I_{DD2}	Both LDO active		42	**52**	µA
Shutdown Current	I_{DDS}	@ +25°C		0.1	1.0	µA
UVLO Threshold	V_{UV+}		**1.9**	2.1	**2.3**	V
	V_{UV-}		**1.6**	1.8	**2.0**	V
Regulation Voltage Accuracy		Initial accuracy at VIN = V_O + 0.5V, I_O = 10mA, T_J = +25°C	-0.7		+0.7	%
		VIN = V_O + 0.5V to 5.5V, I_O = 10µA to 300mA, T_J = +25°C	-0.8		+0.8	%
		VIN = V_O + 0.5V to 5.5V, I_O = 10µA to 300mA, T_J = -40°C to +125°C	-1.8		+1.8	%
Maximum Output Current	I_{MAX}	Continuous	**300**			mA
Internal Current Limit	I_{LIM}		**350**	475	**600**	mA
Dropout Voltage (Note 7)	V_{DO1}	I_O = 300mA; $V_O < 2.5V$		300	**500**	mV
	V_{DO2}	I_O = 300mA; $2.5V \le V_O \le 2.8V$		250	**400**	mV
	V_{DO3}	I_O = 300mA; $V_O > 2.8V$		200	**325**	mV
Thermal Shutdown Temperature	T_{SD+}			145		°C
	T_{SD-}			110		°C
AC CHARACTERISTICS						
Ripple Rejection (Note 6)		I_O = 10mA, VIN = 2.8V(min), V_O = 1.8V, C_{BYP} = 0.1µF				
		@ 1kHz		90		dB
		@ 10kHz		70		dB
		@ 100kHz		50		dB
Output Noise Voltage (Note 6)		I_O = 100µA, V_O = 1.5V, T_A = +25°C, C_{BYP} = 0.1µF BW = 10Hz to 100kHz		30		μV_{RMS}

Electrical Specifications Unless otherwise noted, all parameters are guaranteed over the operational supply voltage and temperature range of the device as follows: T_A = -40°C to +85°C; VIN = (V_O + 0.5V) to 6.5V with a minimum VIN of 2.3V; C_{IN} = 1µF; C_O = 1µF; C_{BYP} = 0.01µF; C_{POR} = 0.01µF. **Boldface limits apply over the operating temperature range, -40°C to +85°C. (Continued)**

PARAMETER	SYMBOL	TEST CONDITIONS	MIN (Note 8)	TYP	MAX (Note 8)	UNITS
DEVICE START-UP CHARACTERISTICS						
Device Enable Time	t_{EN}	Time from assertion of the ENx pin to when the output voltage reaches 95% of the VOx(NOM)		250	**500**	µs
LDO Soft-Start Ramp Rate	t_{SSR}	Slope of linear portion of LDO output voltage ramp during start-up		30	**60**	µs/V
EN1, EN2 PIN CHARACTERISTICS						
Input Low Voltage	V_{IL}		**-0.3**		**0.5**	V
Input High Voltage	V_{IH}		**1.4**		**VIN + 0.3**	V
Input Leakage Current	I_{IL}, I_{IH}				**0.1**	µA
Pin Capacitance	C_{PIN}	Informative		5		pF
$\overline{POR1}$, $\overline{POR2}$ PIN CHARACTERISTICS						
$\overline{POR1}$, $\overline{POR2}$ Thresholds	V_{POR+}	As a percentage of nominal output voltage	**91**	94	**97**	%
	V_{POR-}		**87**	90	**93**	%
$\overline{POR1}$ Delay	t_{P1LH}		**1.0**	2.0	**3.0**	ms
	t_{P1HL}			25		µs
$\overline{POR2}$ Delay	t_{P2LH}	C_{POR} = 0.01µF	**100**	200	**300**	ms
	t_{P2HL}			25		µs
$\overline{POR1}$, $\overline{POR2}$ Pin Output Low Voltage	V_{OL}	@ I_{OL} = 1.0mA			**0.2**	V
$\overline{POR1}$, $\overline{POR2}$ Pin Internal Pull-Up Resistance	R_{POR}		**78**	100	**180**	kΩ

NOTES:

6. Limits established by characterization and are not production tested.
7. VOx = 0.98*VOx(NOM); Valid for VOx greater than 1.85V.
8. Parameters with MIN and/or MAX limits are 100% tested at +25°C, unless otherwise specified. Temperature limits established by characterization and are not production tested.

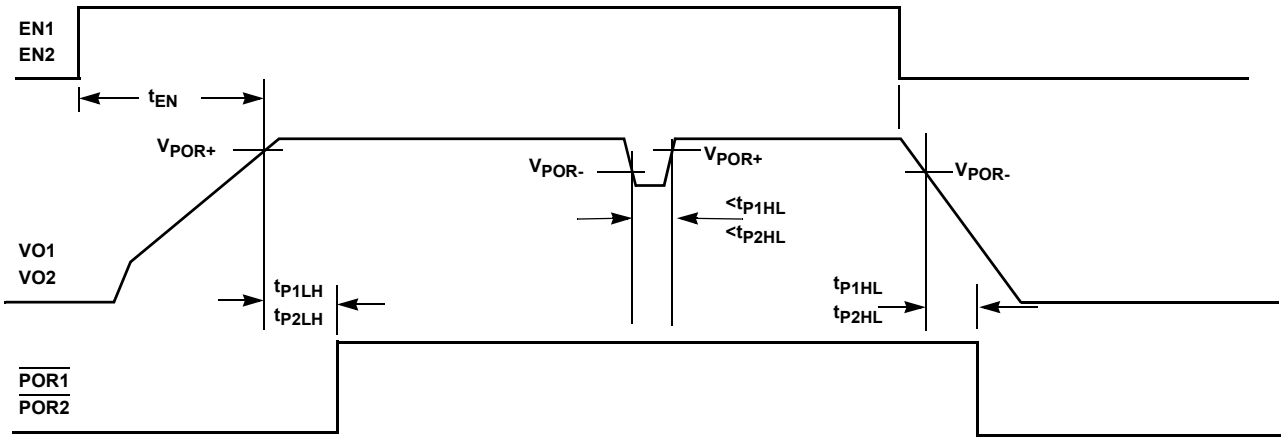


FIGURE 2. TIMING PARAMETER DEFINITION

Typical Performance Curves

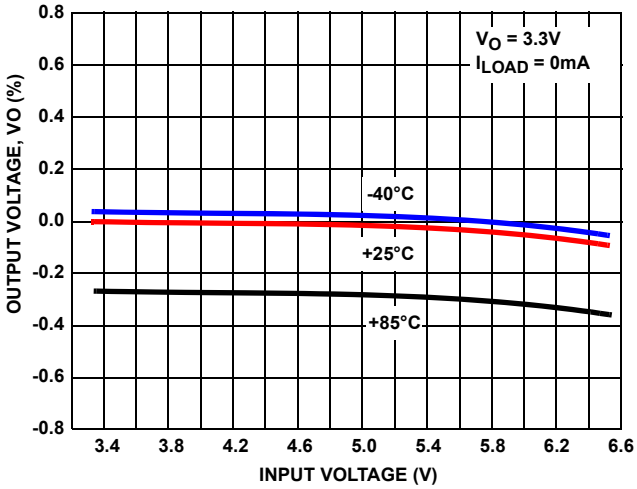


FIGURE 3. OUTPUT VOLTAGE vs INPUT VOLTAGE (3.3V OUTPUT)

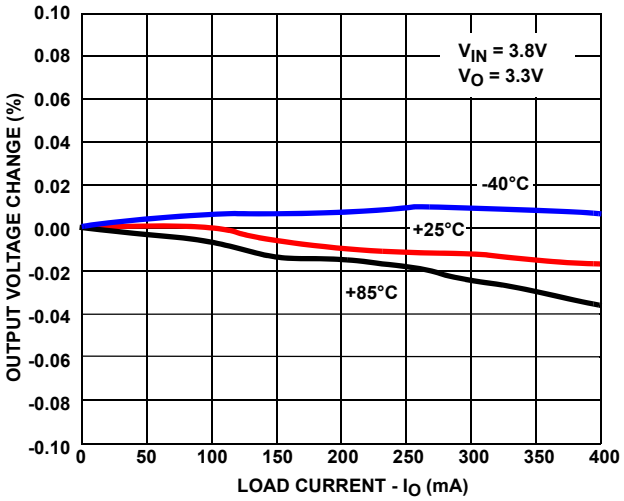


FIGURE 4. OUTPUT VOLTAGE CHANGE vs LOAD CURRENT

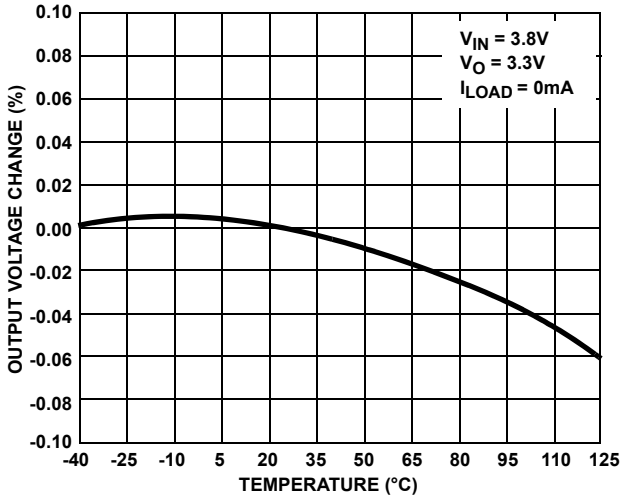


FIGURE 5. OUTPUT VOLTAGE CHANGE vs TEMPERATURE

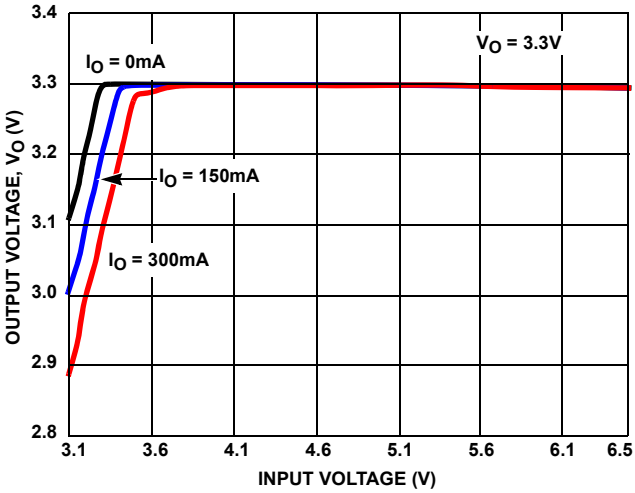


FIGURE 6. OUTPUT VOLTAGE vs INPUT VOLTAGE (3.3V OUTPUT)

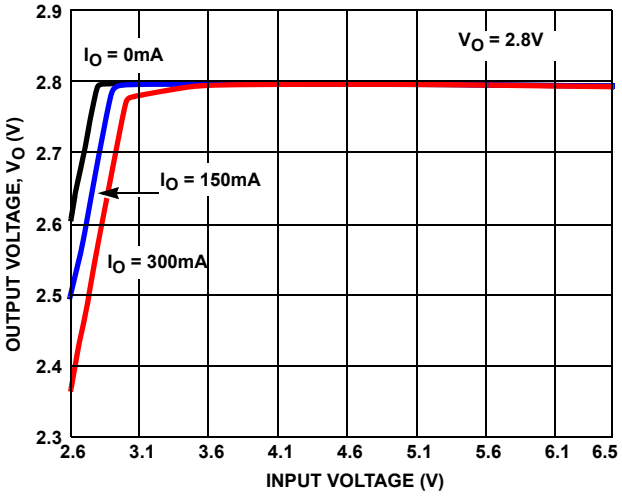


FIGURE 7. OUTPUT VOLTAGE vs INPUT VOLTAGE (2.8V OUTPUT)

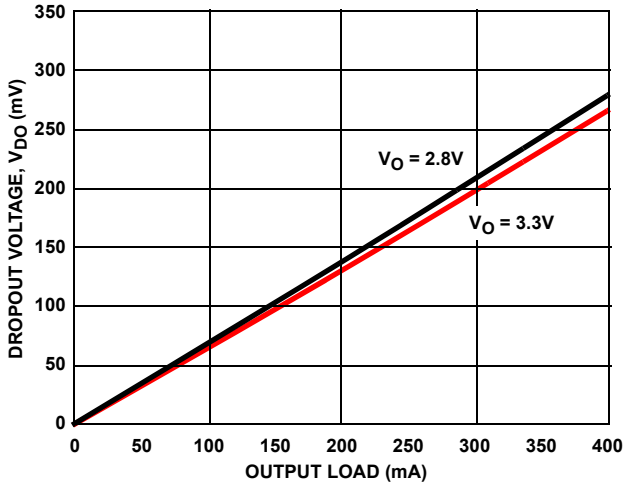


FIGURE 8. DROPOUT VOLTAGE vs LOAD CURRENT

Typical Performance Curves (Continued)

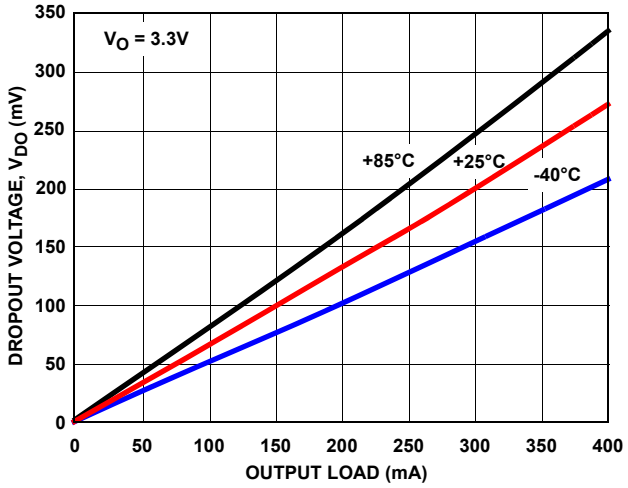


FIGURE 9. DROPOUT VOLTAGE vs LOAD CURRENT

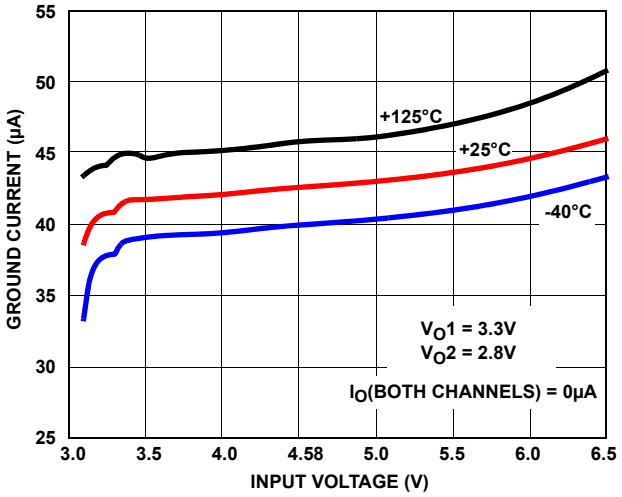


FIGURE 10. GROUND CURRENT vs INPUT VOLTAGE

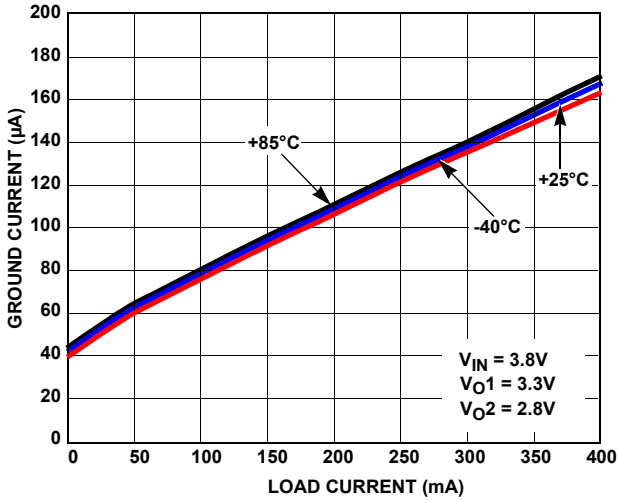


FIGURE 11. GROUND CURRENT vs LOAD

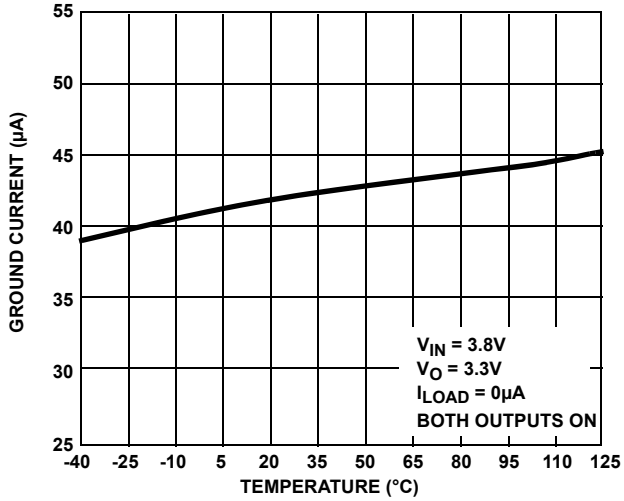


FIGURE 12. GROUND CURRENT vs TEMPERATURE

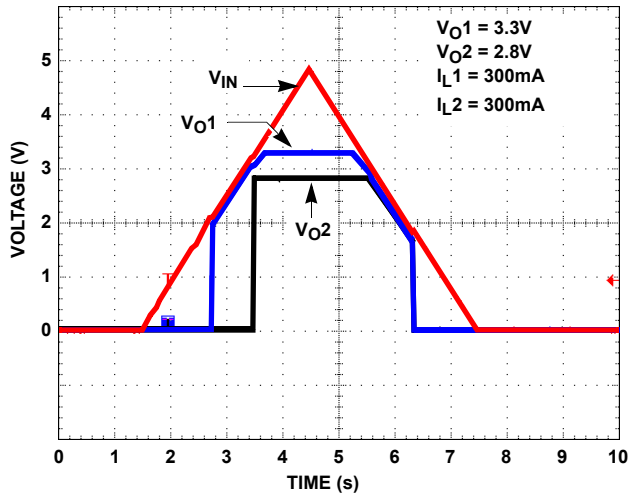


FIGURE 13. POWER-UP/POWER-DOWN

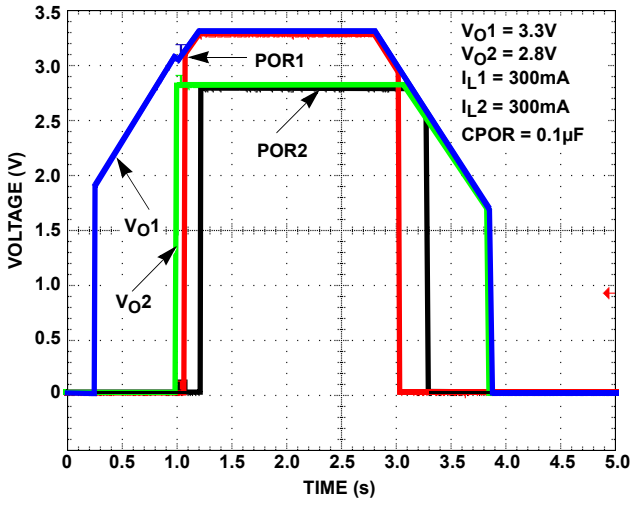


FIGURE 14. POWER-UP/POWER-DOWN WITH POR SIGNALS

Typical Performance Curves (Continued)

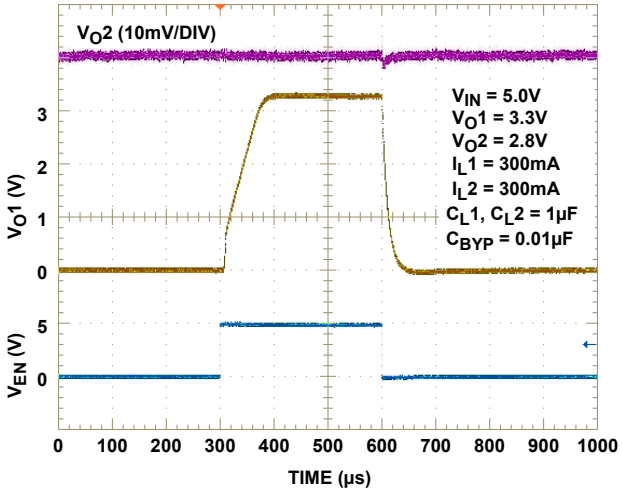


FIGURE 15. TURN-ON/TURN-OFF RESPONSE

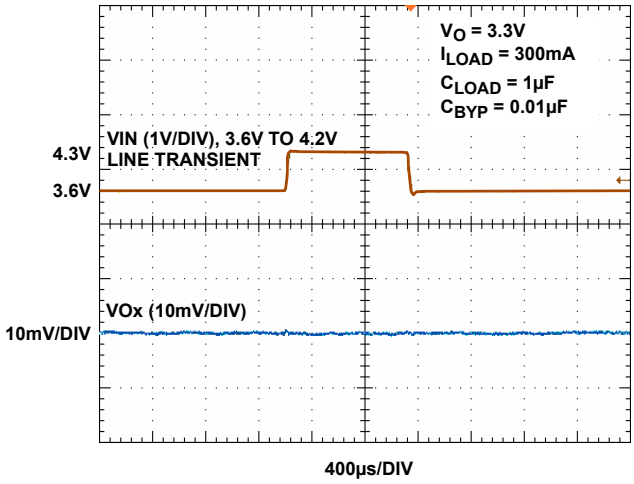


FIGURE 16. LINE TRANSIENT RESPONSE (3.3V OUTPUT)

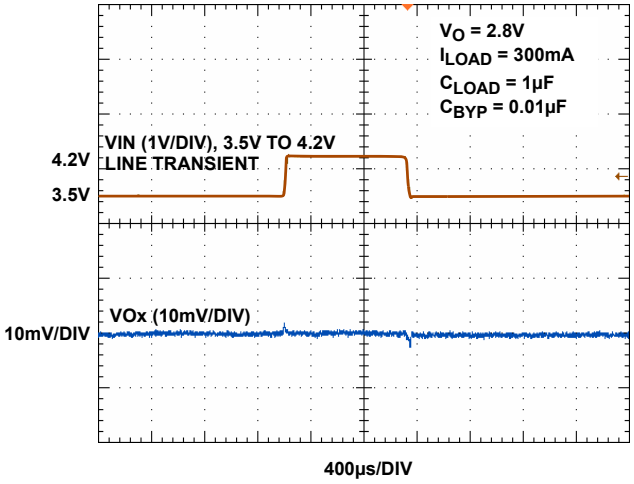


FIGURE 17. LINE TRANSIENT RESPONSE (2.8V OUTPUT)

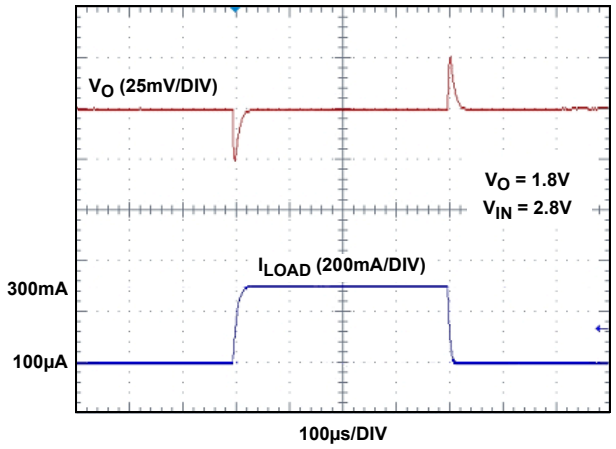


FIGURE 18. LOAD TRANSIENT RESPONSE

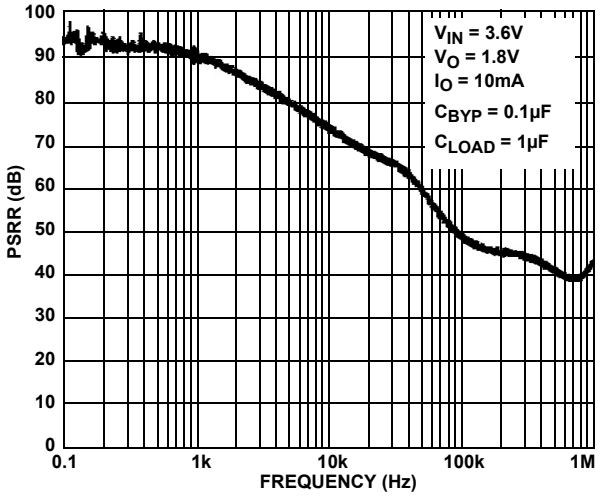


FIGURE 19. PSRR vs FREQUENCY

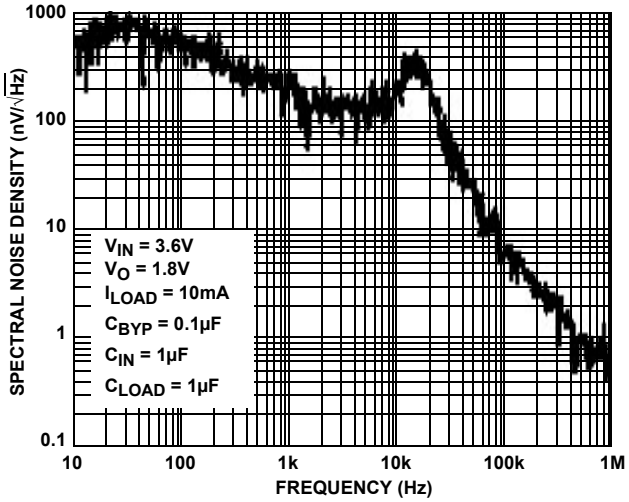


FIGURE 20. SPECTRAL NOISE DENSITY vs FREQUENCY

Functional Description

The ISL9000A contains two high performance LDO's. High performance is achieved through a circuit that delivers fast transient response to varying load conditions. In a quiescent condition, the ISL9000A adjusts its biasing to achieve the lowest standby current consumption.

The device also integrates current limit protection, smart thermal shutdown protection, staged turn-on and soft-start. Smart thermal shutdown protects the device against overheating. Staged turn-on and soft-start minimize start-up input current surges without causing excessive device turn-on time.

Power Control

The ISL9000A has two separate enable pins (EN1 and EN2) to individually control power to each of the LDO outputs. When both EN1 and EN2 are LOW, the device is in shutdown mode. During this condition, all on-chip circuits are OFF, and the device draws minimum current, typically less than 0.1µA.

When one or both of the enable pins are asserted, the device first polls the output of the UVLO detector to ensure that VIN voltage is at least about 2.1V. Once verified, the device initiates a start-up sequence. During the start-up sequence, trim settings are first read and latched. Then, sequentially, the bandgap, reference voltage and current generation circuitry power-up. Once the references are stable, a fast-start circuit quickly charges the external reference bypass capacitor (connected to the CBYP pin) to the proper operating voltage. After the bypass capacitor has been charged, the LDOs power-up in their specified sequence.

Soft-start circuitry integrated into each LDO limits the initial ramp-up rate to about 30µs/V to minimize current surge.

If EN1 is brought HIGH, and EN2 goes HIGH before the VO1 output stabilizes, the ISL9000A delays the VO2 turn-on until the VO1 output reaches its target level.

If EN2 is brought high, and EN1 goes HIGH before VO2 starts its output ramp, then VO1 turns on first and, the ISL9000A delays the VO2 turn-on until the VO1 output reaches its target level.

If EN2 is brought HIGH, and EN1 goes HIGH after VO2 starts its output ramp, then the ISL9000A immediately starts to ramp up the VO1 output.

If both EN1 and EN2 are brought HIGH at the same time, the VO1 output has priority, and is always powered up first.

During operation, whenever the VIN voltage drops below about 1.8V, the ISL9000A immediately disables both LDO outputs. When VIN rises back above 2.1V, the device re-initiates its start-up sequence and LDO operation will resume automatically.

Reference Generation

The reference generation circuitry includes a trimmed bandgap, a trimmed voltage reference divider, a trimmed current reference generator, and an RC noise filter. The filter includes the external capacitor connected to the CBYP pin. A 0.01µF capacitor connected CBYP implements a 100Hz lowpass filter, and is recommended for most high performance applications. For the lowest noise application, a 0.1µF or greater CBYP capacitor should be used. This filters the reference noise below the 10Hz to 1kHz frequency band, which is crucial in many noise-sensitive applications.

The bandgap generates a zero temperature coefficient (TC) voltage for the reference divider. The reference divider provides the regulation reference, POR detection thresholds, and other voltage references required for current generation and over-temperature detection.

The current generator provides the references required for adaptive biasing as well as references for LDO output current limit and thermal shutdown determination.

LDO Regulation and Programmable Output Divider

The LDO Regulator is implemented with a high-gain operational amplifier driving a PMOS pass transistor. The design of the ISL9000A provides a regulator that has low quiescent current, fast transient response, and overall stability across all operating and load current conditions. LDO stability is guaranteed for a 1µF to 10µF output capacitor that has a tolerance better than 20% and ESR less than 200mΩ. The design is performance-optimized for a 1µF capacitor. Unless limited by the application, use of an output capacitor value above 4.7µF is not normally needed as LDO performance improvement is minimal.

Each LDO uses an independently trimmed 1V reference. An internal resistor divider drops the LDO output voltage down to 1V. This is compared to the 1V reference for regulation. The resistor division ratio is programmed in the factory to one of the following output voltages: 1.5V, 1.8V, 1.85V, 2.5V, 2.6V, 2.7V, 2.8V, 2.85V, 2.9V, 3.0V, and 3.3V.

Power-On Reset Generation

Each LDO has a separate Power-on Reset signal generation circuit which outputs to the respective $\overline{\text{POR}}$ pins. The POR signal is generated as follows:

A POR comparator continuously monitors the output of each LDO. The LDO enters a power-good state when the output voltage is above 94% of the expected output voltage for a period exceeding the LDO PGOOD entry delay time. In the power-good state, the open-drain $\overline{\text{POR}}$x output is in a high-impedance state. An internal 100kΩ pull-up resistor pulls the pin up to the respective LDO output voltage. An external resistor can be added between the $\overline{\text{POR}}$x output and the LDO output for a faster rise time, however, the $\overline{\text{POR}}$x output should not connect through an external resistor to a supply greater than the associated LDO voltage.

The power-good state is exited when the LDO output falls below 90% of the expected output voltage for a period longer than the PGOOD exit delay time. While power-good is false, the ISL9000A pulls the respective $\overline{\text{POR}}$ pin low.

For LDO-1, the PGOOD entry delay time is fixed at about 2ms while the PGOOD exit delay is about 25µs. For LDO-2, the PGOOD entry and exit delays are determined by the value of the external capacitor connected to the CPOR pin. For a 0.01µF capacitor, the entry and exit delays are 200ms and 25µs respectively. Larger or smaller capacitor values will yield proportionately longer or shorter delay times. The POR exit delay should never be allowed to be less than 10µs to ensure sufficient immunity against transient induced false POR triggering.

Overheat Detection

The bandgap provides a proportional-to-temperature current that is indicative of the temperature of the silicon. This current is compared with references to determine if the device is in danger of damage due to overheating. When the die temperature reaches about +145°C, one or both of the LDO's momentarily shut down until the die cools sufficiently. In the overheat condition, only the LDO sourcing more than 50mA will be shut off. This does not affect the operation of the other LDO. If both LDOs source more than 50mA and an overheat condition occurs, both LDO outputs are disabled. Once the die temperature falls back below about +110°C, the disabled LDO(s) are re-enabled and soft-start automatically takes place.

The ISL9000A provides short-circuit protection by limiting the output current to about 475mA. If short circuited, an output current of 475mA will cause die heating. If the short circuit lasts long enough, the overheat detection circuit will turn off the output.

Revision History

The revision history provided is for informational purposes only and is believed to be accurate, but not warranted. Please go to web to make sure you have the latest revision.

DATE	REVISION	CHANGE
October 15, 2015	FN6391.3	Updated Ordering Information Table on page 1. Updated "Evaluation Board Ordering Information" on page 5. Updated POD from rev 3 to rev 4. Changes since rev 3: Tiebar Note 4 updated From: Tiebar shown (if present) is a non-functional feature. To: Tiebar shown (if present) is a non-functional feature and may be located on any of the 4 sides (or ends).
March 26, 2014	FN6391.2	Added "Evaluation Board Ordering Information" on page 5. Updated θ_{JA} and θ_{JC} in "Thermal Information" on page 6 from 50/10 to 52.8/11 Added standard "Boldface limits apply" verbiage to common conditions of "Electrical Specifications" table. Bolded applicable specs. Changed Note 8 in spec table from "Parts are 100% tested at +25°C. Temperature limits established by characterization and are not production tested." to "Parameters with MIN and/or MAX limits are 100% tested at +25°C, unless otherwise specified. Temperature limits established by characterization and are not production tested." Updated Products section on page 13 to new About Intersil verbiage. Updated "Package Outline Drawing" on page 14. Changes: Updated format to new standard Removed package outline and included center to center distance between lands on recommended land pattern. Removed Note 4 "Dimension b applies to the metallized terminal and is measured between 0.18mm and 0.30mm from the terminal tip." - it is not applicable to this package. Renumbered notes accordingly.
March 11, 2008	FN6391.1	Added "VO1, VO2 Pins" to "Absolute Maximum Ratings" on page 6. Added "Other output voltage options may be available upon request" to page 1.
January 7, 2010	FN6391.0	Initial release.

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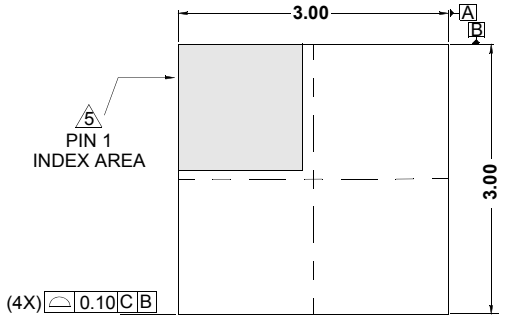
Package Outline Drawing

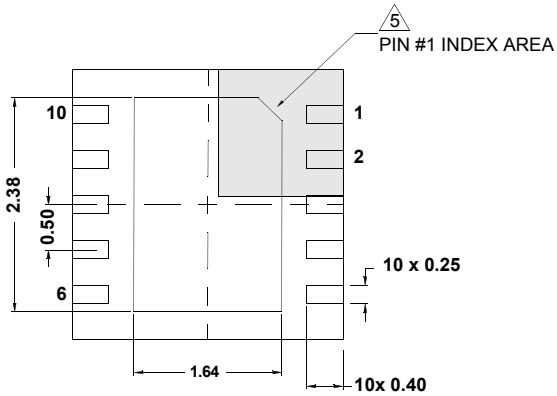
L10.3x3C

10 LEAD DUAL FLAT PACKAGE (DFN)

Rev 4, 3/15



TOP VIEW



BOTTOM VIEW

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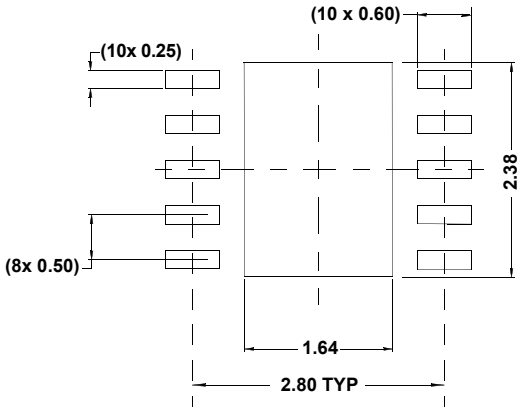
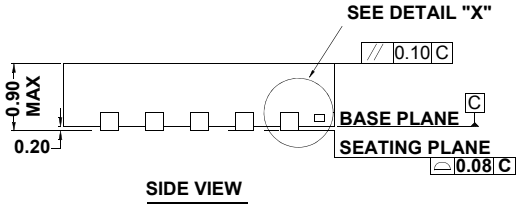
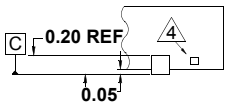


TYPICAL RECOMMENDED LAND PATTERN



SIDE VIEW



DETAIL "X"

NOTES:

1. Dimensions are in millimeters.
   Dimensions in ( ) for Reference Only.
2. Dimensioning and tolerancing conform to AMSE Y14.5m-1994.
3. Unless otherwise specified, tolerance : Decimal ± 0.05
4. Tiebar shown (if present) is a non-functional feature and may be located on any of the 4 sides (or ends).
5. The configuration of the pin #1 identifier is optional, but must be located within the zone indicated. The pin #1 identifier may be either a mold or mark feature.
6. Compliant to JEDEC MO-229-WEED-3 except for E-PAD dimensions.

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