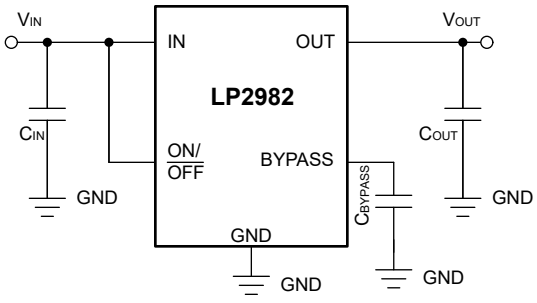
LP2982 50mA, Low-Noise, Low-Dropout Regulator in SOT-23 Package

1 Features

- V_{IN} range (new chip): 2.5V to 16V
- V_{OUT} range (new chip): 1.2V to 5.0V
- V_{OUT} accuracy:
  - ±1% for A-grade (legacy chip)
  - ±1.5% for standard-grade (legacy chip)
  - ±0.5% (new chip)
- ±1% output accuracy over load and temperature (new chip)
- Output current: Up to 50mA
- Low I_Q (new chip): 69µA at I_{LOAD} = 0mA
- Low I_Q (new chip): 380µA at I_{LOAD} = 50mA
- Shutdown current:
  - 1µA for legacy chip
  - 2.25µA for new chip
- Low noise: 30µV_{RMS} with 10nF bypass capacitor
- Output current limiting and thermal protection
- Stable with 2.2µF ceramic capacitors (new chip)
- High PSRR: 70dB at 1kHz, 40dB at 1MHz
- Operating junction temperature: –40°C to +125°C
- Package: 5-pin SOT-23 (DBV)

2 Applications

- Factory automation and control
- Industrial transport (non-car, non-light truck)
- Grid infrastructure
- Medical



Simplified Schematic

3 Description

The LP2982 is a fixed-output, wide-input, low-noise, low-dropout voltage regulator supporting an input voltage range from 2.5V to 16V (for new chip) and up to 50mA of load current. The LP2982 supports an output range of 1.2V to 5.0V (new chip).

Additionally, the LP2982 (new chip) has a ±1% output accuracy across load, and temperature that can meet the needs of low-voltage microcontrollers (MCUs) and processors.

Low output noise of 30µV_{RMS} (with 10nF bypass capacitors) and wide bandwidth PSRR performance of greater than 70dB at 1kHz and 40dB at 1MHz help attenuate the switching frequency of an upstream DC/DC converter and minimize post regulator filtering.

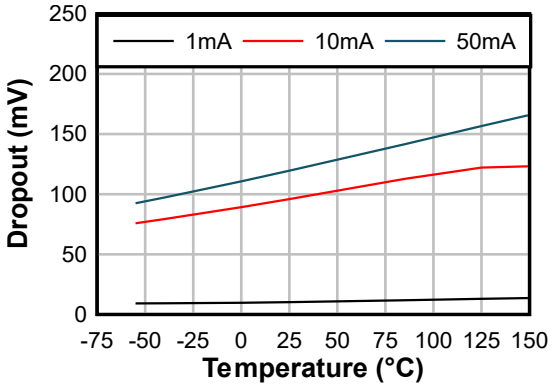
The new chip version of the LP2982 includes an internal soft-start mechanism to reduce inrush current during start up, thus minimizing input capacitance requirement. Standard protection features, such as overcurrent and overtemperature protection, are included.

The LP2982 is available in a 5-pin 2.9mm × 2.8mm SOT-23 (DBV) package.

Package Information

PART NUMBER	PACKAGE(1)	PACKAGE SIZE(2)
LP2982	DBV (SOT-23, 5)	2.9mm × 2.8mm

(1) For more information, see the *Mechanical, Packaging, and Orderable Information*.
(2) The package size (length × width) is a nominal value and includes pins, where applicable.



Dropout Voltage vs Temperature (New Chip)

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4 Pin Configuration and Functions

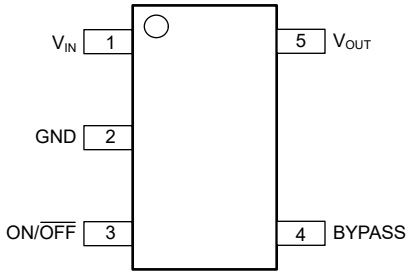

Figure 4-1. DBV Package, 5-Pin SOT-23 (Top View)

Table 4-1. Pin Functions

PIN		TYPE	DESCRIPTION
NAME	NO.		
BYPASS	4	I/O	BYPASS pin to achieve low noise performance. Connecting an external capacitor between BYPASS pin and ground reduces reference voltage noise. See the *Recommended Operating Conditions* section for more information.
GND	2	—	Ground
ON/$\overline{\text{OFF}}$	3	I	Enable pin for the LDO. Driving the ON/$\overline{\text{OFF}}$ pin high enables the device. Driving this pin low disables the device. High and low thresholds are listed in the *Electrical Characteristics* table. Tie this pin to V_{IN} if unused.
V_{IN}	1	I	Input supply pin. Use a capacitor with a value of 1 µF or larger from this pin to ground. See the *Input Capacitor Requirements* section for more information.
V_{OUT}	5	O	Output of the regulator. Use a capacitor with a value of 2.2 µF or larger from this pin to ground. See the *Input Capacitor Requirements* section for more information.(1)

(1) The nominal output capacitor for the new chip must be greater than 2.2 µF. Throughout this document, the nominal derating on these capacitors is 50%. Make sure that the effective capacitance at the pin is greater than 1 µF.

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5 Specifications

5.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1) (2)

		MIN	MAX	UNIT
V_{IN}	Continuous input voltage range (for legacy chip)	–0.3	16	V
	Continuous input voltage range (for new chip)	–0.3	18	
V_{OUT}	Output voltage range (for legacy chip)	–0.3	9	
	Output voltage range (for new chip)	–0.3	V_{IN} + 0.3 or 9 (whichever is smaller)	
$V_{ON/\overline{OFF}}$	ON/$\overline{OFF}$ pin voltage range (for legacy chip)	–0.3	16	
	ON/$\overline{OFF}$ pin voltage range (for new chip)	–0.3	18	
$V_{IN} – V_{OUT}$	Input-output voltage (for legacy chip)	–0.3	16	
	Input-output voltage (for new chip)	–0.3	18	
Current	Maximum output current	Internally limited		mA
Temperature	Operating junction, T_J	–55	150	°C
	Storage, T_{stg}	–65	150	

(1) Operation outside the *Absolute Maximum Ratings* may cause permanent device damage. *Absolute Maximum Ratings* do not imply functional operation of the device at these or any other conditions beyond those listed under *Recommended Operating Conditions*. If used outside the *Recommended Operating Conditions* but within the *Absolute Maximum Ratings,* the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.
(2) All voltages with respect to GND.

5.2 ESD Ratings

			VALUE (Legacy Chip)	VALUE (New Chip)	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001 (Pin 1,2 and 5) (1)	±2000	±3000	V
		Human body model (HBM), per ANSI/ESDA/JEDEC JS-001 (Pin 3 and 4) (1)	±1000		
		Charged device model (CDM), per JEDEC specification JESD22-C101(2)	N/A	±1000	

(1) JEDEC document JEP155 states that 2-kV HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 500-V CDM allows safe manufacturing with a standard ESD control process.

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5.3 Recommended Operating Conditions

		MIN	NOM	MAX	UNIT
V_{IN}	Supply input voltage (for legacy chip)	2.1		16	V
	Supply input voltage (for new chip)	2.5		16	
$V_{IN} – V_{OUT}$	Input-output differential (for legacy chip)	0.7		11	
	Input-output differential (for new chip)	0		16	
V_{OUT}	Output voltage (for new chip)	1.2		5	
$V_{ON/\overline{OFF}}$	Enable voltage (for legacy chip)	0		V_{IN}	
	Enable voltage (for new chip)	0		16	
I_{OUT}	Output current	0		50	mA
C_{IN} (1)	Input capacitor		1		µF
C_{OUT}	Output capacitor (for legacy chip)	2.2	4.7		
	Output capacitance (for new chip) (1)	1	2.2	200	
C_{OUT} ESR (2)	Output capacitor ESR (for new chip) (3)	0		1	Ω
T_J	Operating junction temperature	–40		125	°C

(1) All capacitor values are assumed to derate to 50% of the nominal capacitor value. Maintain an effective output capacitance of 1 µF minimum for stability.
(2) Maximum supported ESR range for new chip is 1Ω. For output capacitor with higher ESR values, place a low ESR MLCC capacitor.
(3) Details related to supported ESR range for the legacy chip are available in *Recommended Capacitors (Legacy Chip)*.

5.4 Thermal Information

THERMAL METRIC (1)		Legacy Chip (2) DBV (SOT23-5) 5 PINS	New Chip (2) DBV (SOT23-5) 5 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	175.7	178.6	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	121.8	77.9	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	29.5	47.2	°C/W
ψ_{JT}	Junction-to-top characterization parameter	16.1	15.9	°C/W
ψ_{JB}	Junction-to-board characterization parameter	29.0	46.9	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application note.
(2) Thermal performance results are based on the JEDEC standard of 2s2p PCB configuration. These thermal metric parameters can be further improved by 35-55% based on thermally optimized PCB layout designs. See the analysis of the *Impact of board layout on LDO thermal performance* application report.

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5.5 Electrical Characteristics

specified at T_J = 25 °C, V_{IN} = $V_{OUT(nom)}$ + 1.0 V or VIN = 2.5 V (whichever is greater), I_{OUT} = 1 mA, $V_{ON/OFF}$ = 2 V, C_{IN} = 1.0 µF, and C_{OUT} = 2.2 µF (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
ΔV_{OUT}	Output voltage tolerance	I_L = 1 mA	Legacy chip (standard grade)	–1.5		1.5	%
			Legacy chip (A grade)	–1.0		1.0	
			New chip	–0.5		0.5	
		1 mA < I_L < 50 mA	Legacy chip (standard grade)	–2		2	
			Legacy chip (A grade)	–1.5		1.5	
			New chip	–0.5		0.5	
		1 mA < I_L < 50 mA, –40°C ≤ T_J ≤ 125°C	Legacy chip (standard grade)	–3.5		3.5	
			Legacy chip (A grade)	–2		2	
			New chip	–1		1	
$\Delta V_{OUT(\Delta VIN)}$	Line regulation	$V_{O(NOM)}$ + 1 V < V_{IN} < 16 V	Legacy chip		0.007	0.014	%/V
			New chip		0.002	0.014	
		$V_{O(NOM)}$ + 1 V < V_{IN} < 16 V, –40°C ≤ T_J ≤ 125°C	Legacy chip		0.007	0.032	
			New chip		0.002	0.032	
$\Delta V_{OUT(\Delta ILOAD)}$	Load regulation	1 mA < I_L < 50 mA, –40°C ≤ T_J ≤ 125°C, V_{IN} = $V_{O(NOM)}$ +0.5 V	New chip		0.1	0.5	%/A
V_{DO}	Dropout voltage	I_{OUT} = 0 mA	Legacy chip		1	3	mV
			New chip		1	2.75	
		I_{OUT} = 0 mA, –40°C ≤ T_J ≤ 125°C	Legacy chip			5	
			New chip			3	
		I_{OUT} = 1 mA	Legacy chip		7	10	
			New chip		11.5	14	
		I_{OUT} = 1 mA, –40°C ≤ T_J ≤ 125°C	Legacy chip			15	
			New chip			17	
		I_{OUT} = 10 mA	Legacy chip		40	60	
			New chip		98	115	
		I_{OUT} = 10 mA, –40°C ≤ T_J ≤ 125°C	Legacy chip			90	
			New chip			148	
		I_{OUT} = 50 mA	Legacy chip		120	150	
			New chip		120	145	
		I_{OUT} = 50 mA, –40°C ≤ T_J ≤ 125°C	Legacy chip			225	
			New chip			184	
		I_{OUT} = 80 mA	Legacy chip		180	225	
			New chip		150	165	
		I_{OUT} = 80 mA, –40°C ≤ T_J ≤ 125°C	Legacy chip			325	
			New chip			204	

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5.5 Electrical Characteristics (continued)

specified at T_J = 25 °C, V_{IN} = $V_{OUT(nom)}$ + 1.0 V or VIN = 2.5 V (whichever is greater), I_{OUT} = 1 mA, $V_{ON/OFF}$ = 2 V, C_{IN} = 1.0 µF, and C_{OUT} = 2.2 µF (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
I_{GND}	GND pin current	I_{OUT} = 0 mA	Legacy chip		65	95	µA
			New chip		69	95	
		I_{OUT} = 0 mA, –40°C ≤ T_J ≤ 125°C	Legacy chip			125	
			New chip			123	
		I_{OUT} = 1 mA	Legacy chip		80	110	
			New chip		78	110	
		I_{OUT} = 1 mA, –40°C ≤ T_J ≤ 125°C	Legacy chip			170	
			New chip			140	
		I_{OUT} = 10 mA	Legacy chip		140	220	µA
			New chip		175	210	
		I_{OUT} = 10 mA, –40°C ≤ T_J ≤ 125°C	Legacy chip			460	
			New chip			250	
		I_{OUT} = 50 mA	Legacy chip		375	600	µA
			New chip		380	440	
		I_{OUT} = 50 mA, –40°C ≤ T_J ≤ 125°C	Legacy chip			1200	µA
			New chip			650	µA
		I_{OUT} = 80 mA	Legacy chip		525	750	µA
			New chip		575	720	µA
		I_{OUT} = 80 mA, –40°C ≤ T_J ≤ 125°C	Legacy chip			1400	µA
						900	µA
		$V_{ON/OFF}$ < 0.3 V, V_{IN} = 16 V	Legacy chip		0.01	0.8	µA
			New chip		1.25	1.75	µA
		$V_{ON/OFF}$ < 0.15 V, V_{IN} = 16 V, –40°C ≤ T_J ≤ 125°C	Legacy chip		0.1	2	µA
			New chip		1.12	2.75	µA
V_{UVLO+}	Rising bias supply UVLO	V_{IN} rising, –40°C ≤ T_J ≤ 125°C	New chip		2.2	2.4	V
V_{UVLO-}	Falling bias supply UVLO	V_{IN} falling, –40°C ≤ T_J ≤ 125°C		1.9			V
$V_{UVLO(HYST)}$	UVLO hysteresis	–40°C ≤ T_J ≤ 125°C			0.130		V
$I_{O(MAX)}$	Short Output Current	R_L = 0 Ω (steady state)	Legacy chip		150		mA
			New chip		150		mA
$I_{O(PK)}$	Peak Output Current	V_{OUT} ≥ $V_{O(NOM)}$ –5% (steady state)	Legacy chip	100	150		mA
			New chip	100	150		mA
$V_{ON/\overline{OFF}}$	ON/$\overline{OFF}$ input voltage	Low = Output OFF	Legacy chip		0.55		V
			New chip		0.72		
		Low = Output OFF, V_{OUT} + 1 < V_{IN} < 16 V, –40°C ≤ T_J ≤ 125°C	Legacy chip			0.15	
			New chip			0.15	
		High = Output ON	Legacy chip		1.4		
			New chip		0.85		
		High = Output ON, V_{OUT} + 1 < V_{IN} < 16 V, –40°C ≤ T_J ≤ 125°C	Legacy chip	1.6			
			New chip	1.6			

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5.5 Electrical Characteristics (continued)

specified at T_J = 25 °C, V_{IN} = $V_{OUT(nom)}$ + 1.0 V or VIN = 2.5 V (whichever is greater), I_{OUT} = 1 mA, $V_{ON/OFF}$ = 2 V, C_{IN} = 1.0 µF, and C_{OUT} = 2.2 µF (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
$I_{ON/\overline{OFF}}$	ON/OFF input current	$V_{ON/OFF}$ = 0 V	Legacy chip		0.01		µA
			New chip		0.42		
		$V_{ON/OFF}$ = 0 V, V_{OUT} + 1 < V_{IN} < 16 V, –40°C ≤ T_J ≤ 125°C	Legacy chip			–2	µA
			New chip			–0.9	µA
		$V_{ON/OFF}$ = 5 V	Legacy chip		5		µA
			New chip		0.011		µA
		$V_{ON/OFF}$ = 5 V, V_{OUT} + 1 < V_{IN} < 16 V, –40°C ≤ T_J ≤ 125°C	Legacy chip			15	µA
			New chip			2.20	µA
$\Delta V_O/\Delta V_{IN}$	Ripple rejection	f = 1 kHz, C_{BYPASS} = 10 nF, C_{OUT} = 10 µF	Legacy chip		45		dB
			New chip		78		
		f = 100 kHz, C_{BYPASS} = 10 nF , I_{LOAD} = 50 mA			45		dB
V_n	Output noise voltage	Bandwidth = 300 Hz to 50 kHz, $C_{NR/SS}$ = 10 nF, C_{OUT} = 2.2 µF, V_{OUT} = 1.8 V, I_{LOAD} = 150 mA	Legacy chip		30		μ_{VRMS}
			New chip		30		
		Bandwidth = 10 Hz to 100 kHz, $C_{NR/SS}$ = 10 nF, C_{OUT} = 2.2 µF, V_{OUT} = 3.3 V, I_{LOAD} = 150 mA			50		
T_{sd+}	Thermal shutdown threshold	Shutdown, temperature increasing	New chip		170		°C
T_{sd-}		Reset, temperature decreasing			150		

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5.6 Typical Characteristics

unless otherwise specified: T_A = 25°C, V_{IN} = $V_{O(NOM)}$ + 1 V, C_{OUT} = 4.7 µF, C_{IN} = 1 µF, all voltage options, ON/ $\overline{OFF}$ pin tied to V_{IN}.

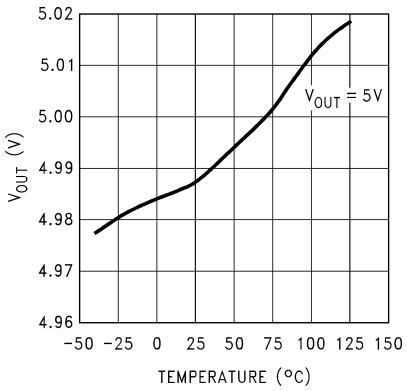


Figure 5-1. Output Voltage vs Temperature (Legacy Chip)

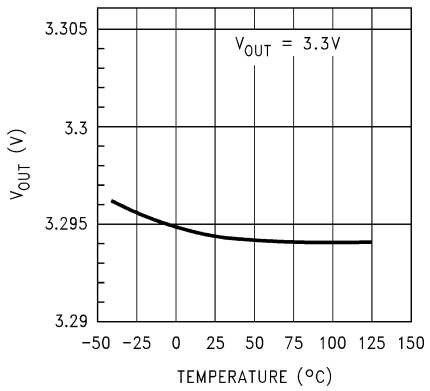


Figure 5-2. Output Voltage vs Temperature (Legacy Chip)

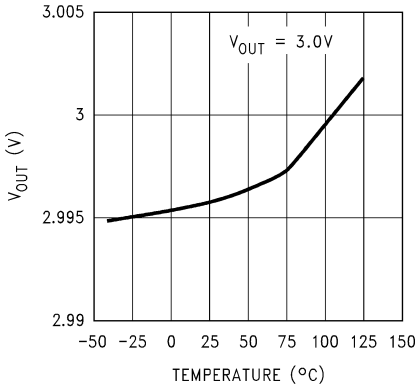
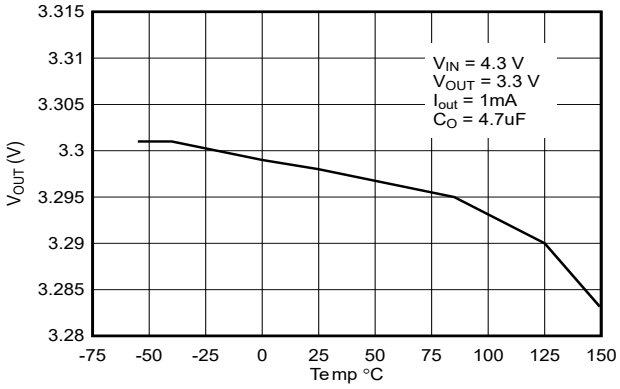
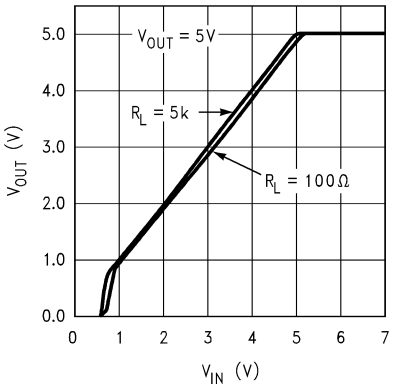


Figure 5-3. Output Voltage vs Temperature (Legacy Chip)



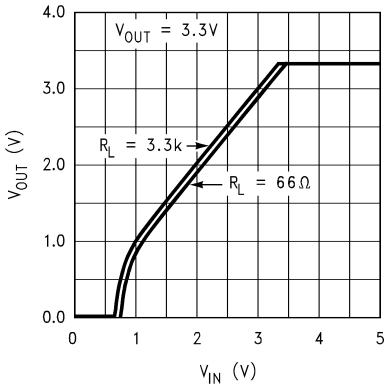
V_{IN} = 4.3 V, V_{OUT} = 3.3 V

Figure 5-4. Output Voltage vs Temperature (New Chip)



V_{OUT} = 5.0 V

Figure 5-5. Output Voltage vs V_{IN} (Legacy Chip)



V_{OUT} = 3.3 V

Figure 5-6. Output Voltage vs V_{IN} (Legacy Chip)

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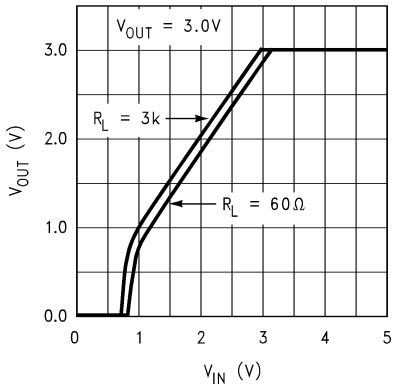
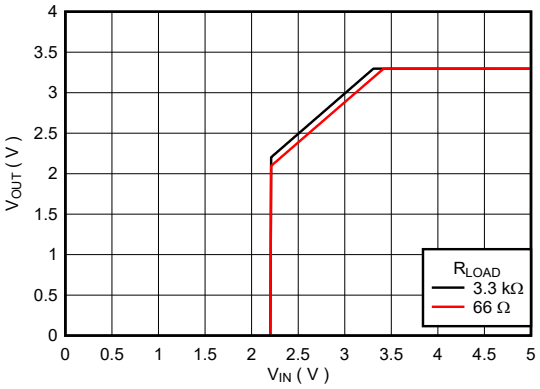
5.6 Typical Characteristics (continued)

unless otherwise specified: T_A = 25°C, V_{IN} = $V_{O(NOM)}$ + 1 V, C_{OUT} = 4.7 µF, C_{IN} = 1 µF, all voltage options, ON/ $\overline{OFF}$ pin tied to V_{IN}.



V_{OUT} = 3.0 V

Figure 5-7. Output Voltage vs V_{IN} (Legacy Chip)



V_{OUT} = 3.3 V

Figure 5-8. Output Voltage vs V_{IN} (New Chip)

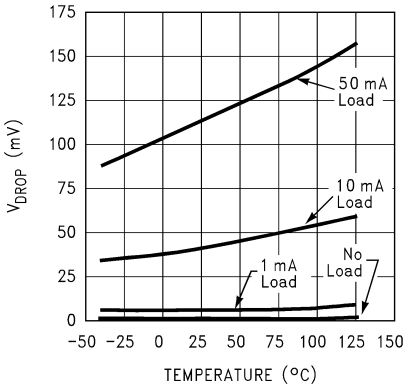


Figure 5-9. Dropout Voltage vs Temperature (Legacy Chip)

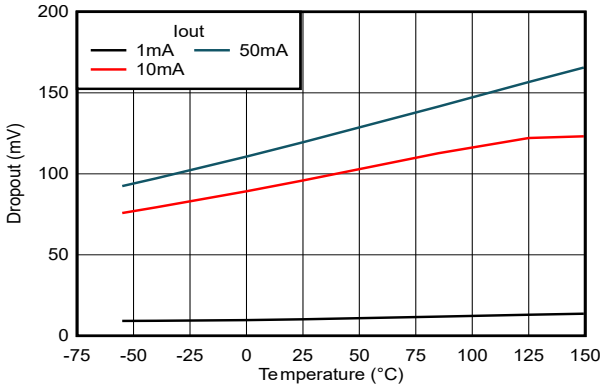


Figure 5-10. Dropout Voltage vs Temperature (New Chip)

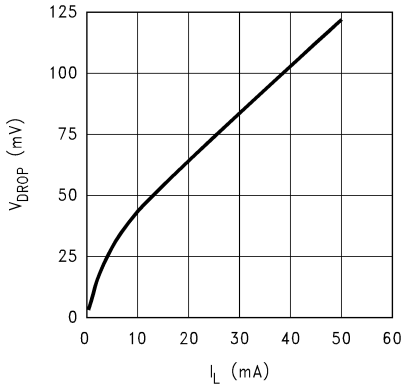


Figure 5-11. Dropout Voltage vs Load Current (Legacy Chip)

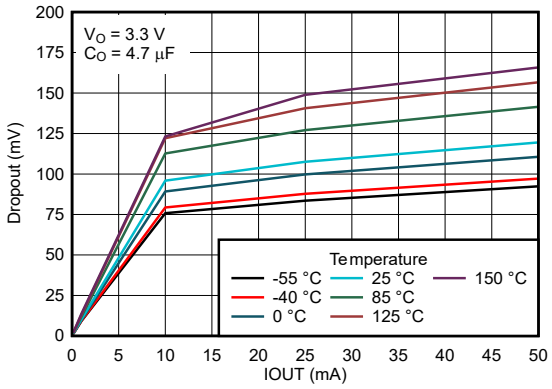


Figure 5-12. Dropout Voltage vs Load Current (New Chip)

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5.6 Typical Characteristics (continued)

unless otherwise specified: T_A = 25°C, V_{IN} = $V_{O(NOM)}$ + 1 V, C_{OUT} = 4.7 µF, C_{IN} = 1 µF, all voltage options, ON/ $\overline{OFF}$ pin tied to V_{IN}.

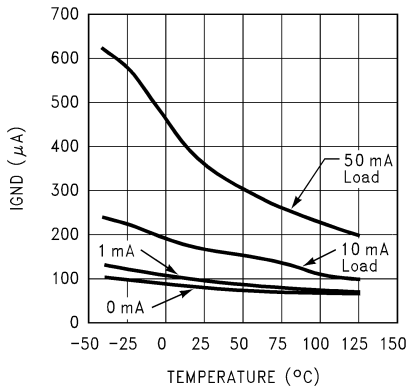


Figure 5-13. Ground Pin Current vs Temperature (Legacy Chip)

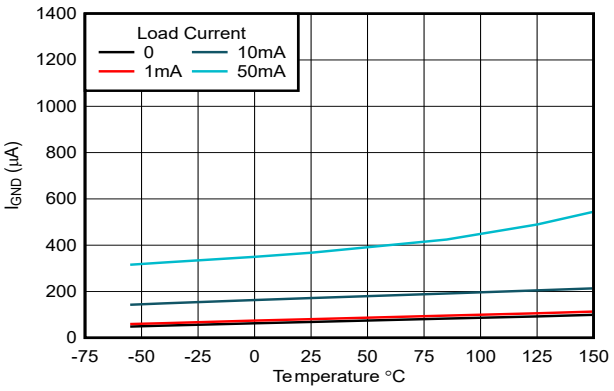


Figure 5-14. Ground Pin Current vs Temperature (New Chip)

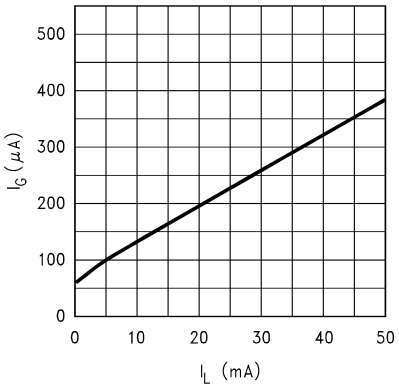


Figure 5-15. Ground Pin Current vs Load Current (Legacy Chip)

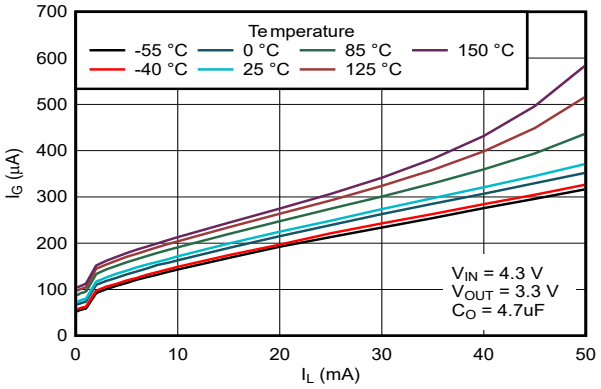


Figure 5-16. Ground Pin Current vs Load Current (New Chip)

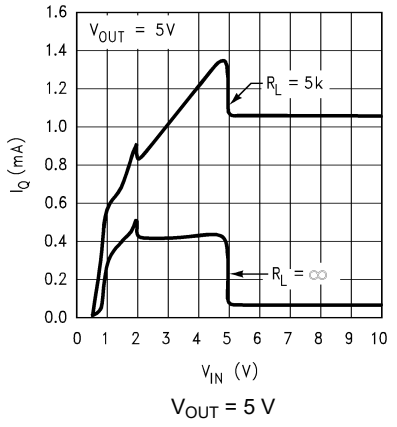


Figure 5-17. Input Current vs V_{IN} (Legacy Chip)

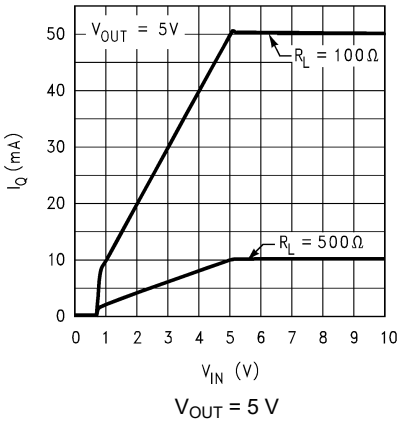


Figure 5-18. Input Current vs V_{IN} (Legacy Chip)

5.6 Typical Characteristics (continued)

unless otherwise specified: T_A = 25°C, V_{IN} = $V_{O(NOM)}$ + 1 V, C_{OUT} = 4.7 µF, C_{IN} = 1 µF, all voltage options, ON/ $\overline{OFF}$ pin tied to V_{IN}.

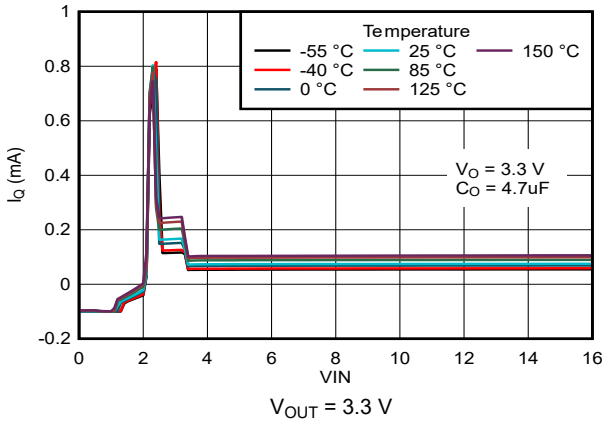


Figure 5-19. Input Current vs Input Voltage (New Chip)

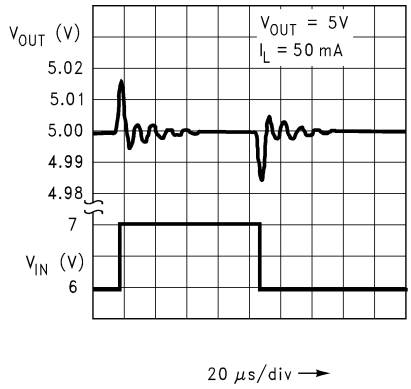


Figure 5-20. Line Transient Response (Legacy Chip)

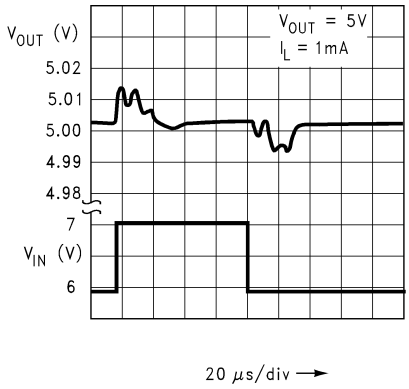
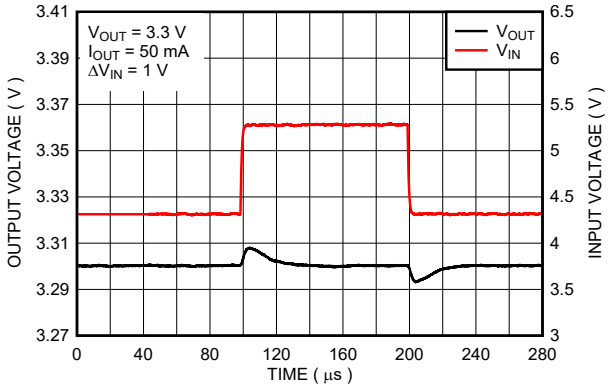


Figure 5-21. Line Transient Response (Legacy Chip)



V_{OUT} = 3.3 V, ΔV_{IN} = 1 V, I_{OUT} = 50 mA, dV/dt = 1 V/µs

Figure 5-22. Line Transient Response (New Chip)

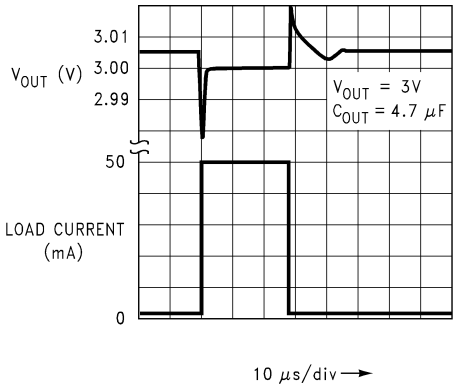


Figure 5-23. Load Transient Response (Legacy Chip)

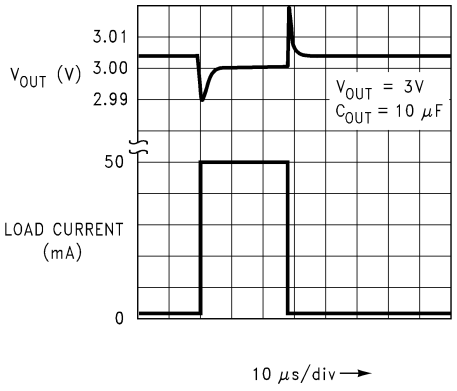


Figure 5-24. Load Transient Response (Legacy Chip)

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5.6 Typical Characteristics (continued)

unless otherwise specified: T_A = 25°C, V_{IN} = $V_{O(NOM)}$ + 1 V, C_{OUT} = 4.7 µF, C_{IN} = 1 µF, all voltage options, ON/ $\overline{OFF}$ pin tied to V_{IN}.

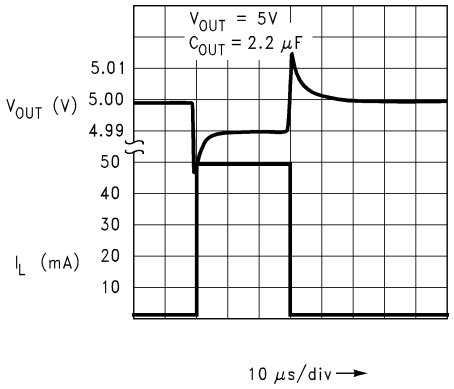

Figure 5-25. Load Transient Response (Legacy Chip)

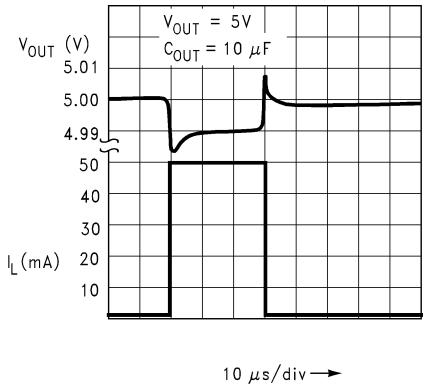

Figure 5-26. Load Transient Response (Legacy Chip)

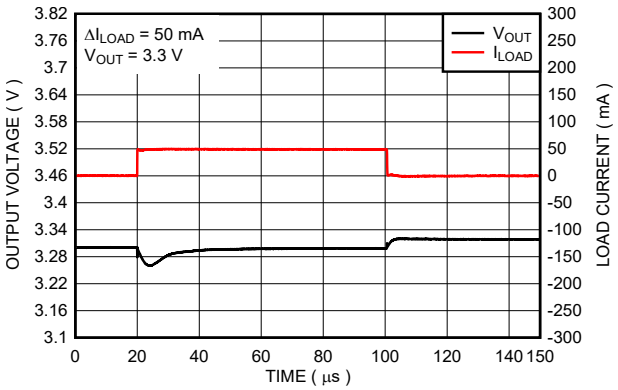

Figure 5-27. Load Transient Response (New Chip)

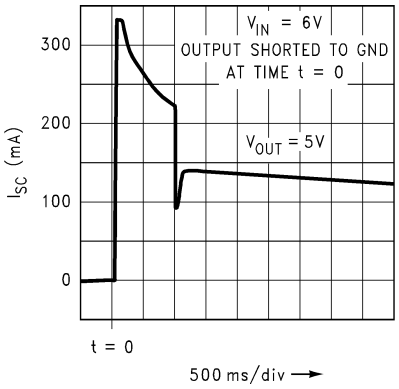

Figure 5-28. Short-Circuit Current vs Time (Legacy Chip)

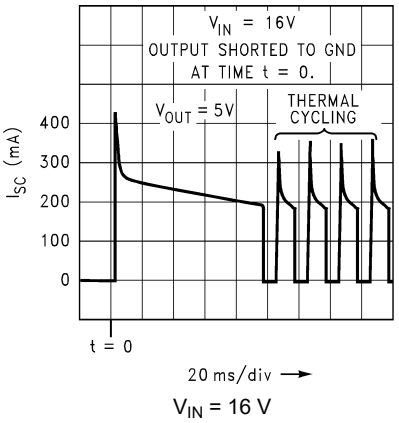

Figure 5-29. Short-Circuit Current vs Time (Legacy Chip)

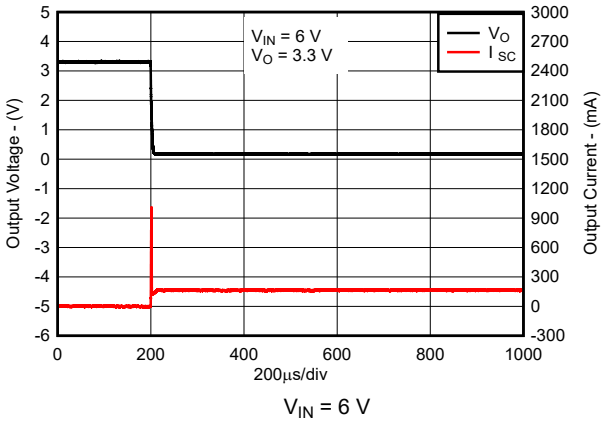

Figure 5-30. Short-Circuit Current vs Time (New Chip)

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5.6 Typical Characteristics (continued)

unless otherwise specified: T_A = 25°C, V_{IN} = $V_{O(NOM)}$ + 1 V, C_{OUT} = 4.7 µF, C_{IN} = 1 µF, all voltage options, ON/ $\overline{OFF}$ pin tied to V_{IN}.

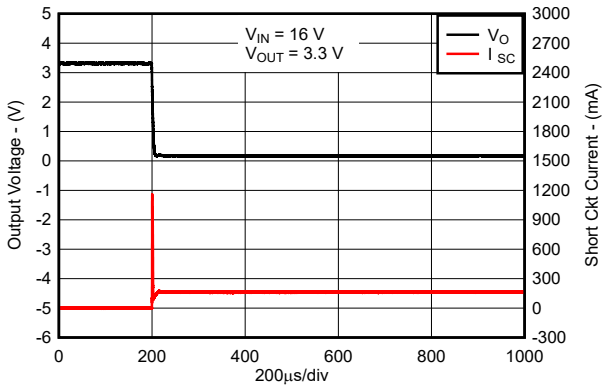

Figure 5-31. Short-Circuit Current vs Time (New Chip)

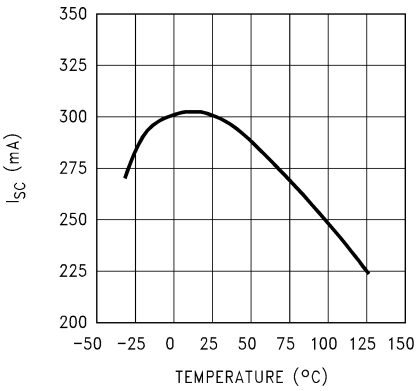

Figure 5-32. Instantaneous Short-Circuit Current vs Temperature (Legacy Chip)

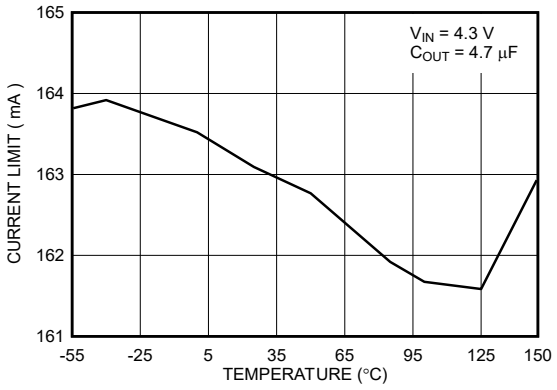

Figure 5-33. Short-Circuit Current vs Temperature (New Chip)

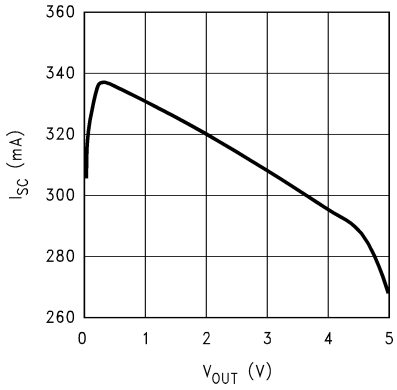

Figure 5-34. Instantaneous Short Circuit Current vs Output Voltage (Legacy Chip)

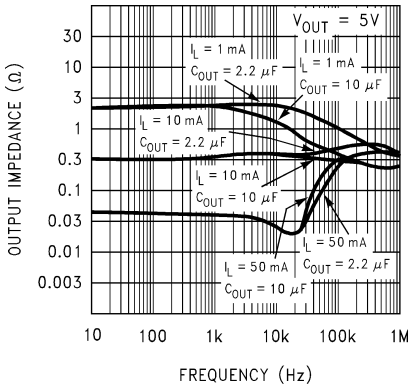

Figure 5-35. Output Impedance vs Frequency (Legacy Chip)

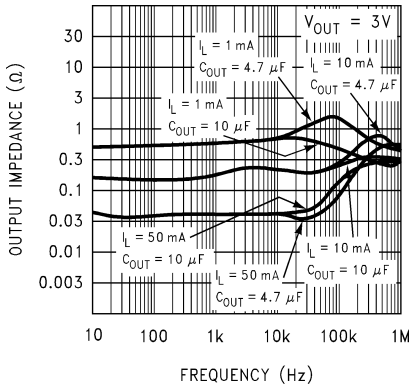

Figure 5-36. Output Impedance vs Frequency (Legacy Chip)

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5.6 Typical Characteristics (continued)

unless otherwise specified: T_A = 25°C, V_{IN} = $V_{O(NOM)}$ + 1 V, C_{OUT} = 4.7 µF, C_{IN} = 1 µF, all voltage options, ON/ $\overline{OFF}$ pin tied to V_{IN}.

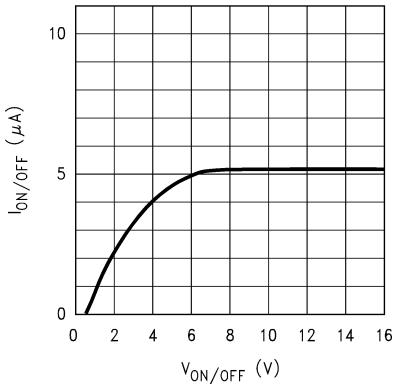

Figure 5-37. ON/$\overline{OFF}$ Pin Current vs $V_{ON/OFF}$ (Legacy Chip)

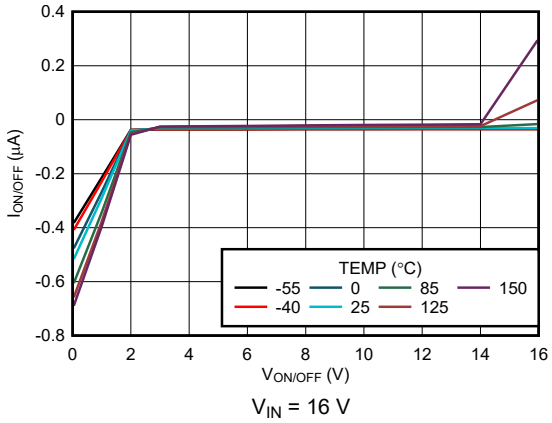

Figure 5-38. ON/$\overline{OFF}$ Pin Current vs $V_{ON/\overline{OFF}}$ (New Chip)

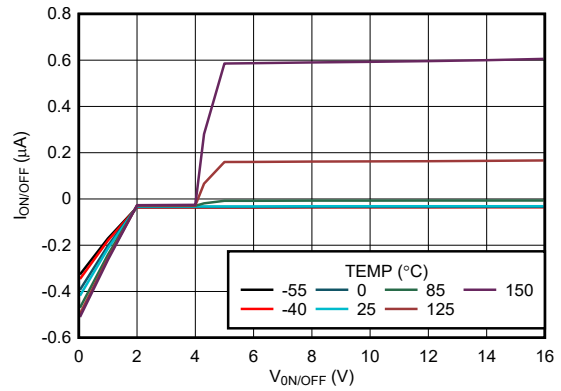

Figure 5-39. ON/$\overline{OFF}$ Pin Current vs $V_{ON/\overline{OFF}}$ (New Chip)

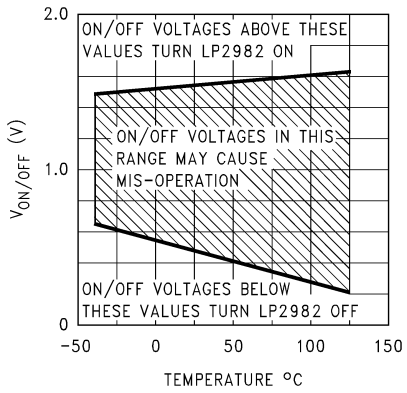

Figure 5-40. ON/$\overline{OFF}$ Threshold vs Temperature (Legacy Chip)

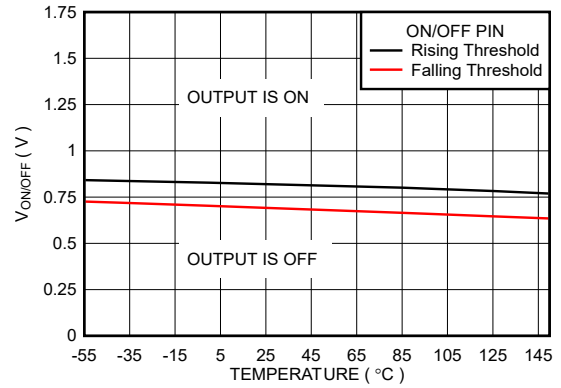

Figure 5-41. ON/$\overline{OFF}$ Threshold vs Temperature (New Chip)

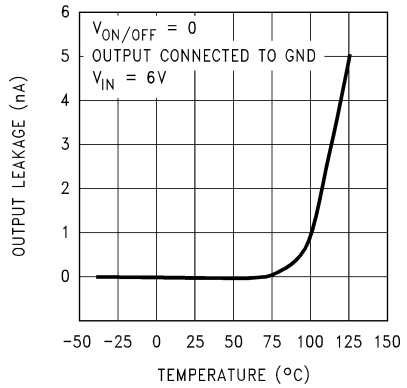

Figure 5-42. Input-to-Output Leakage vs Temperature (Legacy Chip)

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5.6 Typical Characteristics (continued)

unless otherwise specified: T_A = 25°C, V_{IN} = $V_{O(NOM)}$ + 1 V, C_{OUT} = 4.7 µF, C_{IN} = 1 µF, all voltage options, ON/ $\overline{OFF}$ pin tied to V_{IN}.

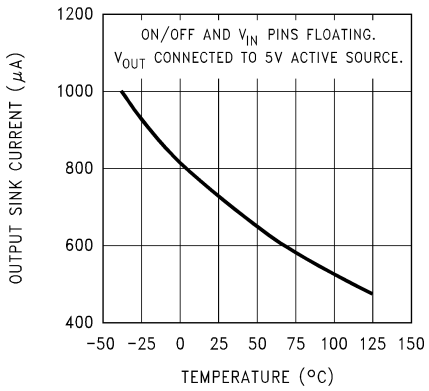


Figure 5-43. Output Reverse Leakage vs Temperature (Legacy Chip)

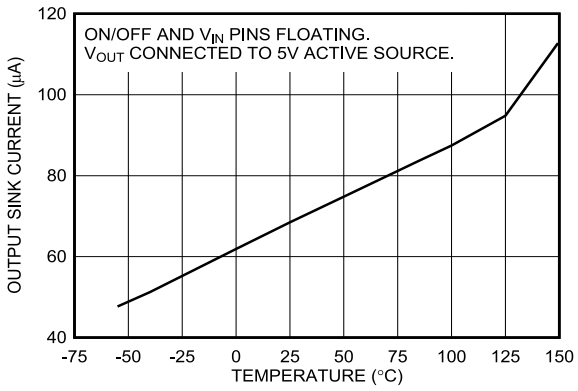


Figure 5-44. Output Reverse Leakage vs Temperature (New Chip)

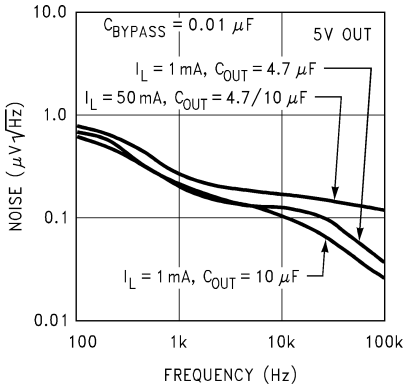


Figure 5-45. Output Noise Density (Legacy Chip)

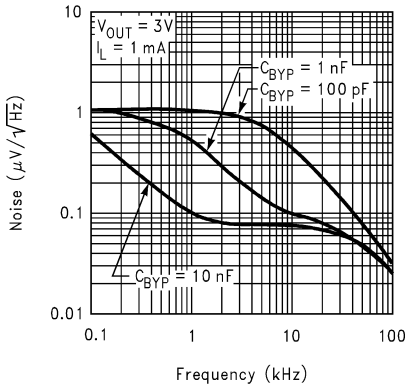


Figure 5-46. Output Noise Density (Legacy Chip)

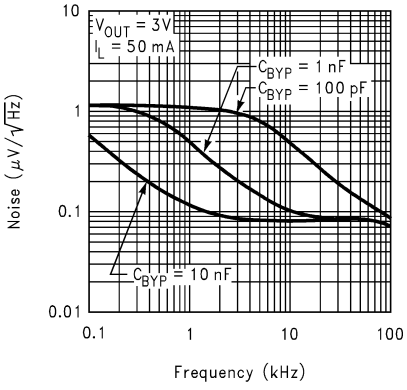
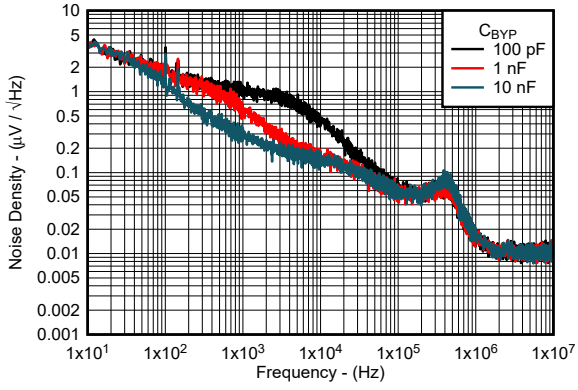


Figure 5-47. Output Noise Density (Legacy Chip)



V_{IN} = 4.3V, V_{OUT} = 3.3V, C_{OUT} = 2.2µF and I_{LOAD} = 50 mA

Figure 5-48. Output Noise Density vs Frequency (New Chip)

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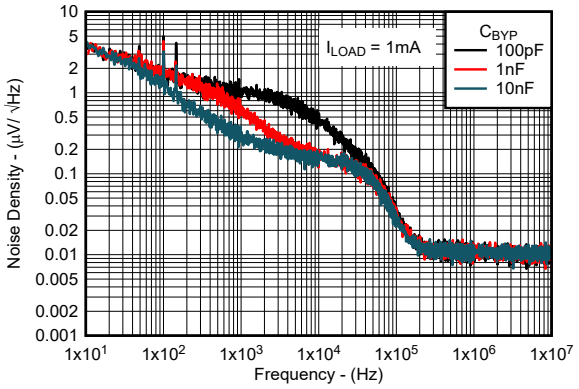
5.6 Typical Characteristics (continued)

unless otherwise specified: T_A = 25°C, V_{IN} = $V_{O(NOM)}$ + 1 V, C_{OUT} = 4.7 µF, C_{IN} = 1 µF, all voltage options, ON/ $\overline{OFF}$ pin tied to V_{IN}.



V_{IN} = 4.3V, V_{OUT} = 3.3V, C_{OUT} = 2.2µF and I_{LOAD} = 1 mA

Figure 5-49. Output Noise Density vs Frequency (New Chip)

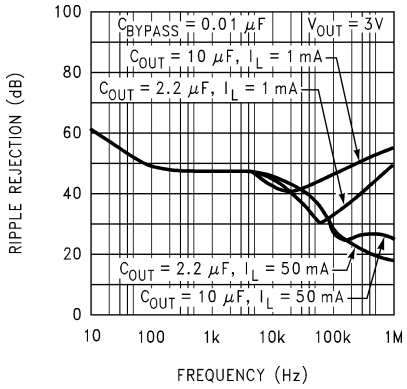
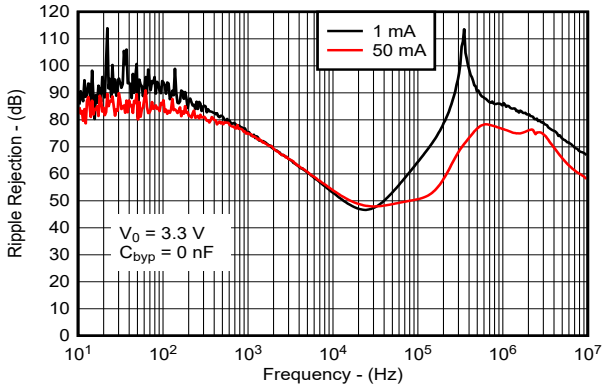
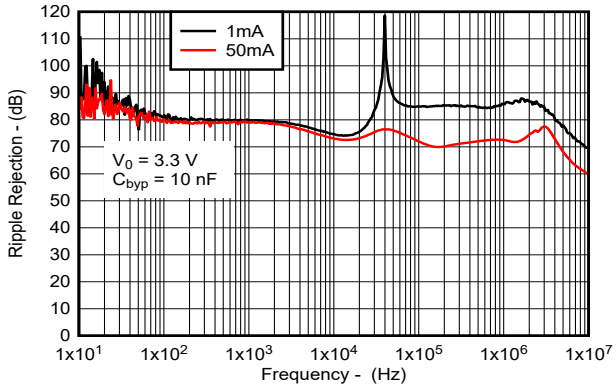


Figure 5-50. Ripple Rejection (Legacy Chip)



V_{OUT} = 3.3 V, C_{byp} = 0 nF

Figure 5-51. Ripple Rejection vs I_{OUT} (New Chip)



V_{OUT} = 3.3 V, C_{byp} = 10 nF

Figure 5-52. Ripple Rejection vs I_{OUT} (New Chip)

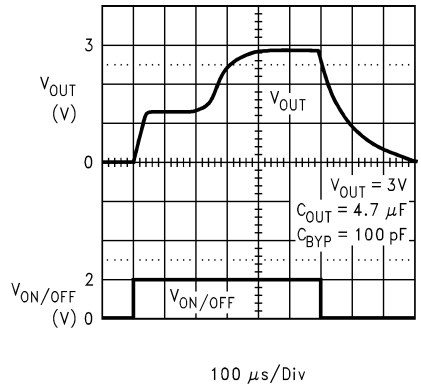


Figure 5-53. Turnon Waveform (Legacy Chip)

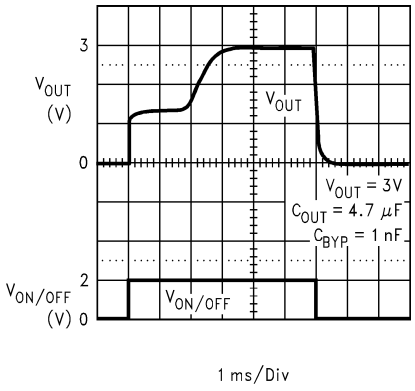


Figure 5-54. Turnon Waveform (Legacy Chip)

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5.6 Typical Characteristics (continued)

unless otherwise specified: T_A = 25°C, V_{IN} = $V_{O(NOM)}$ + 1 V, C_{OUT} = 4.7 µF, C_{IN} = 1 µF, all voltage options, ON/ $\overline{OFF}$ pin tied to V_{IN}.

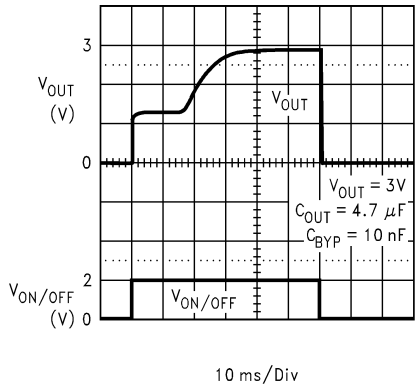

Figure 5-55. Turnon Waveform (Legacy Chip)

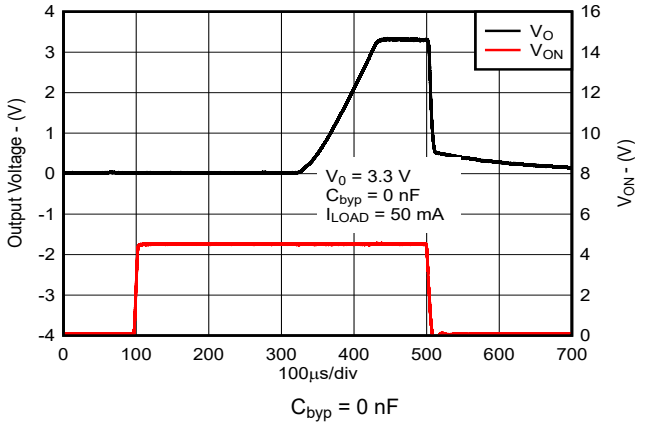

Figure 5-56. Turnon Waveform (New Chip)

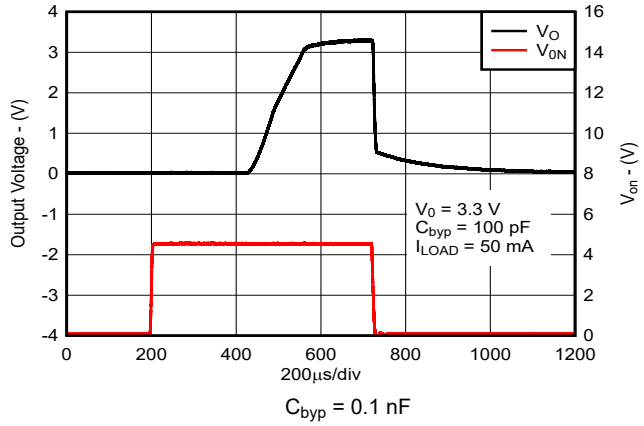

Figure 5-57. Turnon Waveform (New Chip)

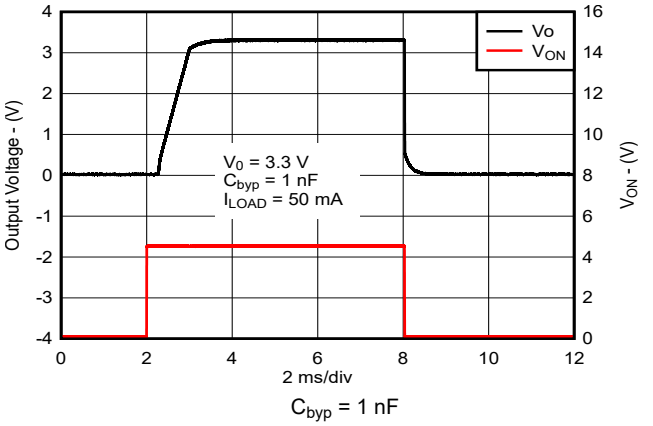

Figure 5-58. Turnon Waveform (New Chip)

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6 Detailed Description

6.1 Overview

The LP2982 is a fixed-output, low-noise, high PSRR, low-dropout regulator that offers exceptional, cost-effective performance for both portable and nonportable applications. The LP2982 has an output tolerance of ±1% across load, and temperature variation (new chip) and is capable of delivering 50 mA of continuous load current.

This device features integrated overcurrent protection, thermal shutdown and output enable. The new chip version of the LP2982 also features internal output pulldown and has a built-in soft-start mechanism for controlled inrush current. This device delivers excellent line and load transient performance. The operating ambient temperature range of the device is –40°C to +125°C.

6.2 Functional Block Diagrams

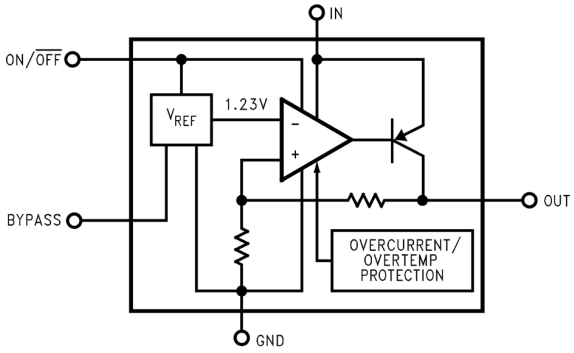

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Figure 6-1. Functional Block Diagram (Legacy Chip)

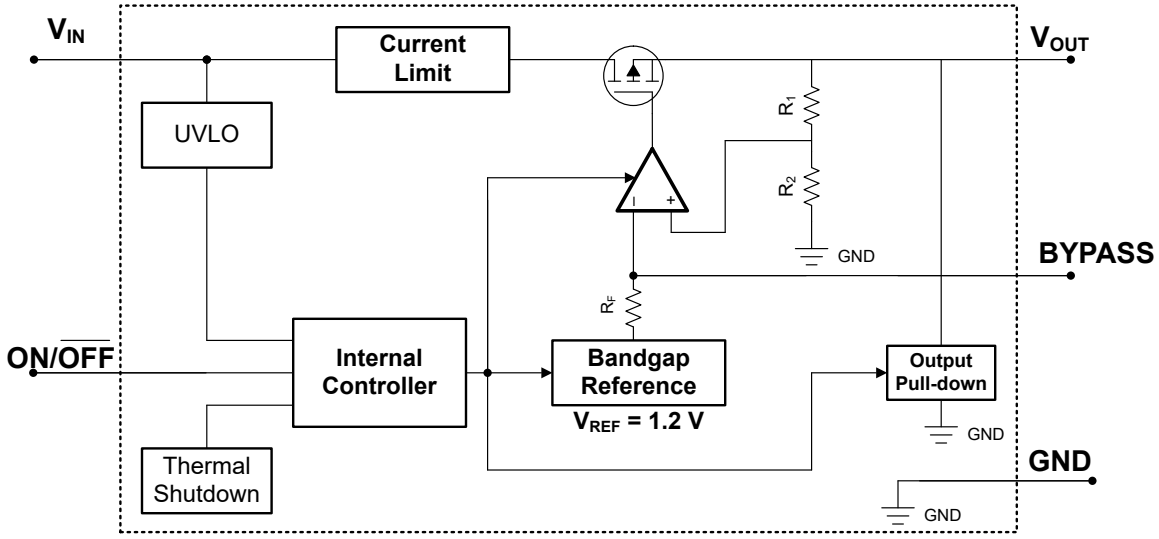

Figure 6-2. Functional Block Diagram (New Chip)

6.3 Feature Description

6.3.1 Output Enable

The ON/$\overline{\text{OFF}}$ pin for the device is an active-high pin. The output voltage is enabled when the voltage of the ON/$\overline{\text{OFF}}$ pin is greater than the high-level input voltage of the ON/$\overline{\text{OFF}}$ pin and disabled with the ON/$\overline{\text{OFF}}$ pin voltage is less than the low-level input voltage of the ON/$\overline{\text{OFF}}$ pin. If independent control of the output voltage is not needed, connect the ON/$\overline{\text{OFF}}$ pin to the input of the device.

The new chip version of the device has an internal pulldown circuit that activates when the device is disabled by pulling the ON/$\overline{OFF}$ pin voltage lower than the low-level input voltage of the ON/$\overline{OFF}$ pin, to actively discharge the output voltage.

6.3.2 Dropout Voltage

Dropout voltage (V_{DO}) is defined as the input voltage minus the output voltage ($V_{IN} – V_{OUT}$) at the rated output current (I_{RATED}), where the pass transistor is fully on. I_{RATED} is the maximum I_{OUT} listed in the *Recommended Operating Conditions* table. The pass transistor is in the ohmic or triode region of operation, and acts as a switch. The dropout voltage indirectly specifies a minimum input voltage greater than the nominal programmed output voltage at which the output voltage is expected to stay in regulation. If the input voltage falls to less than the nominal output regulation, then the output voltage falls as well.

For a CMOS regulator, the dropout voltage is determined by the drain-source on-state resistance ($R_{DS(ON)}$) of the pass transistor. Therefore, if the linear regulator operates at less than the rated current, the dropout voltage for that current scales accordingly. The following equation calculates the $R_{DS(ON)}$ of the device.

$$R_{DS(ON)} = \frac{V_{DO}}{I_{RATED}} \quad (1)$$

6.3.3 Current Limit

For the legacy chip, the internal current-limit circuit is used to protect the LDO against high-load current faults or shorting events. The LDO is not designed to operate in a steady-state current limit. During a current-limit event, the LDO sources constant current. Therefore, the output voltage falls when load impedance decreases. If a current limit occurs and the resulting output voltage is low, excessive power may be dissipated across the LDO resulting in a thermal shutdown of the output. A foldback feature limits the short-circuit current to protect the regulator from damage under all load conditions. If V_{OUT} is forced below 0 V before ON/$\overline{OFF}$ goes high, and the load current required exceeds the foldback current limit, the device may not start up correctly.

For the new chip, the device has an internal current limit circuit that protects the regulator during transient high-load current faults or shorting events. The current limit is a brick-wall scheme. In a high-load current fault, the brick-wall scheme limits the output current to the current limit (I_{CL}). I_{CL} is listed in the *Electrical Characteristics* table.

The output voltage is not regulated when the device is in current limit. When a current limit event occurs, the device begins to heat up because of the increase in power dissipation. When the device is in brick-wall current limit, the pass transistor dissipates power [($V_{IN} – V_{OUT}$) × I_{CL}]. If thermal shutdown is triggered, the device turns off. After the device cools down, the internal thermal shutdown circuit turns the device back on. If the output current fault condition continues, the device cycles between current limit and thermal shutdown. For more information on current limits, see the *Know Your Limits* application note.

Figure 6-3 shows a diagram of the current limit.

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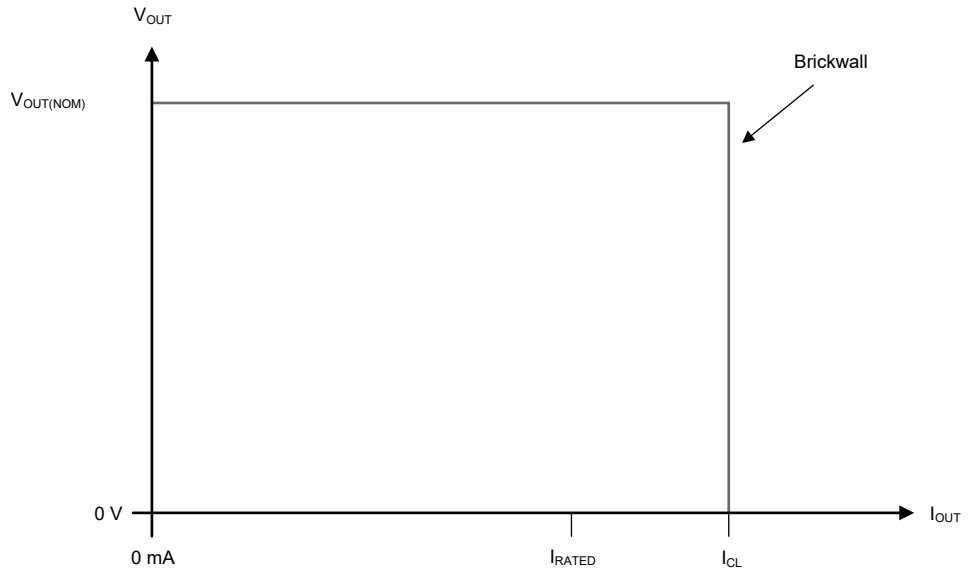

Figure 6-3. Current Limit

6.3.4 Undervoltage Lockout (UVLO)

The new chip version of the device has an independent undervoltage lockout (UVLO) circuit that monitors the input voltage, allowing a controlled and consistent turn on and off of the output voltage. To prevent the device from turning off if the input drops during turn on, the UVLO has hysteresis as specified in the *Electrical Characteristics* table.

6.3.5 Output Pulldown

The new chip has an output pulldown circuit. The output pulldown activates in the following conditions:

- When the device is disabled ($V_{ON/\overline{OFF}} < V_{ON/\overline{OFF}(LOW)}$)
- If 1.0 V < V_{IN} < V_{UVLO}

Do not rely on the output pulldown circuit for discharging a large amount of output capacitance after the input supply has collapsed because reverse current can flow from the output to the input. This reverse current flow can cause damage to the device. See the *Reverse Current* section for more details.

6.3.6 Thermal Shutdown

The device contains a thermal shutdown protection circuit to disable the device when the junction temperature (T_J) of the pass transistor rises to $T_{SD(shutdown)}$ (typical). Thermal shutdown hysteresis enables the device to reset (turns on) when the temperature falls to $T_{SD(reset)}$ (typical). Thermal shutdown circuit limits are defined in *Electrical Characteristics* section.

The thermal time-constant of the semiconductor die is fairly short, thus the device can cycle on and off when thermal shutdown is reached until power dissipation is reduced. Power dissipation during start up can be high from large V_{IN} – V_{OUT} voltage drops across the device or from high inrush currents charging large output capacitors. Under some conditions, the thermal shutdown protection disables the device before start up completes.

For reliable operation, limit the junction temperature to the maximum listed in the *Recommended Operating Conditions* table. Operation above this maximum temperature causes the device to exceed operational specifications. Although the internal protection circuitry of the device is designed to protect against thermal overall conditions, this circuitry is not intended to replace proper heat sinking. Continuously running the device into thermal shutdown or above the maximum recommended junction temperature reduces long-term reliability.

6.4 Device Functional Modes

6.4.1 Device Functional Mode Comparison

Device Functional Mode Comparison shows the conditions that lead to the different modes of operation. See the *Electrical Characteristics* table for parameter values.

Table 6-1. Device Functional Mode Comparison

OPERATING MODE	PARAMETER			
	V_{IN}	$V_{ON/\overline{OFF}}$	I_{OUT}	T_J
Normal operation	$V_{IN} > V_{OUT(nom)} + V_{DO}$ and $V_{IN} > V_{IN(min)}$	$V_{ON/\overline{OFF}} > V_{ON/\overline{OFF}(HI)}$	$I_{OUT} < I_{OUT(max)}$	$T_J < T_{SD(shutdown)}$
Dropout operation	$V_{IN(min)} < V_{IN} < V_{OUT(nom)} + V_{DO}$	$V_{ON/\overline{OFF}} > V_{ON/\overline{OFF}(HI)}$	$I_{OUT} < I_{OUT(max)}$	$T_J < T_{SD(shutdown)}$
Disabled (any true condition disables the device)	$V_{IN} < V_{UVLO}$	$V_{ON/\overline{OFF}} < V_{ON/\overline{OFF}(LOW)}$	Not applicable	$T_J > T_{SD(shutdown)}$

6.4.2 Normal Operation

The device regulates to the nominal output voltage when the following conditions are met:

- The input voltage is greater than the nominal output voltage plus the dropout voltage ($V_{OUT(nom)} + V_{DO}$)
- The output current is less than the current limit ($I_{OUT} < I_{CL}$)
- The device junction temperature is less than the thermal shutdown temperature ($T_J < T_{SD}$)
- The ON/$\overline{OFF}$ voltage has previously exceeded the ON/$\overline{OFF}$ rising threshold voltage and has not yet decreased to less than the enable falling threshold

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6.4.3 Dropout Operation

If the input voltage is lower than the nominal output voltage plus the specified dropout voltage, but all other conditions are met for normal operation, the device operates in dropout mode. In this mode, the output voltage tracks the input voltage. During this mode, the transient performance of the device becomes significantly degraded because the pass transistor is in the ohmic or triode region, and acts as a switch. Line or load transients in dropout can result in large output-voltage deviations.

When the device is in a steady dropout state (defined as when the device is in dropout, $V_{IN} < V_{OUT(NOM)} + V_{DO}$, directly after being in a normal regulation state, but *not* during start up), the pass transistor is driven into the ohmic or triode region. When the input voltage returns to a value greater than or equal to the nominal output voltage plus the dropout voltage ($V_{OUT(NOM)} + V_{DO}$), the output voltage can overshoot for a short period of time while the device pulls the pass transistor back into the linear region.

6.4.4 Disabled

The output of the device can be shutdown by forcing the voltage of the ON/$\overline{\text{OFF}}$ pin to less than the maximum ON/$\overline{\text{OFF}}$ pin low-level input voltage (see the *Electrical Characteristics* table). When disabled, the pass transistor is turned off, internal circuits are shutdown, and the output voltage is actively discharged to ground by an internal discharge circuit from the output to ground.

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7 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

7.1 Application Information

The LP2982 is a linear voltage regulator operating from 2.5 V to 16 V (for new chip) on the input and regulates voltages between 1.2 V to 5 V with ±1% accuracy (across load and temperature) and 50-mA maximum output current.

Successfully implementing an LDO in an application depends on the application requirements. If the requirements are simply input voltage and output voltage, compliance specifications (such as internal power dissipation or stability) must be verified for a solid design. If timing, start-up, noise, power supply rejection ratio (PSRR), or any other transient specification is required, then the design becomes more challenging.

7.1.1 Recommended Capacitor Types

7.1.1.1 Recommended Capacitors (Legacy Chip)

Tantalum Capacitors: Tantalum capacitors are the best choice for use with the LP2982. Most good quality tantalums can be used with the LP2982, but check the manufacturer's data sheet to be sure the ESR is in range. As the ESR increases at lower temperatures and a capacitor that is near the upper limit for stability at room temperature can cause instability when temperature gets cold.

In applications which must operate at very low temperatures, the output tantalum capacitor needs to be placed in parallel with a ceramic capacitor to prevent the ESR from going up too high (see ceramic capacitors discussion in this section for important information on ceramic capacitors).

Ceramic Capacitors: TI does not recommend use of ceramic capacitors at the output of the LP2982. This is because the ESR of a ceramic can be low enough to go below the minimum stable value for the LP2982. A 2.2µF ceramic was measured and found to have an ESR of about 15mΩ, which is low enough to cause oscillations. If a ceramic capacitor is used on the output, a 1Ω resistor must be placed in series with the capacitor.

Aluminum Capacitors: Because of large physical size, aluminum electrolytics are not typically used with the LP2982. The aluminum capacitors must meet the same ESR requirements over the operating temperature range, more difficult because of the ESR steep increase at cold temperature. An aluminum electrolytic can exhibit an ESR increase of as much as 50× when going from 20°C to −40°C. Also, some aluminum electrolytics are not operational below −25°C because the electrolyte can freeze.

7.1.1.2 Recommended Capacitors (New Chip)

The new chip is designed to be stable using low equivalent series resistance (ESR) ceramic capacitors at the input and output. Multilayer ceramic capacitors have become the industry standard for these types of applications and are recommended, but must be used with good judgment. Ceramic capacitors that employ X7R-, X5R-, and C0G-rated dielectric materials provide relatively good capacitive stability across temperature, whereas using Y5V-rated capacitors is discouraged because of large variations in capacitance.

The maximum supported ESR range across complete temperature (−40°C to +125°C) and load current range (0mA-50mA) is less than 1Ω. If in an existing implementation, where different type of capacitors with higher ESR are being used, place a low ESR MLCC capacitor with a value of 100nF, as close as possible to the output (V_{OUT}) pin of the LP2982.

Regardless of the ceramic capacitor type selected, the effective capacitance varies with operating voltage and temperature. Generally, expect the effective capacitance to decrease by as much as 50%. The input and

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output capacitors listed in the *Recommended Operating Conditions* table account for an effective capacitance of approximately 50% of the nominal value.

7.1.2 Input Capacitor Requirements

For the legacy chip, an input capacitor with a value ≥ 1µF is required with the LP2982 (amount of capacitance can be increased without limit). This capacitor must be located a distance of not more than 0.5 inches from the input pin of the LP2982 and returned to a clean analog ground. Any good quality ceramic or tantalum can be used for this capacitor.

For the new chip, although an input capacitor is not required for stability, good analog design practice is to connect a capacitor from IN to GND. This capacitor counteracts reactive input sources and improves transient response, input ripple, and PSRR. Use an input capacitor if the source impedance is more than 0.5 Ω. A higher value capacitor can be necessary if large, fast rise-time load or line transients are anticipated or if the device is located several inches from the input power source.

7.1.3 Output Capacitor Requirements

For the legacy chip, the output capacitor must meet both the requirement for minimum amount of capacitance and equivalent series resistance (ESR) value. Curves are provided which show the allowable ESR range as a function of load current for various output voltages and capacitor values (see Figure 7-1 and Figure 7-2).

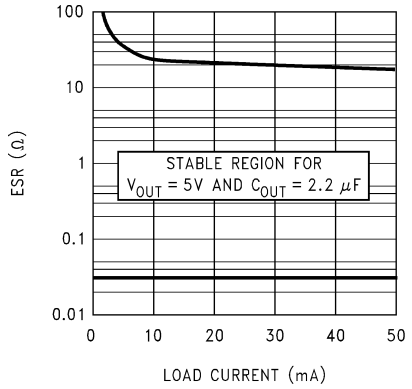

Figure 7-1. 5-V, 2.2-µF ESR Curves (Legacy Chip)

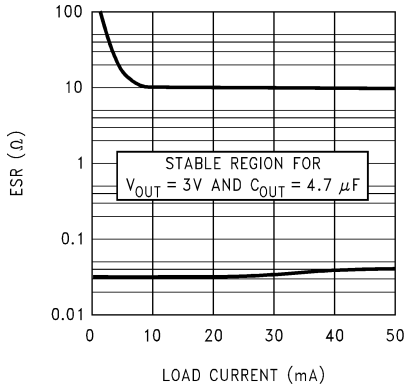

Figure 7-2. 3-V, 4.7-µF ESR Curves (Legacy Chip)

Note

The output capacitor must maintain its ESR in the stable region over the full operating temperature range to ensure stability. Also, capacitor tolerance and variation with temperature must be considered to ensure the minimum amount of capacitance is provided at all times.

This capacitor must be located not more than 0.5 inches from the OUT pin of the LP2982 and returned to a clean analog ground.

For the new chip, dynamic performance of the device is improved with the use of an output capacitor. Use an output capacitor within the range specified in the *Recommended Operating Conditions* table for stability.

7.1.4 Noise Bypass Capacitor (C_{BYPASS})

The LP2982 allows for low-noise performance with the use of a bypass capacitor that is connected to the internal band-gap reference with the BYPASS pin. This high-impedance band-gap circuitry is biased in the microampere range and, thus, cannot be loaded significantly, otherwise, the output (and, correspondingly, the output of the regulator) changes. Thus, for best output accuracy, dc leakage current through C_{BYPASS} must be minimized as much as possible and must never exceed 100 nA. The C_{BYPASS} capacitor also impacts the start-up behavior of the regulator. Inrush current and start-up time increase with larger bypass capacitor values.

Use a 10-nF capacitor for C_{BYPASS}. Ceramic and film capacitors are good choices for this purpose.

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7.1.5 Reverse Current

Excessive reverse current can damage this device. Reverse current flows through the intrinsic body diode of the pass transistor instead of the normal conducting channel. At high magnitudes, this current flow degrades the long-term reliability of the device.

Conditions where reverse current can occur are outlined in this section, all of which can exceed the absolute maximum rating of $V_{OUT} \leq V_{IN} + 0.3$ V.

- If the device has a large C_{OUT} and the input supply collapses with little or no load current
- The output is biased when the input supply is not established
- The output is biased above the input supply

If reverse current flow is expected in the application, use external protection to protect the device. Reverse current is not limited in the device, so external limiting is required if extended reverse voltage operation is anticipated.

Figure 7-3 shows one approach for protecting the device.

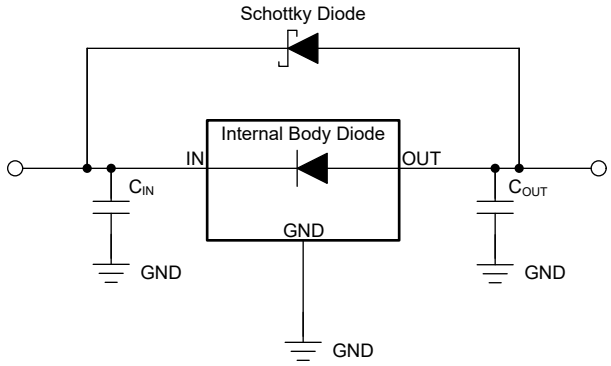

Figure 7-3. Example Circuit for Reverse Current Protection Using a Schottky Diode

7.1.6 Power Dissipation (P_D)

Circuit reliability requires consideration of the device power dissipation, location of the circuit on the printed circuit board (PCB), and correct sizing of the thermal plane. The PCB area around the regulator must have few or no other heat-generating devices that cause added thermal stress.

To first-order approximation, power dissipation in the regulator depends on the input-to-output voltage difference and load conditions. The following equation calculates power dissipation (P_D).

$$P_D = (V_{IN} – V_{OUT}) \times I_{OUT} \quad (2)$$

Note

Power dissipation can be minimized, and therefore greater efficiency can be achieved, by correct selection of the system voltage rails. For the lowest power dissipation use the minimum input voltage required for correct output regulation.

For devices with a thermal pad, the primary heat conduction path for the device package is through the thermal pad to the PCB. Solder the thermal pad to a copper pad area under the device. This pad area must contain an array of plated vias that conduct heat to additional copper planes for increased heat dissipation.

The maximum power dissipation determines the maximum allowable ambient temperature (T_A) for the device. According to the following equation, power dissipation and junction temperature are most often related by the junction-to-ambient thermal resistance ($R_{\theta JA}$) of the combined PCB and device package and the temperature of the ambient air (T_A).

$$T_J = T_A + (R_{\theta JA} \times P_D) \quad (3)$$

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Thermal resistance ($R_{\theta JA}$) is highly dependent on the heat-spreading capability built into the particular PCB design, and therefore varies according to the total copper area, copper weight, and location of the planes. The junction-to-ambient thermal resistance listed in the *Thermal Information* table is determined by the JEDEC standard PCB and copper-spreading area, and is used as a relative measure of package thermal performance.

7.1.7 Estimating Junction Temperature

The JEDEC standard now recommends the use of psi (Ψ) thermal metrics to estimate the junction temperatures of the linear regulator when in-circuit on a typical PCB board application. These metrics are not thermal resistance parameters and instead offer a practical and relative way to estimate junction temperature. These psi metrics are determined to be significantly independent of the copper area available for heat-spreading. The *Thermal Information* table lists the primary thermal metrics, which are the junction-to-top characterization parameter (ψ_{JT}) and junction-to-board characterization parameter (ψ_{JB}). These parameters provide two methods for calculating the junction temperature (T_J), as described in the following equations. Use the junction-to-top characterization parameter (ψ_{JT}) with the temperature at the center-top of device package (T_T) to calculate the junction temperature. Use the junction-to-board characterization parameter (ψ_{JB}) with the PCB surface temperature 1 mm from the device package (T_B) to calculate the junction temperature.

$$T_J = T_T + \psi_{JT} \times P_D \tag{4}$$

where:

- P_D is the dissipated power
- T_T is the temperature at the center-top of the device package

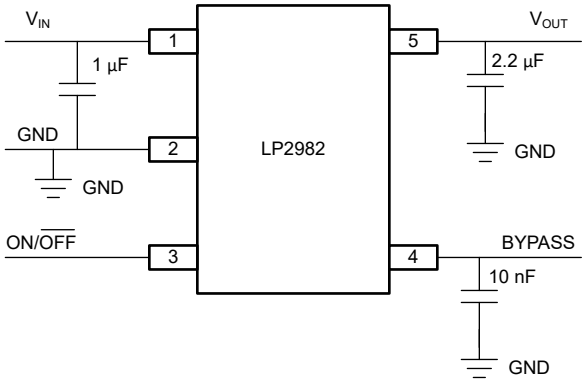
$$T_J = T_B + \psi_{JB} \times P_D \tag{5}$$

where:

- T_B is the PCB surface temperature measured 1 mm from the device package and centered on the package edge

For detailed information on the thermal metrics and how to use them, see the *Semiconductor and IC Package Thermal Metrics* application note.

7.2 Typical Application



ON/ $\overline{\text{OFF}}$ input must be actively terminated. Tie to V_{IN} if this function is not to be used. Minimum output capacitance is shown to insure stability over full load current range. More capacitance provides better dynamic performance and additional stability margin (see the *Recommended Capacitor Types* section).

Figure 7-4. LP2982 Typical Application

7.2.1 Design Requirements

PARAMETER	DESIGN REQUIREMENT
Input voltage	12 V ±10%
Output voltage	3.3 V ±1.5%
Output current	50 mA
Ambient temperature	85°C

7.2.2 Detailed Design Procedure

7.2.2.1 ON/ $\overline{\text{OFF}}$ Input Operation

The LP2982 is shut off by pulling the ON/ $\overline{\text{OFF}}$ input low, and turned on by driving the input high. If this feature is not to be used, the ON/OFF input required to be tied to V_{IN} to keep the regulator on at all times (the ON/ $\overline{\text{OFF}}$ input must **not** be left floating).

For proper operation of the LDO, the signal source used to drive the ON/ $\overline{\text{OFF}}$ input must be able to swing above and below the specified turnon/turnoff voltage thresholds which specify an ON or $\overline{\text{OFF}}$ state.

The ON/ $\overline{\text{OFF}}$ signal can come from either a totem-pole output, or an open-collector output with pullup resistor to the LP2982 input voltage or another logic supply. The high-level voltage can exceed the LP2982 input voltage, but must remain within the absolute maximum ratings for the ON/ $\overline{\text{OFF}}$ pin.

It is also important that the turnon/turnoff voltage signals applied to the ON/ $\overline{\text{OFF}}$ input have a slew rate which is greater than 40 mV/µs.

Note

IMPORTANT: For the legacy chip, the regulator shutdown function does not operate correctly if a slow-moving signal is applied to the ON/ $\overline{\text{OFF}}$ input.

7.2.3 Application Curves

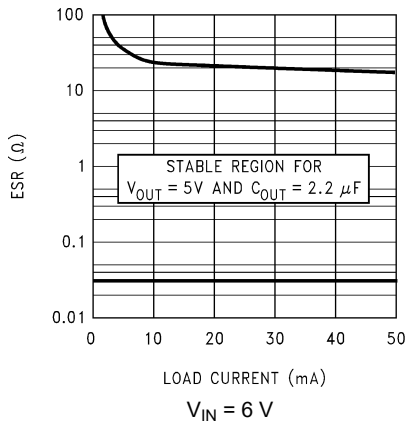


Figure 7-5. 5-V, 2.2-µF ESR Curves (Legacy chip)

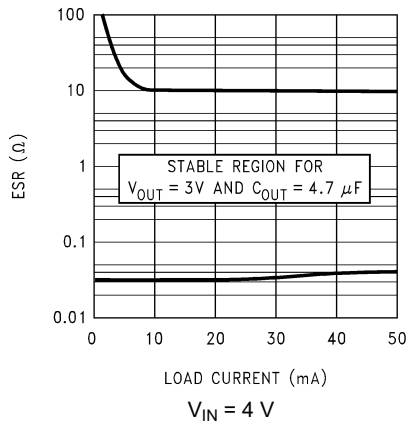


Figure 7-6. 3-V, 4.7-µF ESR Curves (Legacy chip)

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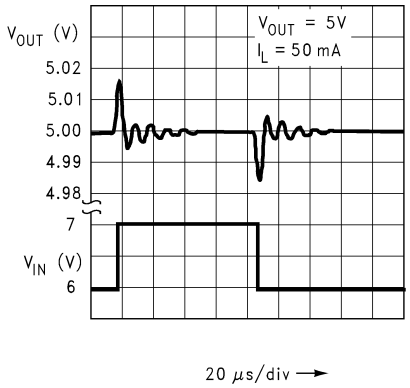


Figure 7-7. Line Transient Response (Legacy chip)

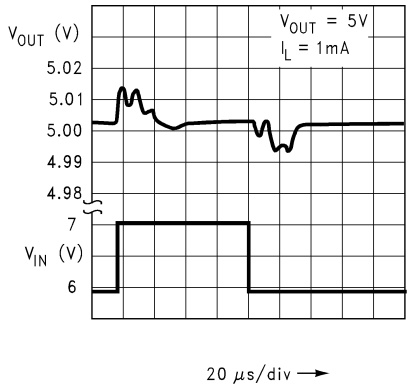
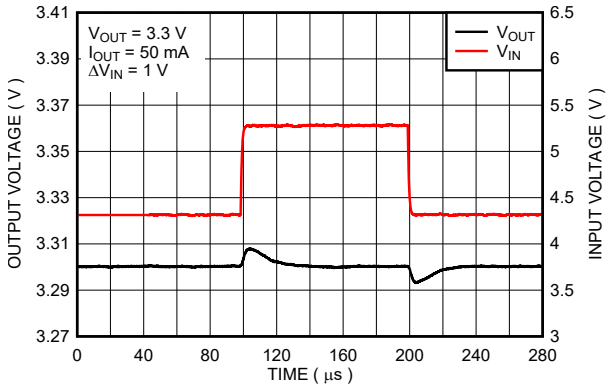


Figure 7-8. Line Transient Response (Legacy chip)



V_{OUT} = 3.3 V, ΔV_{IN} = 1 V, I_{OUT} = 50 mA, dV/dt = 1 V/µs

Figure 7-9. Line Transient Response (New Chip)

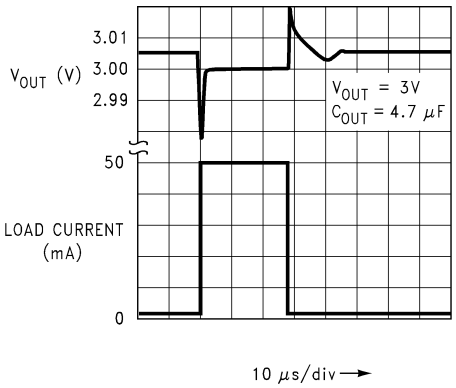


Figure 7-10. Load Transient Response (Legacy chip)

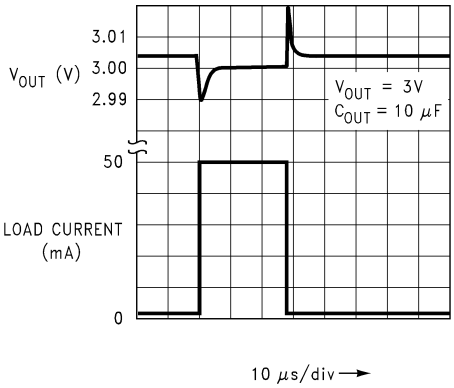


Figure 7-11. Load Transient Response (Legacy chip)

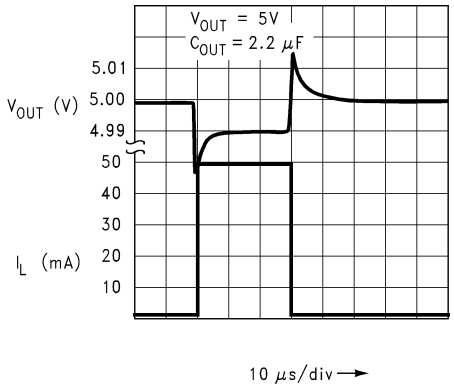


Figure 7-12. Load Transient Response (Legacy chip)

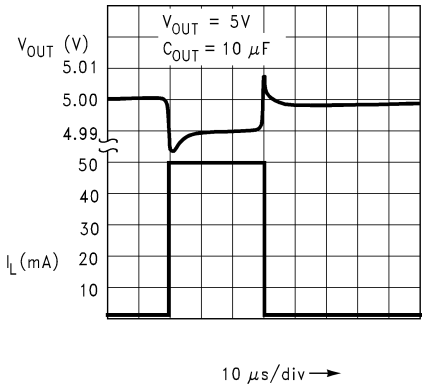
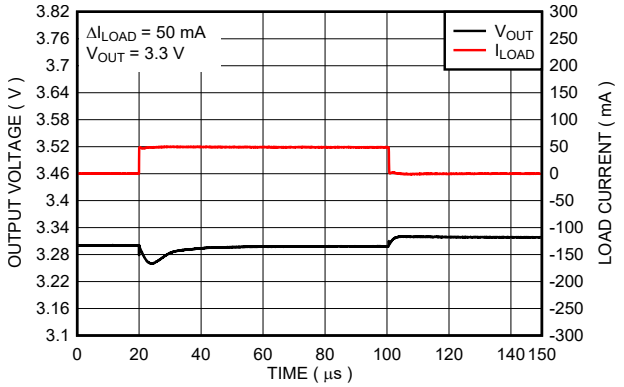


Figure 7-13. Load Transient Response (Legacy chip)



dI/dt = 1 A/µs

Figure 7-14. Load Transient Response (New Chip)

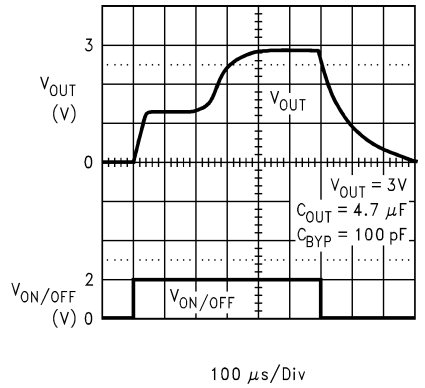


Figure 7-15. Turnon Waveform (Legacy chip)

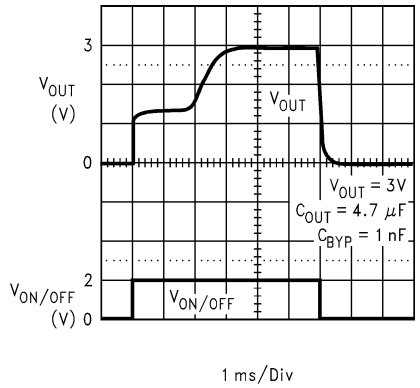


Figure 7-16. Turnon Waveform (Legacy chip)

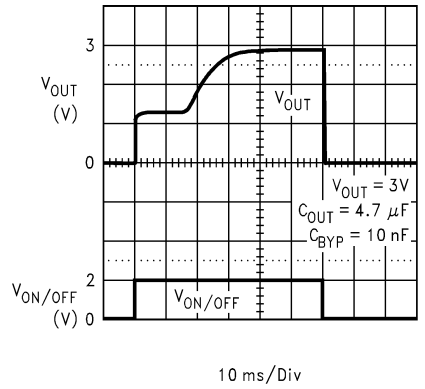
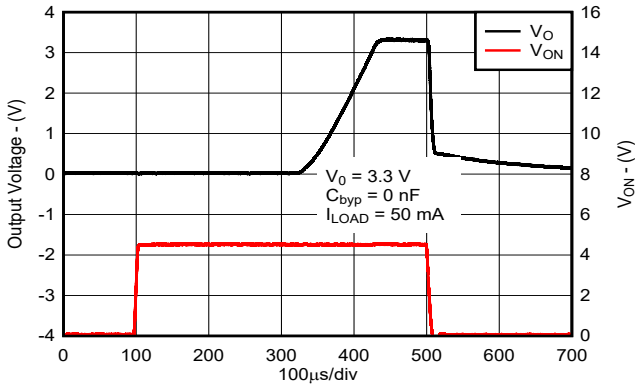


Figure 7-17. Turnon Waveform (Legacy chip)



C_{byp} = 0 nF

Figure 7-18. Turnon Waveform (New chip)

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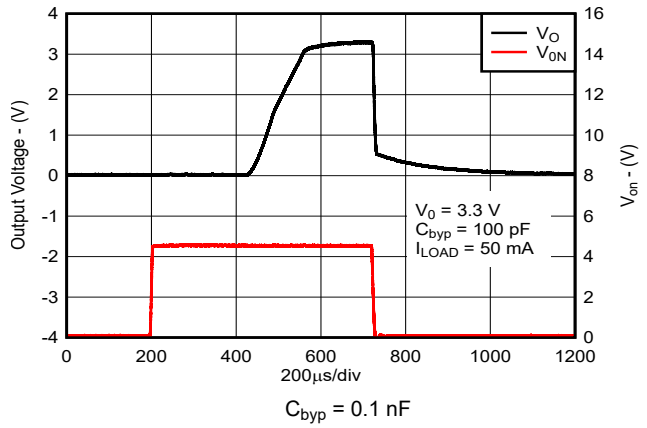
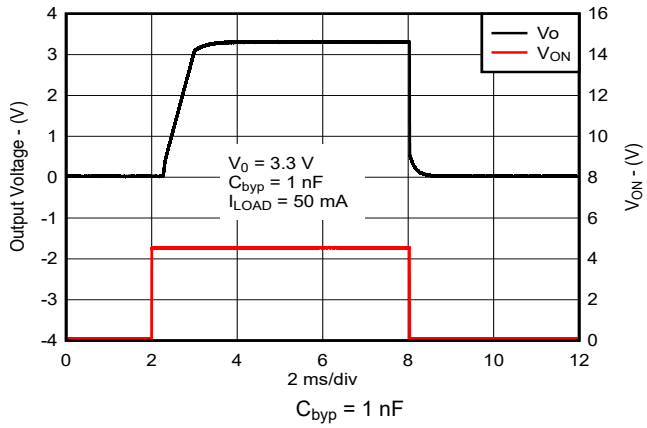


C_{byp} = 0.1 nF

Figure 7-19. Turnon Waveform (New chip)



C_{byp} = 1 nF

Figure 7-20. Turnon Waveform (New chip)

7.3 Power Supply Recommendations

The LP2982 is designed to operate from an input voltage supply range between between $V_{OUT(NOM)}$ + 1 V and 16 V. The input voltage range provides adequate headroom for the device to have a regulated output. This input supply must be well regulated. If the input supply is noisy, additional input capacitors with low ESR can help improve the output noise performance.

7.4 Layout

7.4.1 Layout Guidelines

For best overall performance, place all circuit components on the same side of the circuit board and as near as practical to the respective LDO pin connections. Place ground return connections to the input and output capacitors, and to the LDO ground pin as close to each other as possible, connected by a wide, component-side, copper surface. The use of vias and long traces to create LDO circuit connections is strongly discouraged and negatively affects system performance. This grounding and layout scheme minimizes inductive parasitics, and thereby reduces load-current transients, minimizes noise, and increases circuit stability. A ground reference plane is also recommended and is either embedded in the PCB itself or located on the bottom side of the PCB opposite the components. This reference plane serves for better accuracy of the output voltage, shield noise, and behaves similar to a thermal plane to spread (or sink) heat from the LDO device. In most applications, this ground plane is necessary to meet thermal requirements.

7.4.2 Layout Example

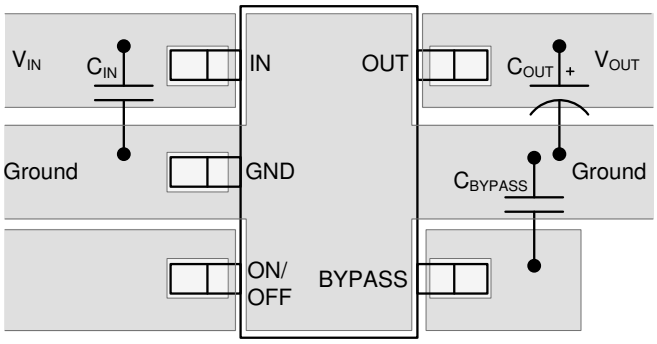


Figure 7-21. LP2982 Layout Example

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8 Device and Documentation Support

8.1 Device Nomenclature

Table 8-1. Available Options

PRODUCT(1)	DESCRIPTION
LP2982**vwxxy-z.z**/NOPB	**v** is the accuracy specification for the legacy chip (A or blank). See the *Section 5.5* for more information. This character is insignificant for the new chip. **w** is the operating temperature range (I = −40°C to +125°C). **xx** is the package designator (M5 = SOT-23). **y** is the reel designator size. See the Package Addendum for more information on package quantity. **z.z** is the nominal output voltage (for example, 3.3 = 3.3 V; 5.0 = 5.0 V). **/NOPB** indicates material construction that does not use Lead (Pb). This device ships with either the legacy chip (CSO: DLN or GF8) or the new chip (CSO:RFB), which uses the latest manufacturing flow. The reel packaging label provides CSO information to distinguish which chip is being used. Device performance for new and legacy chips is denoted throughout the document.

(1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or visit the device product folder at www.ti.com.

8.2 Third-Party Products Disclaimer

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8.3 Documentation Support

8.3.1 Related Documentation

For additional information, see the following:

- Texas Instruments, *Semiconductor and IC Package Thermal Metrics* application note
- Texas Instruments, *Using New Thermal Metrics* application note
- Texas Instruments, *Thermal Characteristics of Linear and Logic Packages Using JEDEC PCB Designs* application note

8.4 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

8.5 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

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8.7 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

8.8 Glossary

TI Glossary This glossary lists and explains terms, acronyms, and definitions.

9 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision L (December 2023) to Revision M (June 2025)	Page
• Changed entire document to identify the features and differences of the legacy chip and new chip	1
• Changed soft-start discussion pertaining to the new chip in *Description*section	1
• Changed *Overview* section	19
• Changed *Functional Block Diagrams* section	19
• Changed *Current Limit* section	20
• Changed *Recommended Capacitors (Legacy Chip)* section	24
• Changed *Recommended Capacitors (New Chip)* section	24
• Changed *Input Capacitor Requirements* section	25
• Changed *Input and Output Capacitor Requirements* section	25
• Changed *Device Nomenclature* section	33

Changes from Revision K (June 2016) to Revision L (December 2023)	Page
• Updated the numbering format for tables, figures, and cross-references throughout the document	1
• Changed entire document to align with current family format	1
• Added M3 devices to document	1

10 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

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PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
LP2982AIM5-3.0/NO.A	Active	Production	SOT-23 (DBV) | 5	1000 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	L20A
LP2982AIM5-3.0/NOPB	Active	Production	SOT-23 (DBV) | 5	1000 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	L20A
LP2982AIM5-3.3/NO.A	Active	Production	SOT-23 (DBV) | 5	3000 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	L19A
LP2982AIM5-3.3/NOPB	Active	Production	SOT-23 (DBV) | 5	3000 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	L19A
LP2982AIM5-5.0/NO.A	Active	Production	SOT-23 (DBV) | 5	3000 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	L18A
LP2982AIM5-5.0/NOPB	Active	Production	SOT-23 (DBV) | 5	3000 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	L18A
LP2982AIM5X-3.0/NO.A	Active	Production	SOT-23 (DBV) | 5	3000 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	L20A
LP2982AIM5X-3.0/NOPB	Active	Production	SOT-23 (DBV) | 5	3000 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	L20A
LP2982AIM5X-3.3/NO.A	Active	Production	SOT-23 (DBV) | 5	3000 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	L19A
LP2982AIM5X-3.3/NOPB	Active	Production	SOT-23 (DBV) | 5	3000 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	L19A
LP2982AIM5X-5.0/NO.A	Active	Production	SOT-23 (DBV) | 5	3000 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	L18A
LP2982AIM5X-5.0/NOPB	Active	Production	SOT-23 (DBV) | 5	3000 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	L18A
LP2982IM5-3.0/NOPB	Active	Production	SOT-23 (DBV) | 5	1000 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	L20B
LP2982IM5-3.0/NOPB.A	Active	Production	SOT-23 (DBV) | 5	1000 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	L20B
LP2982IM5-3.0/NOPB.B	Active	Production	SOT-23 (DBV) | 5	1000 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	L20B
LP2982IM5-3.3/NOPB	Active	Production	SOT-23 (DBV) | 5	3000 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	L19B
LP2982IM5-3.3/NOPB.A	Active	Production	SOT-23 (DBV) | 5	3000 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	L19B
LP2982IM5-5.0/NOPB	Active	Production	SOT-23 (DBV) | 5	3000 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	L18B
LP2982IM5-5.0/NOPB.A	Active	Production	SOT-23 (DBV) | 5	3000 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	L18B
LP2982IM5X-3.0/NO.A	Active	Production	SOT-23 (DBV) | 5	3000 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	L20B
LP2982IM5X-3.0/NOPB	Active	Production	SOT-23 (DBV) | 5	3000 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	L20B
LP2982IM5X-3.3/NO.A	Active	Production	SOT-23 (DBV) | 5	3000 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	L19B
LP2982IM5X-3.3/NOPB	Active	Production	SOT-23 (DBV) | 5	3000 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	L19B
LP2982IM5X-5.0/NO.A	Active	Production	SOT-23 (DBV) | 5	3000 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	L18B
LP2982IM5X-5.0/NOPB	Active	Production	SOT-23 (DBV) | 5	3000 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	L18B

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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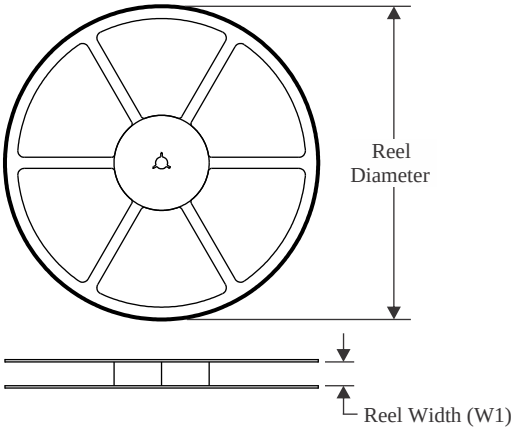
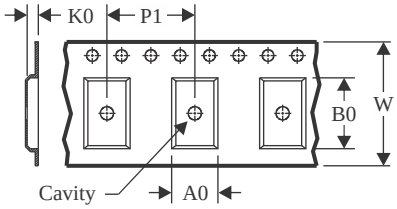
TAPE AND REEL INFORMATION

REEL DIMENSIONS

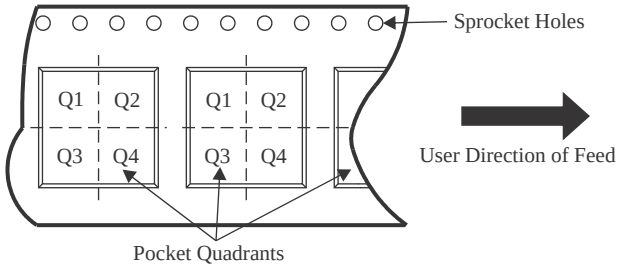


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE

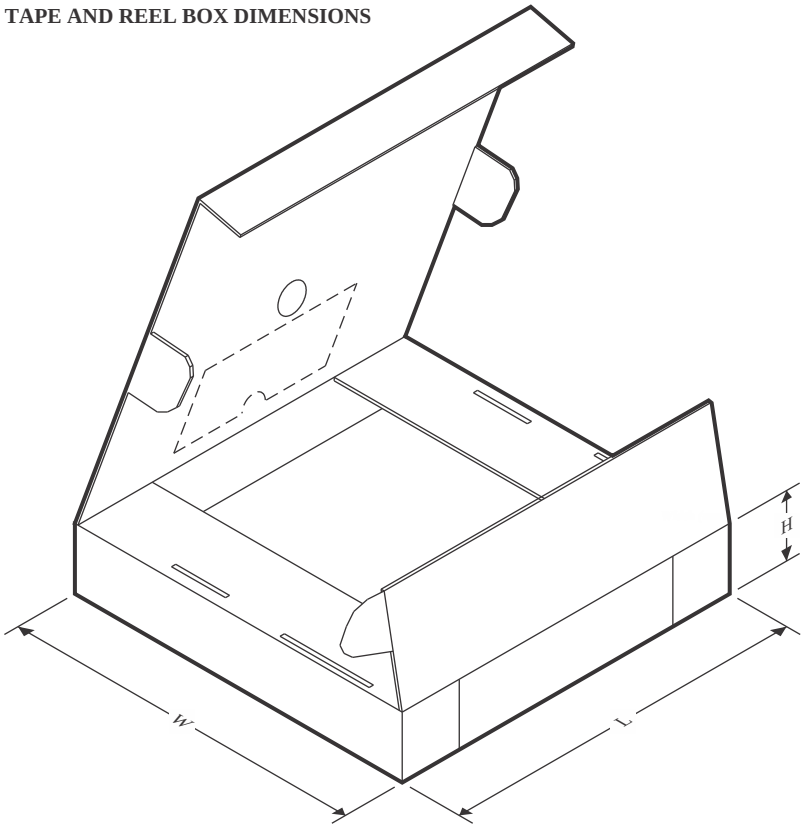


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LP2982AIM5-3.0/NOPB	SOT-23	DBV	5	1000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LP2982AIM5-3.3/NOPB	SOT-23	DBV	5	3000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LP2982AIM5-3.3/NOPB	SOT-23	DBV	5	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LP2982AIM5-5.0/NOPB	SOT-23	DBV	5	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LP2982AIM5-5.0/NOPB	SOT-23	DBV	5	3000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LP2982AIM5X-3.0/NOPB	SOT-23	DBV	5	3000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LP2982AIM5X-3.3/NOPB	SOT-23	DBV	5	3000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LP2982AIM5X-5.0/NOPB	SOT-23	DBV	5	3000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LP2982AIM5X-5.0/NOPB	SOT-23	DBV	5	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LP2982IM5-3.0/NOPB	SOT-23	DBV	5	1000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LP2982IM5-3.3/NOPB	SOT-23	DBV	5	3000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LP2982IM5-3.3/NOPB	SOT-23	DBV	5	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LP2982IM5-5.0/NOPB	SOT-23	DBV	5	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LP2982IM5-5.0/NOPB	SOT-23	DBV	5	3000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LP2982IM5X-3.0/NOPB	SOT-23	DBV	5	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LP2982IM5X-3.0/NOPB	SOT-23	DBV	5	3000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LP2982IM5X-3.3/NOPB	SOT-23	DBV	5	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LP2982IM5X-3.3/NOPB	SOT-23	DBV	5	3000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LP2982IM5X-5.0/NOPB	SOT-23	DBV	5	3000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LP2982AIM5-3.0/NOPB	SOT-23	DBV	5	1000	208.0	191.0	35.0
LP2982AIM5-3.3/NOPB	SOT-23	DBV	5	3000	208.0	191.0	35.0
LP2982AIM5-3.3/NOPB	SOT-23	DBV	5	3000	210.0	185.0	35.0
LP2982AIM5-5.0/NOPB	SOT-23	DBV	5	3000	210.0	185.0	35.0
LP2982AIM5-5.0/NOPB	SOT-23	DBV	5	3000	208.0	191.0	35.0
LP2982AIM5X-3.0/NOPB	SOT-23	DBV	5	3000	208.0	191.0	35.0
LP2982AIM5X-3.3/NOPB	SOT-23	DBV	5	3000	208.0	191.0	35.0
LP2982AIM5X-5.0/NOPB	SOT-23	DBV	5	3000	208.0	191.0	35.0
LP2982AIM5X-5.0/NOPB	SOT-23	DBV	5	3000	210.0	185.0	35.0
LP2982IM5-3.0/NOPB	SOT-23	DBV	5	1000	208.0	191.0	35.0
LP2982IM5-3.3/NOPB	SOT-23	DBV	5	3000	208.0	191.0	35.0
LP2982IM5-3.3/NOPB	SOT-23	DBV	5	3000	210.0	185.0	35.0
LP2982IM5-5.0/NOPB	SOT-23	DBV	5	3000	210.0	185.0	35.0
LP2982IM5-5.0/NOPB	SOT-23	DBV	5	3000	208.0	191.0	35.0
LP2982IM5X-3.0/NOPB	SOT-23	DBV	5	3000	210.0	185.0	35.0
LP2982IM5X-3.0/NOPB	SOT-23	DBV	5	3000	208.0	191.0	35.0
LP2982IM5X-3.3/NOPB	SOT-23	DBV	5	3000	210.0	185.0	35.0
LP2982IM5X-3.3/NOPB	SOT-23	DBV	5	3000	208.0	191.0	35.0

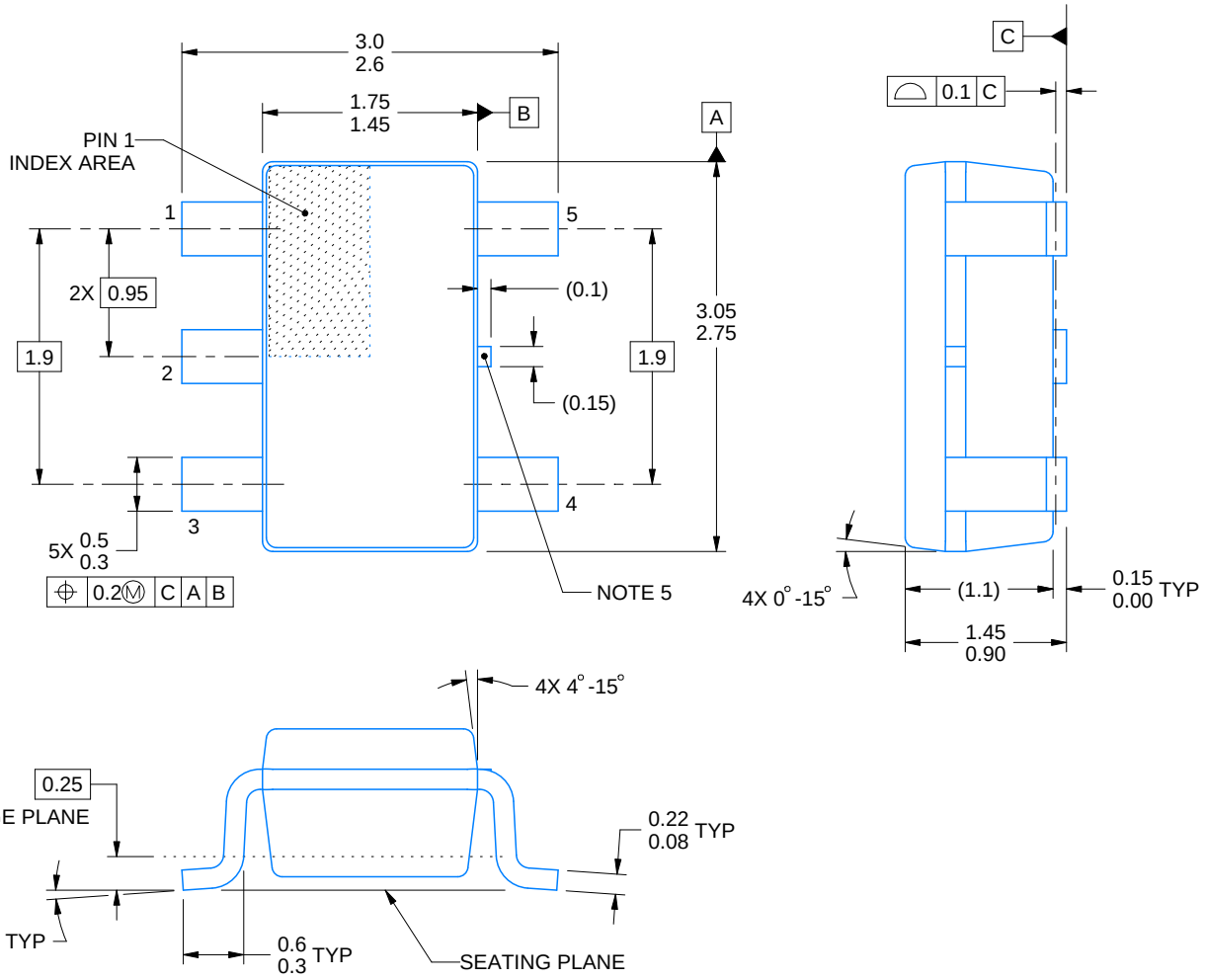
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LP2982IM5X-5.0/NOPB	SOT-23	DBV	5	3000	208.0	191.0	35.0

PACKAGE OUTLINE

DBV0005A

SOT-23 - 1.45 mm max height

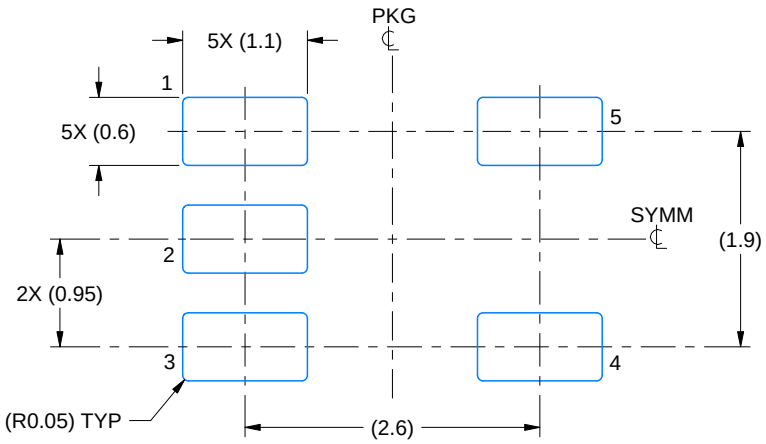
SMALL OUTLINE TRANSISTOR



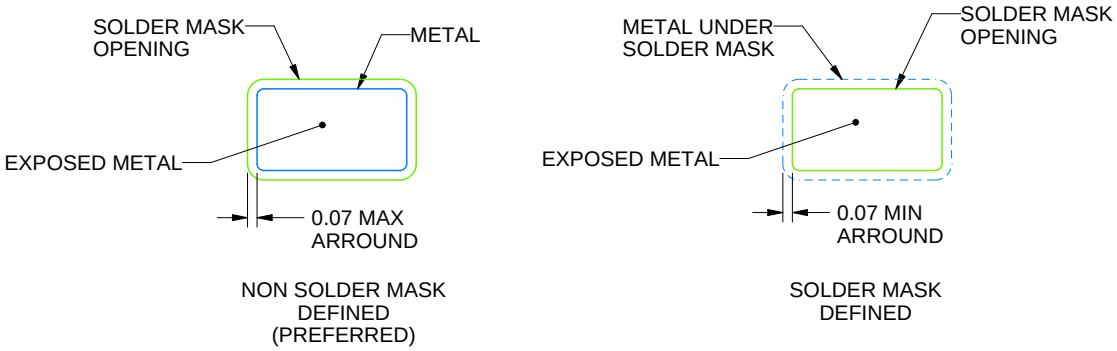
4214839/K 08/2024

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Refernce JEDEC MO-178.
4. Body dimensions do not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.25 mm per side.
5. Support pin may differ or may not be present.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:15X

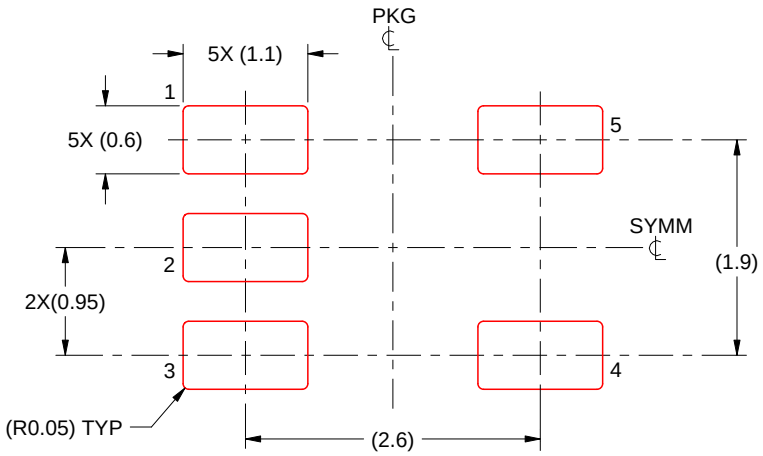


SOLDER MASK DETAILS

4214839/K 08/2024

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:15X

4214839/K 08/2024

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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