MIC5373/83

Triple 200mA µCap LDO in 2.5mm x 2.5mm Thin MLF®

General Description

The MIC5373/83 is a triple output device with three 200mA LDOs which is ideal for application processor support in mobile platforms. The MIC5373 provides independent control active high enables for each of the 200mA LDOs. The MIC5383 provides active low enables. Both the MIC5373 and MIC5383 are available in the tiny 2.5mm x 2.5mm Thin MLF® package.

The MIC5373/83 is designed for high input ripple rejection (high PSRR) and provides low output noise making it ideal for powering sensitive RF circuitry such as GPS, WiFi and Bluetooth applications. The MIC5373/83 also incorporates a power-on-reset (POR) supervisor with adjustable delay time set by an external capacitor, and an independent input pin to monitor any voltage level. Once high, the POR output can be asserted low again by enabling the manual reset (MR) pin. When the MR pin is restored low, the POR output will re-time the delay set by the external delay capacitor.

The MIC5373/83 operates with very small ceramic output capacitors to reduce board space and component cost. It is available in various fixed output voltages. The MIC5373/83 has a junction temperature range from –40°C to 125°C.

Datasheets and support documentation can be found on Micrel's web site at: www.micrel.com.

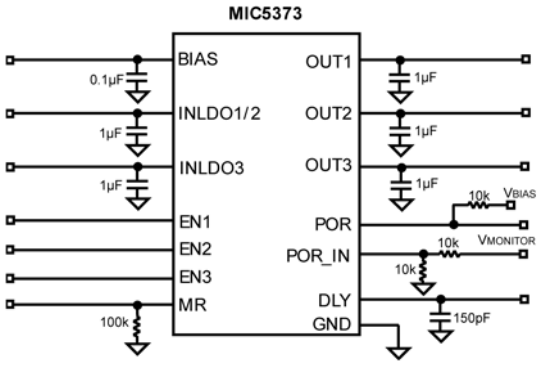
Features

- 1.7V to 5.5V input supply voltage range
- Output current - 200mA LDO1/2/3
- High output accuracy (±2%)
- Independent enable pins
- POR with user-defined voltage monitoring
  - POR voltage input
  - Adjustable delay time
  - Manual reset pin
- Low dropout voltage – 170mV at 150mA
- High PSRR - 55dB at 1kHz on each LDO
- Stable with tiny ceramic output capacitors
- 2.5mm x 2.5mm Thin MLF16-pin package
- Thermal-shutdown and current-limit protection

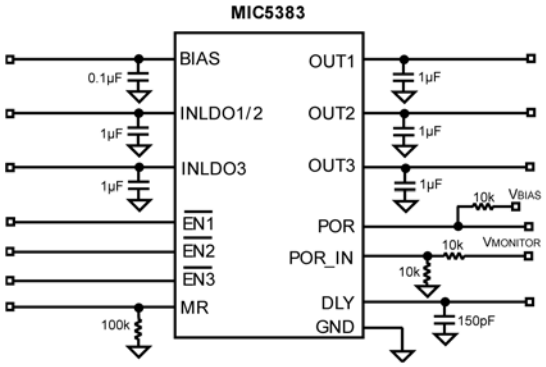
Applications

- Mobile phones
- GPS receivers
- Application co-processors
- PDAs and handheld devices

Typical Application



Typical MIC5373-xxxYMT Circuit (Active High Enable)



Typical MIC5383-xxxYMT Circuit (Active Low Enable)

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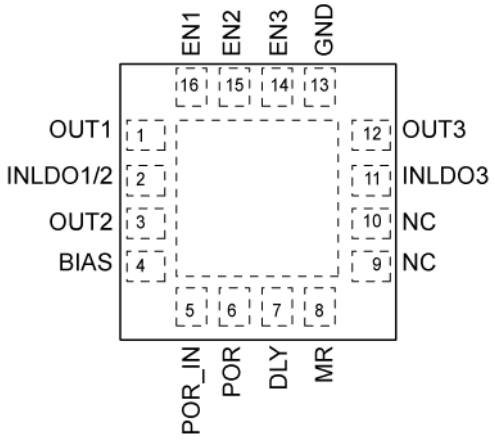
Ordering Information

Part Number	Mark Code	Output Voltage[1]	Junction Temperature Range	Package	Lead Finish
MIC5373-MG4YMT	MG4	2.8V/1.8V/1.2V	–40° to +125°C	16-Pin 2.5mm x 2.5mm Thin MLF	Pb-free
MIC5373-SJGYMT	SJG	3.3V/2.5V/1.8V	–40° to +125°C	16-Pin 2.5mm x 2.5mm Thin MLF	Pb-free
MIC5383-MG4YMT	Z1T	2.8V/1.8V/1.2V	–40° to +125°C	16-Pin 2.5mm x 2.5mm Thin MLF	Pb-free
MIC5383-SJGYMT	Z5T	3.3V/2.5V/1.8V	–40° to +125°C	16-Pin 2.5mm x 2.5mm Thin MLF	Pb-free

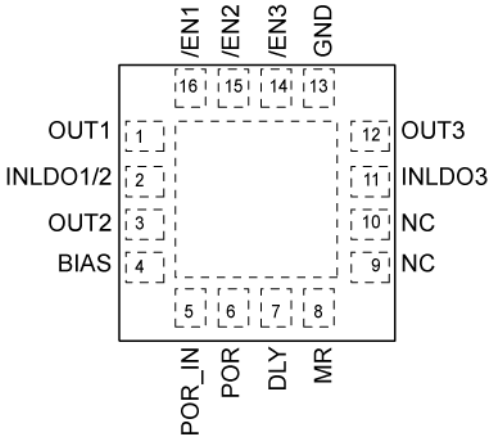
Note:

1. Other voltage options available. Contact Micrel for details.
2. Lead finish is NiPdAu. Mold compound material is halogen free.

Pin Configuration



MIC5373
16-Pin 2.5mm x 2.5mm Thin MLF (MT)
(Top View)



MIC5383
16-Pin 2.5mm x 2.5mm Thin MLF (MT)
(Top View)

Pin Description

Pin Number	Pin Name	Pin Function
1	OUT1	Regulator Output - LDO1.
2	INLDO1/2	Supply Input (LDO1/2).
3	OUT2	Regulator Output – LDO2.
4	BIAS	Internal Bias Supply Voltage. Must be de-coupled to ground with a 0.1µF capacitor.
5	POR_IN	Input to POR. Connect directly to output voltage or input voltage that is to be monitored for a 0.9V reference, or connect a resistor divider network to this pin to program the POR monitoring voltage.
6	POR	Power-on Reset Output. Open drain.
7	DLY	POR Delay. Connect capacitor to ground to set POR delay time.
8	MR	Manual Reset Input. Manually resets output of POR and delay generator. Do not leave floating.
9	NC	Not internally connected.
10	NC	Not internally connected.
11	INLDO3	Supply Input (LDO3).
12	OUT3	Regulator Output – LDO3.
13	GND	Ground.
14	EN3 or /EN3	LDO3 Enable Input. EN (MIC5373): Active High Input. Logic High = On; Logic Low = Off; /EN (MIC5383): Active Low Input. Logic High = Off; Logic Low = On; Do not leave floating.
15	EN2 or /EN2	LDO2 Enable Input. EN (MIC5373): Active High Input. Logic High = On; Logic Low = Off; /EN (MIC5383): Active Low Input. Logic High = Off; Logic Low = On; Do not leave floating.
16	EN1 or /EN1	LDO1 Enable Input. EN (MIC5373): Active High Input. Logic High = On; Logic Low = Off; /EN (MIC5383): Active Low Input. Logic High = Off; Logic Low = On; Do not leave floating.
HS Pad	EPAD	Exposed Heat Sink Pad. Connect to GND.

Absolute Maximum Ratings[1]

Supply Voltage ($V_{INLDO1/2, INLDO3}$) ..... –0.3V to +6V
Bias Supply Voltage (V_{BIAS}) ..... –0.3V to +6V
Enable Input Voltage ($V_{EN1, EN2, EN3}$) ..... –0.3V to +6V
POR Output Voltage (POR) ..... –0.3V to +6V
POR Input Voltage (POR_IN) ..... –0.3V to +6V
MR Voltage (MR) ..... –0.3V to +6V
DLY Voltage (DLY) ..... –0.3V to +6V
Power Dissipation ..... Internally Limited[2]
Lead Temperature (soldering, 10s) ..... 260°C
Storage Temperature (T_s) ..... –60°C to +150°C
ESD Rating[3] ..... ESD Sensitive

Operating Ratings[4]

Supply Voltage[5] ($V_{INLDO1/2, INLDO3}$) ..... +1.7V to V_{BIAS}
Bias Supply Voltage (V_{BIAS}) ..... +2.5V to +5.5V
Enable Input Voltage ($V_{EN1, EN2, EN3}$) ..... 0V to V_{BIAS}
POR Output Voltage (POR) ..... 0V to +5.5V
POR Input Voltage (POR_IN) ..... 0V to V_{BIAS}
MR Voltage (MR) ..... 0V to V_{BIAS}
DLY Voltage (DLY) ..... 0V to V_{BIAS}
Junction Temperature (T_J) ..... –40°C to +125°C
Junction Thermal Resistance
2.5mm x 2.5mm Thin MLF-16L (θ_{JA}) ..... 100°C/W

Electrical Characteristics[6]

(MIC5373) $V_{IN} = V_{OUT} + 1V$ (V_{OUT} is highest of the three regulator outputs); $V_{BIAS} = V_{EN1} = V_{EN2} = V_{EN3} = 5.5V$ (ON);
(MIC5383) $V_{IN} = V_{OUT} + 1V$ (V_{OUT} is highest of the three regulator outputs); $V_{BIAS} = 5.5V$; $V_{/EN1} = V_{/EN2} = V_{/EN3} = GND$ (ON);
$I_{OUT1} = I_{OUT2} = I_{OUT3} = 100\mu A$; $C_{OUT1} = C_{OUT2} = C_{OUT3} = 1\mu F$; $T_A = 25°C$, **Bold** values indicate $–40°C \le T_J \le +125°C$, unless noted.

Parameter	Conditions	Min.	Typ.	Max.	Units
Output Voltage Accuracy	Variation from nominal $V_{OUT1, 2, 3}$	–2.0		+2.0	%
	Variation from nominal $V_{OUT1, 2, 3}$	**–3.0**		**+3.0**	
Line Regulation	$V_{IN} = V_{OUT}$ +1V to 5.5V; I_{OUT} = 100µA		0.02	0.3	%/V
Load Regulation	I_{OUT} = 100µA to 150mA;		0.3	1	%
Dropout Voltage	I_{OUT} = 50mA; $V_{OUT} \ge 2.8V$		60	**115**	mV
	I_{OUT} = 150mA; $V_{OUT} \ge 2.8V$		170	**330**	
	I_{OUT} = 50mA; $V_{OUT} < 2.8V$		85	**145**	
	I_{OUT} = 150mA; $V_{OUT} < 2.8V$		275	**450**	
Input Ground Current	EN1 or EN2 or EN3 = ON; Not including I_{BIAS}		10	**20**	µA
Bias Ground Current	EN1 or EN2 or EN3 = ON		32	**70**	µA
	EN1 = EN2 = EN3 = ON		103	**160**	
Shutdown Ground Current	EN1 = EN2 = EN3 = OFF		0.04	**2**	µA
Shutdown Bias Current	EN1 = EN2 = EN3 = OFF		0.02	**2**	µA
Ripple Rejection	f = 1kHz; C_{OUT} = 1.0µF		55		dB
Current Limit	V_{OUT} = 0V	**200**	350	700	mA
Output Voltage Noise	C_{OUT} =1µF,10Hz to 100kHz; I_{OUT} = 150mA		200		μV_{RMS}
Enable Input Voltage	(MIC5373) LDO OFF; (MIC5383) LDO ON			**0.2**	V
	(MIC5373) LDO ON; (MIC5383) LDO OFF	**1.2**			
Enable Input Current	VIL ≤ 0.2V		0.01		µA
	VIH ≥ 1.2V		0.01		
Turn-On Time	C_{OUT} = 1µF		80	**200**	µs
V_{POR}	POR Output Low Voltage			**0.2**	V

Notes:

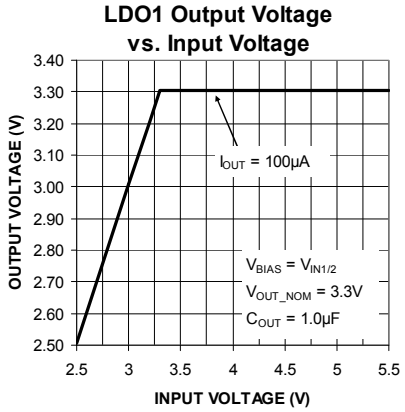
1. Exceeding the absolute maximum rating may damage the device.
2. The maximum allowable power dissipation of any T_A (ambient temperature) is $P_{D(max)} = (T_{J(max)} – T_A) / \theta_{JA}$. Exceeding the maximum allowable power dissipation will result in excessive die temperature and the regulator will go into thermal shutdown.
3. Devices are ESD sensitive. Handling precautions recommended. Human body model, 1.5kΩ in series with 100pF.
4. The device is not guaranteed to function outside its operating rating.
5. For V_{IN} range of 1.7V to 2.5V, output current is limited to 30mA.
6. Specification for packaged product only.

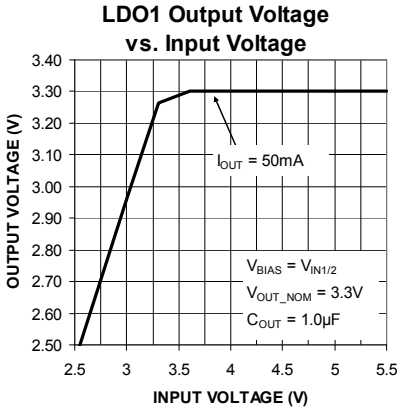
Electrical Characteristics[6]

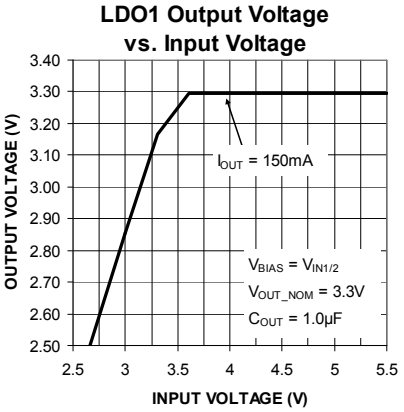
(MIC5373) $V_{IN} = V_{OUT} + 1V$ (V_{OUT} is highest of the three regulator outputs); $V_{BIAS} = V_{EN1} = V_{EN2} = V_{EN3} = 5.5V$ (ON);
(MIC5383) $V_{IN} = V_{OUT} + 1V$ (V_{OUT} is highest of the three regulator outputs); $V_{BIAS} = 5.5V$; $V_{/EN1} = V_{/EN2} = V_{/EN3} = GND$ (ON);
$I_{OUT1} = I_{OUT2} = I_{OUT3} = 100\mu A$; $C_{OUT1} = C_{OUT2} = C_{OUT3} = 1\mu F$; $T_A = 25°C$, **Bold** values indicate $–40°C \le T_J \le +125°C$, unless noted.

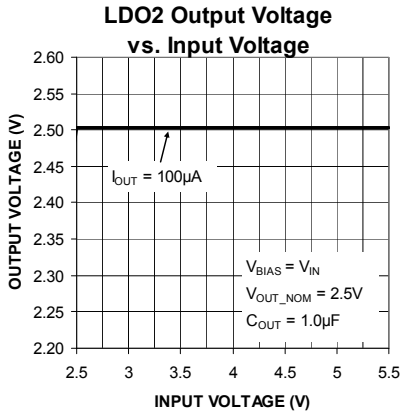
Parameter	Conditions	Min.	Typ.	Max.	Units
DLY Pin Current Source	$V_{DLY} = 0V$	**0.75**	1.25	**2**	µA
DLY Pin Voltage Threshold		**1.13**	1.25	**1.38**	V
I_{POR}	POR Output Leakage Current, V_{POR} OFF		1		µA
V_{TH}	POR Undervoltage Threshold	**0.873**	0.9	**0.927**	V
V_{HYS}	POR Hysteresis		34		mV
I_{POR_IN}	POR Input Pin Leakage Current		1		µA
Thermal Shutdown			155		°C
Thermal-Shutdown Hysteresis			10		°C

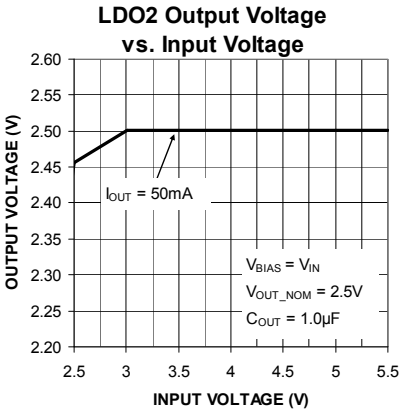
Typical Characteristics

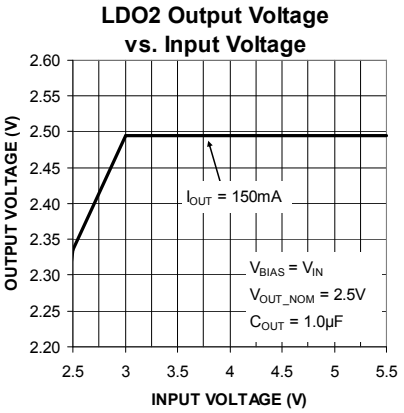


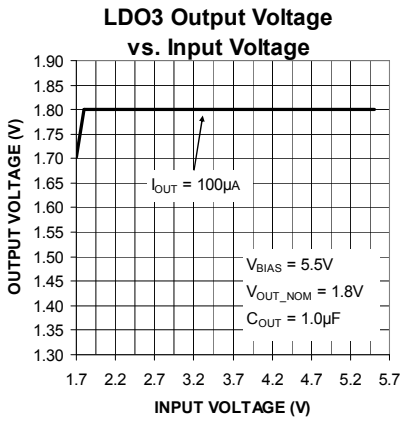


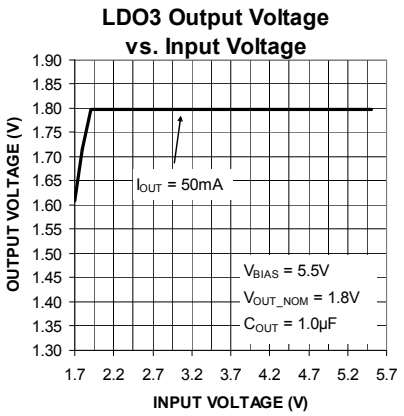


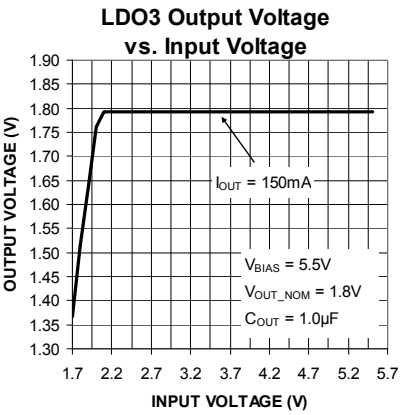






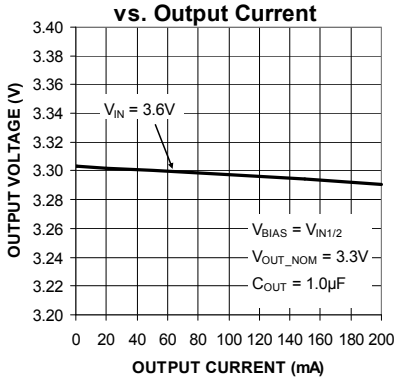




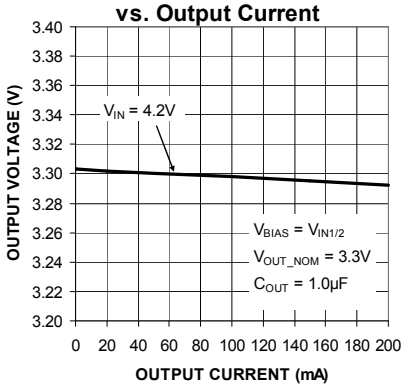


Typical Characteristics (Continued)

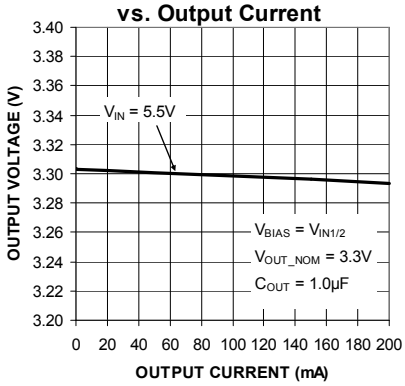
LDO1 Output Voltage vs. Output Current



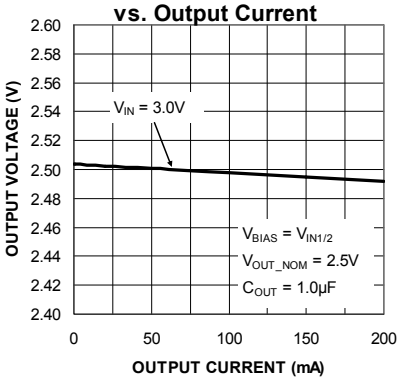
LDO1 Output Voltage vs. Output Current



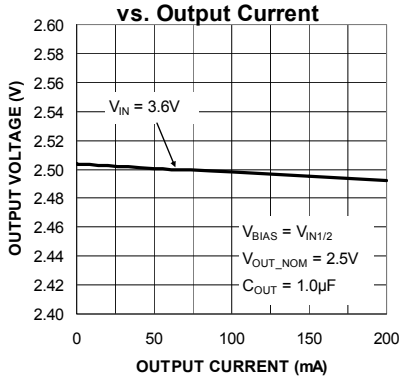
LDO1 Output Voltage vs. Output Current



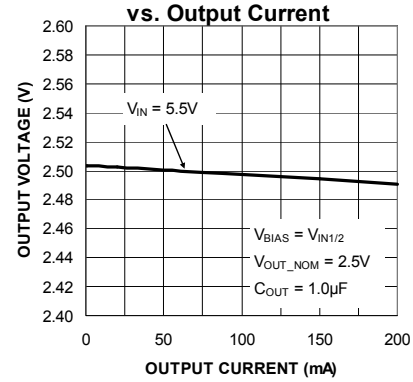
LDO2 Output Voltage vs. Output Current



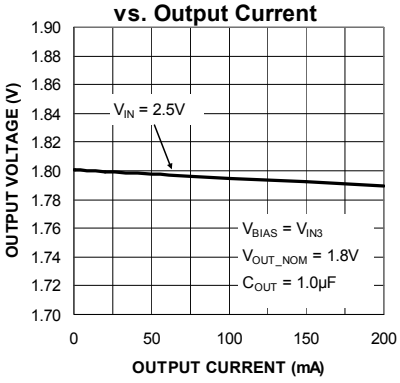
LDO2 Output Voltage vs. Output Current



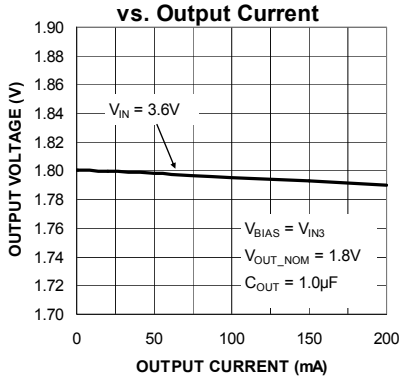
LDO2 Output Voltage vs. Output Current



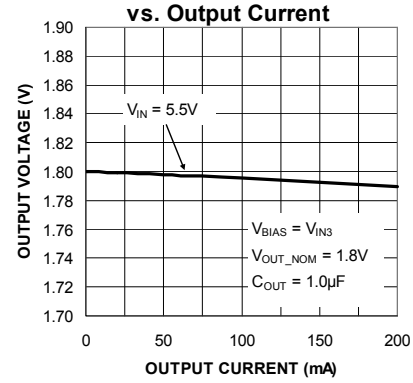
LDO3 Output Voltage vs. Output Current



LDO3 Output Voltage vs. Output Current

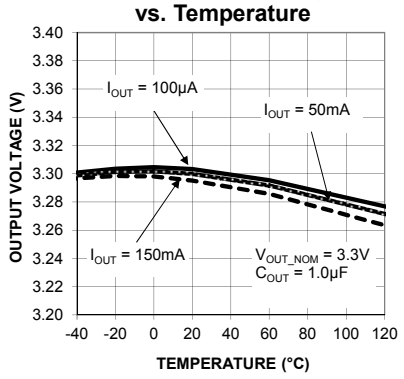


LDO3 Output Voltage vs. Output Current

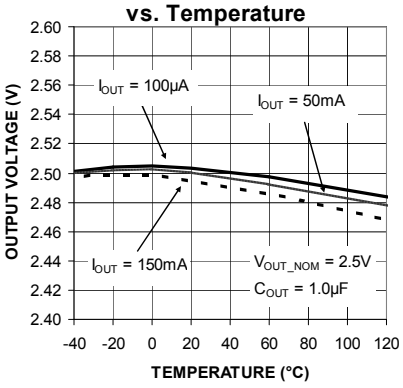


Typical Characteristics (Continued)

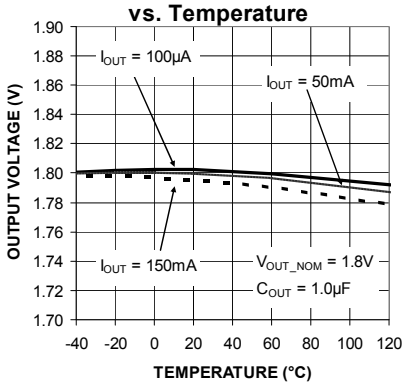
LDO1 Output Voltage vs. Temperature



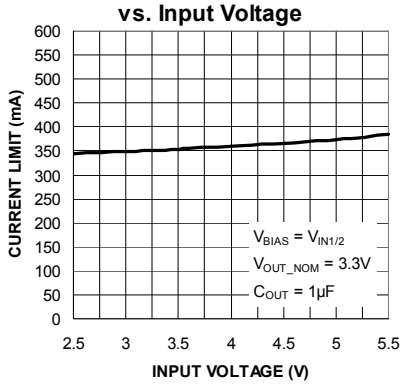
LDO2 Output Voltage vs. Temperature



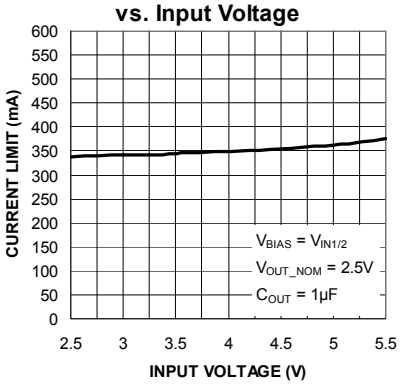
LDO3 Output Voltage vs. Temperature



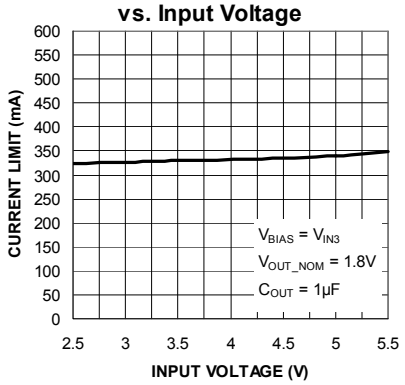
LDO1 Current Limit vs. Input Voltage



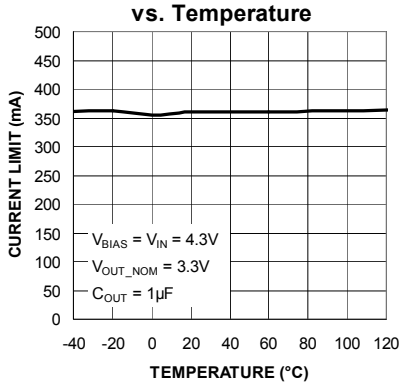
LDO2 Current Limit vs. Input Voltage



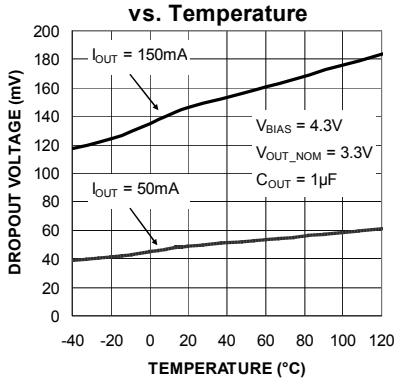
LDO3 Current Limit vs. Input Voltage



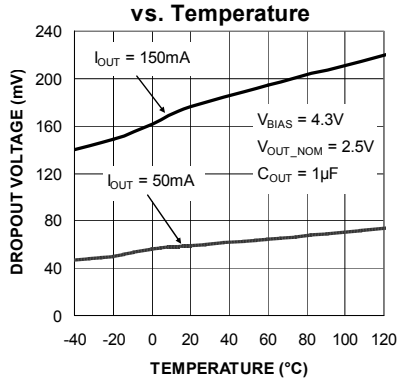
LDO1/2/3 Current Limit vs. Temperature



LDO1 Dropout Voltage vs. Temperature

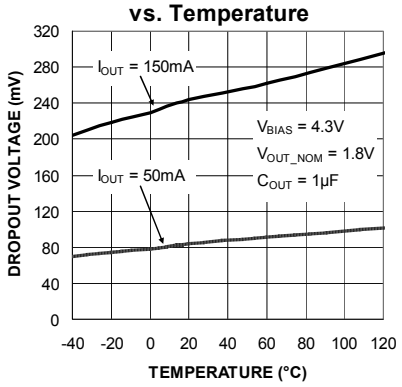


LDO2 Dropout Voltage vs. Temperature

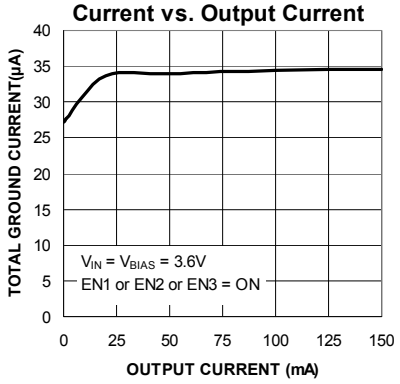


Typical Characteristics (Continued)

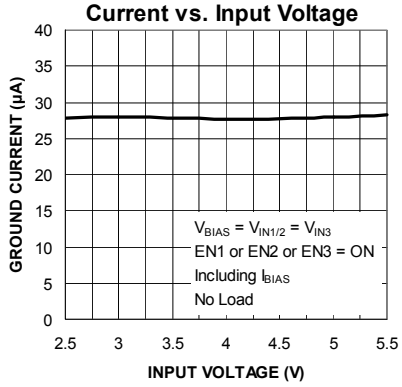
LDO3 Dropout Voltage vs. Temperature



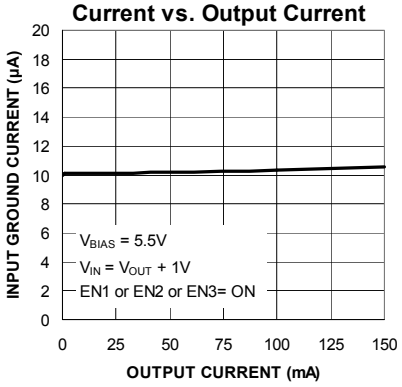
LDO1/2/3 Total Ground Current vs. Output Current



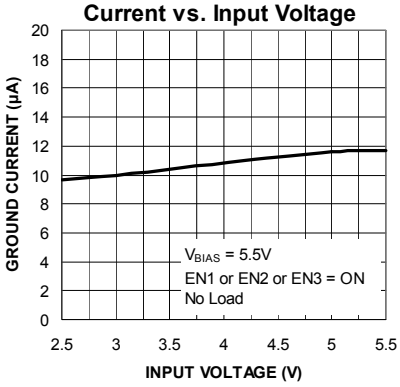
LDO1/2/3 Total Ground Current vs. Input Voltage



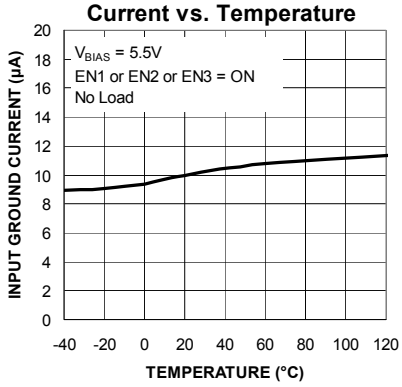
LDO1/2/3 Input Ground Current vs. Output Current



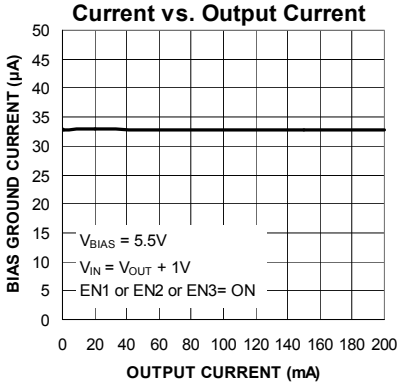
LDO1/2/3 Input Ground Current vs. Input Voltage



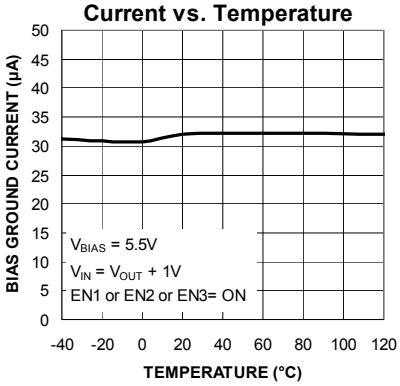
LDO1/2/3 Input Ground Current vs. Temperature



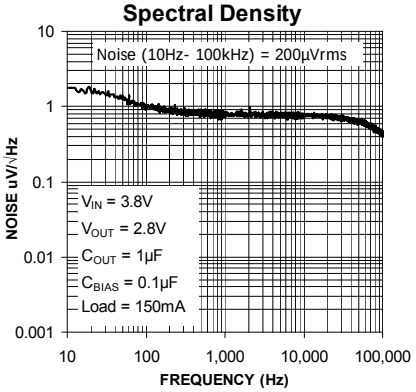
LDO1/2/3 Bias Ground Current vs. Output Current



LDO1/2/3 Bias Ground Current vs. Temperature

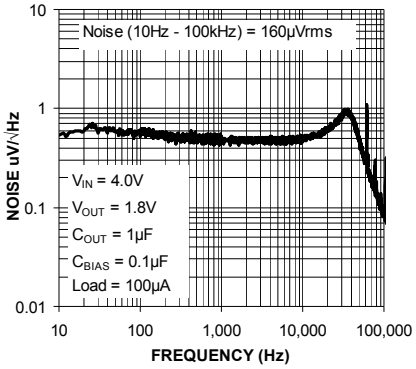


LDO1 Output Noise Spectral Density

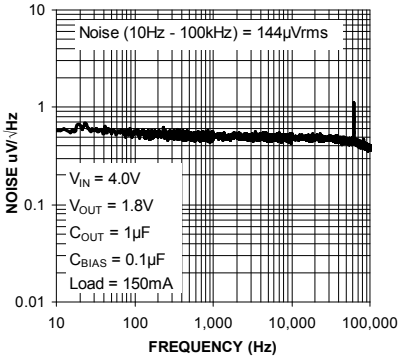


Typical Characteristics (Continued)

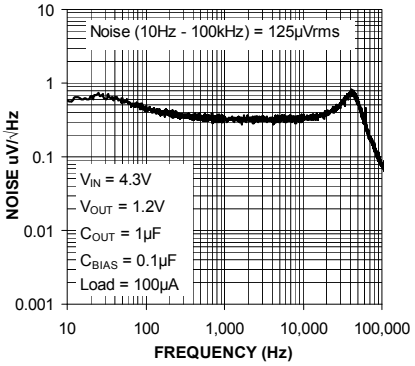
LDO2 Output Noise Spectral Density



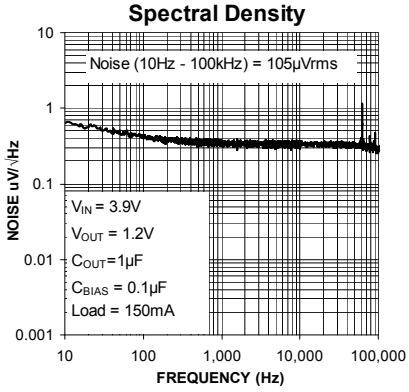
LDO2 Output Noise Spectral Density



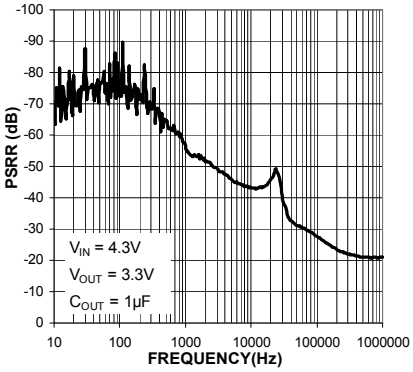
LDO3 Output Noise Spectral Density



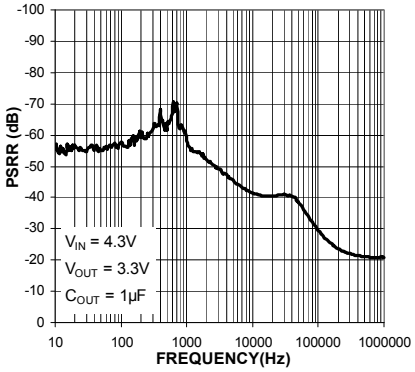
LDO3 Output Noise Spectral Density



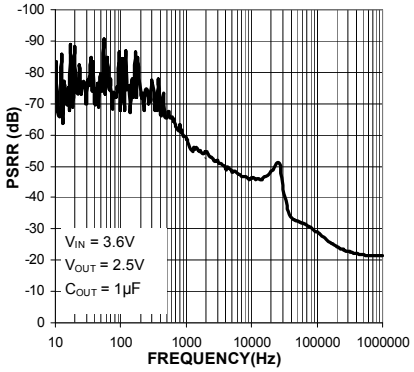
LDO1 PSRR (I_{OUT} = 100µA)



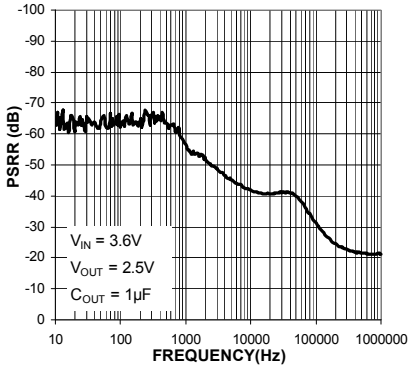
LDO1 PSRR (I_{OUT} = 150mA)



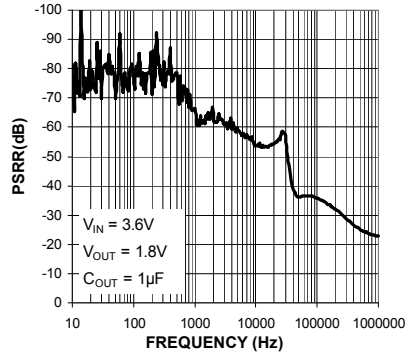
LDO2 PSRR (I_{OUT} = 100µA)



LDO2 PSRR (I_{OUT} = 150mA)

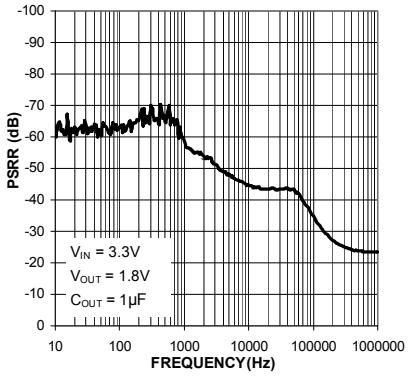


LDO3 PSRR (I_{OUT} = 100µA)



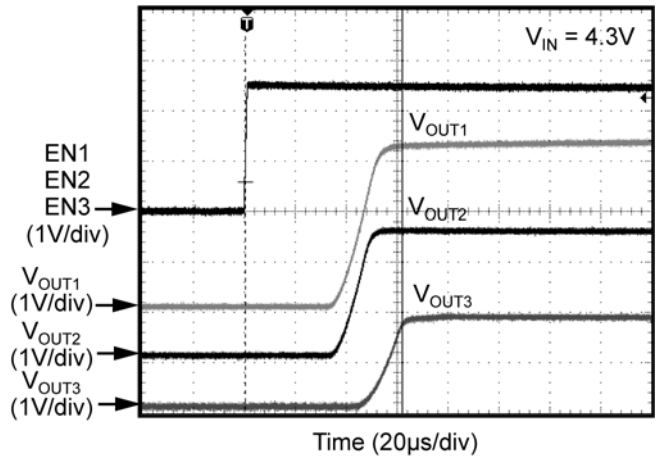
Typical Characteristics (Continued)

LDO3 PSRR (I_{OUT} = 150mA)

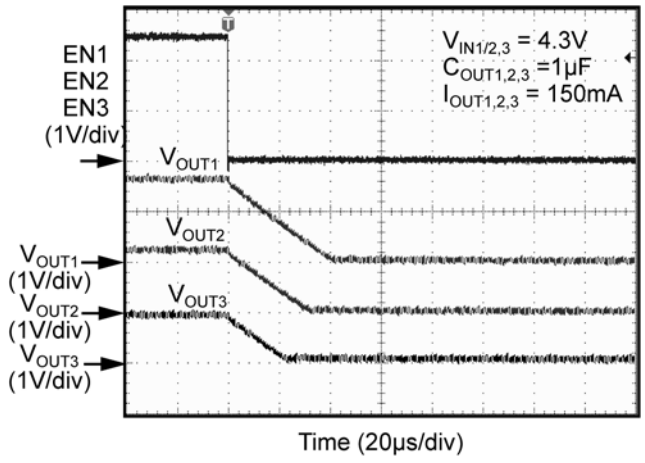


Functional Characteristics

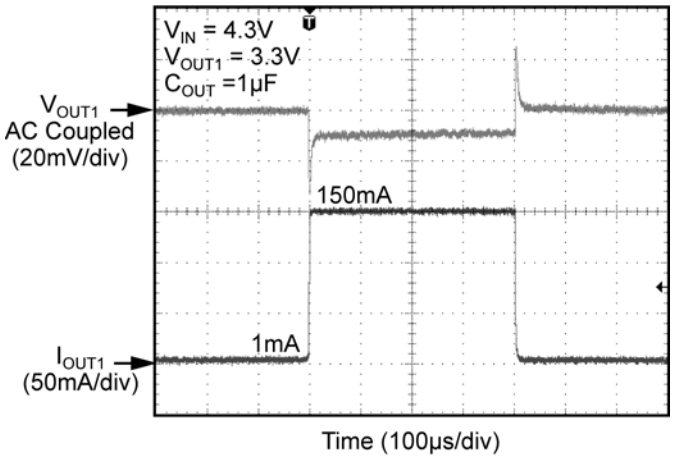
Start-Up Waveform for LDO1/2/3



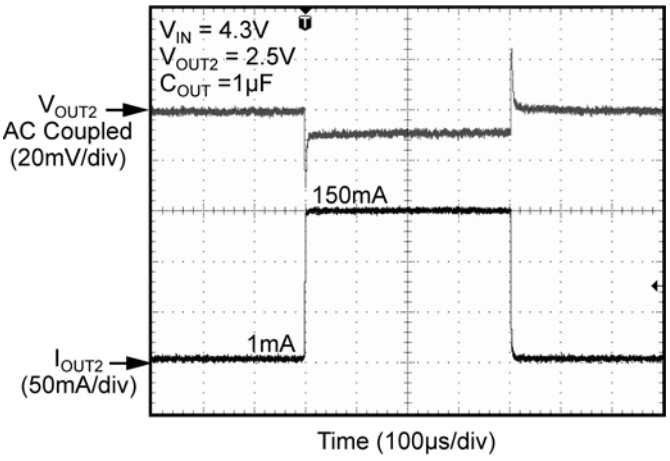
Shutdown Waveform for LDO1/2/3



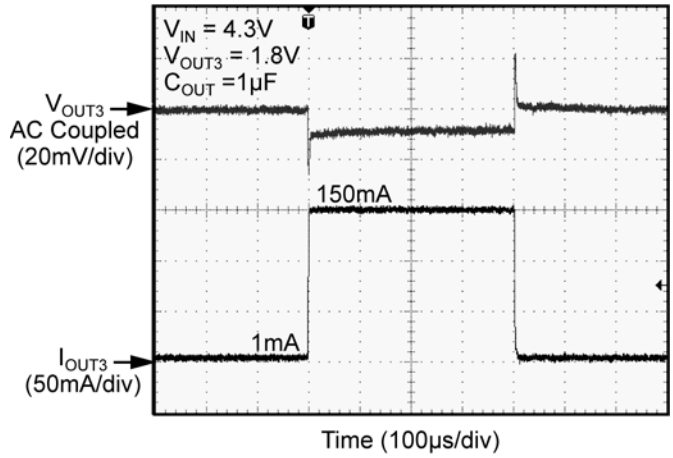
LDO1 Load Transient (1mA to 150mA)



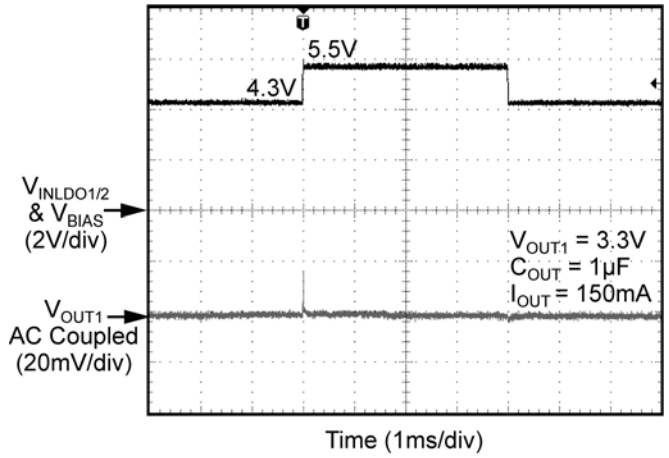
LDO2 Load Transient (1mA to 150mA)



LDO3 Load Transient (1mA to 150mA)

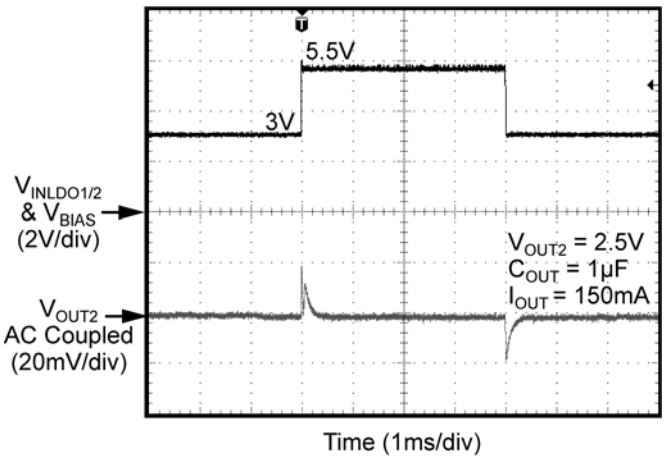


LDO1 Line Transient (4.3V to 5.5V)

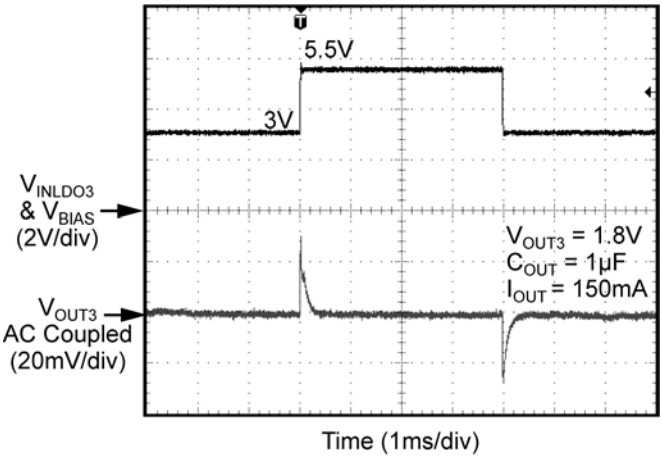


Functional Characteristics (Continued)

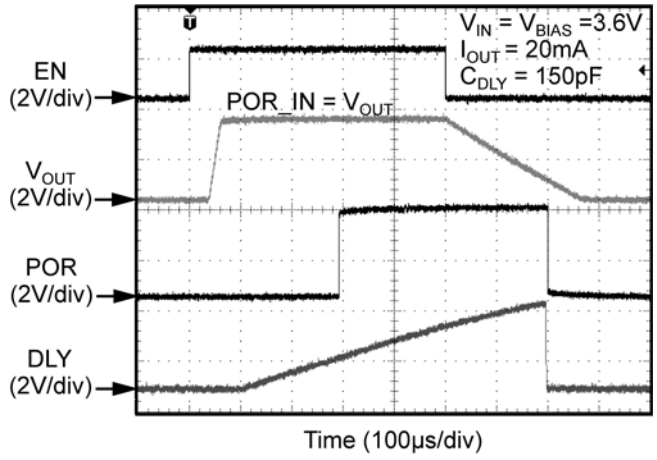
LDO2 Line Transient (3V to 5.5V)



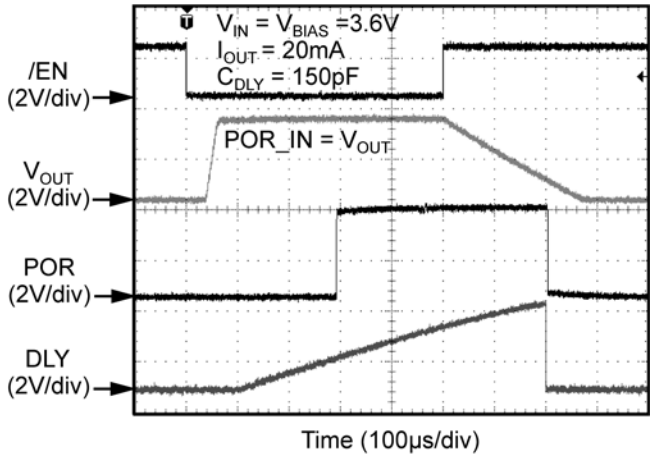
LDO3 Line Transient (3V to 5.5V)



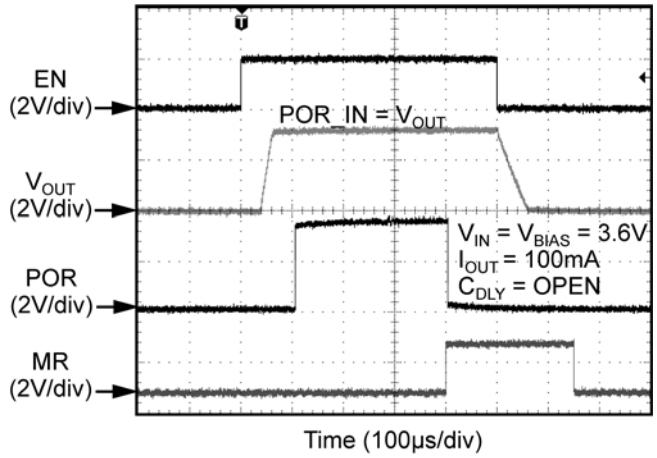
MIC5373 POR with DLY Waveform



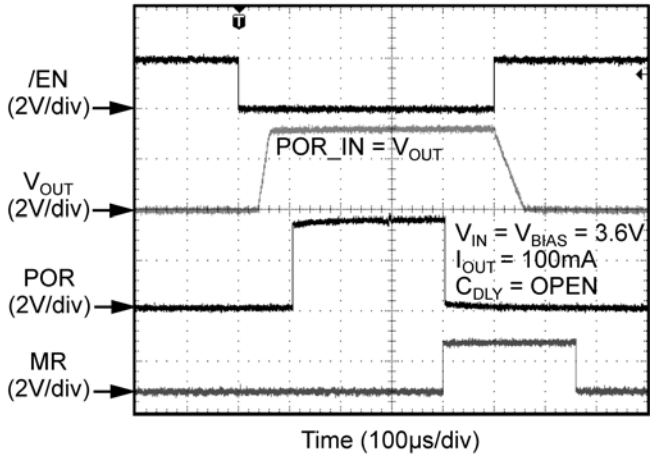
MIC5383 POR with DLY Waveform



MIC5373 POR with MR Waveform

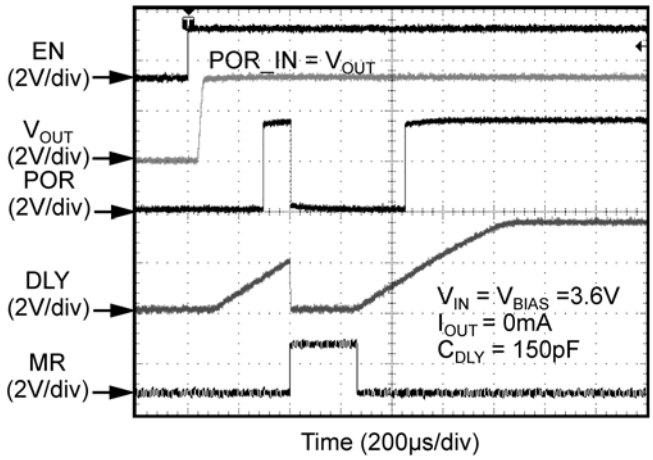


MIC5383 POR with MR Waveform

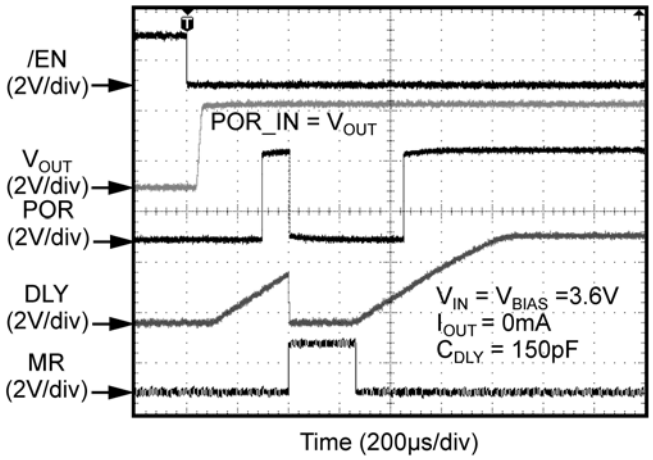


Functional Characteristics (Continued)

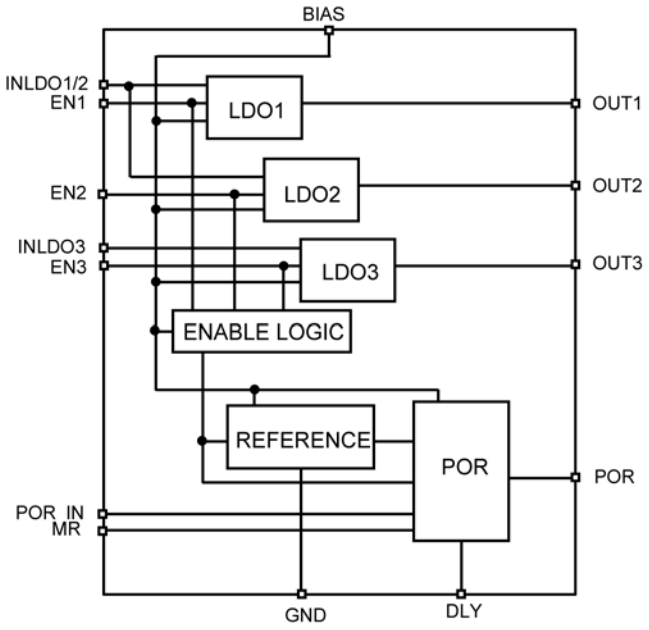
MIC5373 POR with DLY and MR Waveform



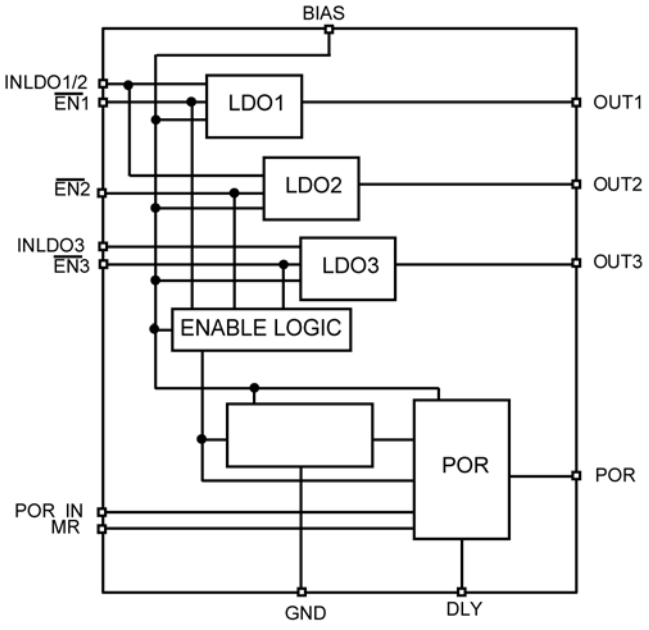
MIC5383 POR with DLY and MR Waveform



Functional Diagram



MIC5373 Block Diagram (Active High Enable)



MIC5383 Block Diagram (Active Low Enable)

Pin Descriptions

INLDO

The LDO input pins INLDO1/2 and INLDO3 provide the input power to the linear regulators LDO1, LDO2 and LDO3. The input operating voltage range is from 1.7V to 5.5V. For input voltages from 1.7V to 2.5V the output current must be limited to 30mA each. Due to line inductance a 1µF capacitor placed close to the INLDO pins and the GND pin is recommended. Please refer to layout recommendations.

BIAS

The BIAS pin provides power to the internal reference and control sections of the MIC5373/83. A 0.1µF ceramic capacitor must be connected from BIAS to GND for clean operation.

EN (MIC5373)

The enable (EN) pins EN1, EN2 and EN3 provide logic level control for the outputs OUT1, OUT2 and OUT3, respectively. A logic high signal on an enable pin activates the respective LDO. A logic low signal on an enable pin deactivates the respective LDO. Do not leave the EN pins floating, as it would leave the regulator in an unknown state.

/EN (MIC5383)

The enable (EN) pins /EN1, /EN2 and /EN3 provide logic level control for the outputs OUT1, OUT2 and OUT3, respectively. A logic high signal on an enable pin deactivates the respective LDO. A logic low signal on an enable pin activates the respective LDO. Do not leave the EN pins floating, as it would leave the regulator in an unknown state.

OUT

OUT1, OUT2 and OUT3 are the output pins of each LDO. A minimum of 1µF capacitor be placed as close as possible to each of the OUT pins. A minimum voltage rating of 6.3V is recommended for each capacitor.

GND

The ground (GND) pin is the ground path for the control circuitry and the power ground for all LDOs. The current loop for the ground should be kept as short as possible. Refer to the layout recommendations for more details.

POR

The power-on-reset (POR) pin is an open drain output. A resistor (10kΩ to 100kΩ) can be used for a pull up to either the input or the output voltage of the regulator. POR is asserted high when the voltage at DLY reaches 1.25V.

A delay can be added by placing a capacitor from the DLY pin to ground.

POR_IN

The power-on-reset input (POR_IN) pin compares any voltage to an internal 0.9V reference. This function can be used to monitor any of the LDO outputs or any external voltage rail. When the monitored voltage is greater than 0.9V, the POR_IN flag will internally trigger a 1.25µA source current to charge the external capacitor at the DLY pin. A resistor divider network may be used to divide down the monitored voltage to be compared with the 0.9V at the POR_IN. This resistor network can change the trigger point to any voltage level. A small decoupling capacitor is recommended between POR_IN and ground to reject high frequency noise that might interfere with the POR circuit. Do not leave the POR_IN pin floating.

DLY

The delay (DLY) pin is used to set the POR delay time. Adding a capacitor to this pin adjusts the delay of the POR signal. When the POR_IN flag is triggered, a constant 1.25µA current begins to charge the external capacitor tied to the DLY pin. When the capacitor reaches 1.25V the POR will be pulled high by the external pull up resistor. Equation 1 illustrates how to calculate the charge time is shown:

$$t_{DELAY}\ (s) = \left(\frac{1.25V \times C_{DLY}}{1.25x10^{-6}} \right) \qquad \text{Eq. 1}$$

The delay time (t) is in seconds, the delay voltage is 1.25V internally, and the external delay capacitance (C_{DLY}) is in microfarads. For a 1µF delay capacitor, the delay time will be 1 second. A capacitor at the DLY pin is recommended when the POR function is used in order to prevent unexpected triggering of the POR signal in noisy systems.

MR

The manual reset (MR) pin resets the output of POR and DLY generator regardless if the monitored voltage is in regulation or not. Applying a voltage greater than 1.2V on the MR pin will cause the POR voltage to be pulled low. When a voltage below 0.2V is applied to the MR pin, the internal 1.25µA will begin to charge the DLY pin until it reaches 1.25V. When the DLY pin reaches 1.25V, the POR voltage will be pulled high by the pull up external resistor again. Do not leave the MR pin floating.

Application Information

MIC5373/83 is a triple output device with three 200mA LDOs. The MIC5373/83 incorporates a POR function with the capability to monitor any voltage using POR_IN. The monitored voltage can be set to any voltage threshold level to trigger the POR flag. A delay on the POR flag may also be set with an external capacitor at the DLY pin. All the LDOs have current limit and thermal shutdown protection to prevent damage from fault conditions. MIC5373 has active high enables while the MIC5383 has active low enables.

Input Capacitor

The MIC5373/83 is a high-performance, high-bandwidth device. An input capacitor of 1µF from the input pin to ground is required to provide stability. Low-ESR ceramic capacitors provide optimal performance in small board area. Additional high-frequency capacitors, such as small valued NPO dielectric type capacitors, help filter out high-frequency noise and are good practice in any RF-based circuit. X5R or X7R dielectrics are recommended for the input capacitor. Y5V dielectrics lose most of their capacitance over temperature and are therefore not recommended.

Output Capacitor

The MIC5373/83 requires an output capacitor of 1µF or greater to maintain stability. The design is optimized for use with low-ESR ceramic chip capacitors. High-ESR capacitors may cause high-frequency oscillation. The output capacitor can be increased, but performance has been optimized for a 1µF ceramic output capacitor and does not improve significantly with larger capacitance.

X7R and X5R dielectric ceramic capacitors are recommended because of their temperature performance. X7R capacitors change capacitance by 15% over their operating temperature range and are the most stable type of ceramic capacitors. Z5U and Y5V dielectric capacitors change value by as much as 50% and 60% respectively over their operating temperature ranges. To use a ceramic chip capacitor with Y5V dielectric the value must be much higher than an X7R ceramic capacitor to ensure the same minimum capacitance over the equivalent operating temperature range.

No Load Stability

Unlike many other voltage regulators, the MIC5373/83 will remain stable and in regulation with no load.

Thermal Considerations

The MIC5373/83 is designed to provide three outputs up to 200mA each of continuous current in a very small package. Maximum ambient operating temperature can be calculated based on the output current and the voltage drop across the part. For example if the input voltages are 3.6V and the output voltages are 3.3V, 2.5V, and 1.8V each with an output current = 150mA. The actual power dissipation of the regulator circuit can be determined using Equation 2:

$$P_D = (V_{INLDO1/2} - V_{OUT1})\, I_{OUT1} + (V_{INLDO1/2} - V_{OUT2})\, I_{OUT2} + (V_{INLDO3} - V_{OUT3})\, I_{OUT3} + V_{IN} \times I_{GND} \quad \text{Eq. 2}$$

As the MIC5373/83 is a CMOS device, the ground current is typically <100µA over the load range, the power dissipation contributed by the ground current is <1% and may be ignored for this calculation, as illustrated in Equation 3:

$$P_D \approx (3.6V - 2.8V)150mA + (3.6V - 1.8V)150mA + (3.6V - 1.2V)150mA$$

$$P_D \approx 0.75W \quad \text{Eq. 3}$$

To determine the maximum ambient operating temperature of the package, use the junction to ambient thermal resistance of the device and Equation 4:

$$P_{D(MAX)} = \left(\frac{T_{J(MAX)} - T_A}{\theta_{JA}} \right) \quad \text{Eq. 4}$$

$T_{J(MAX)} = 125°C$

$\theta_{JA} = 100°C/W$

Substituting P_D for $P_{D(max)}$ and solving for the ambient operating temperature will give the maximum operating conditions for the regulator circuit.

The maximum power dissipation must not be exceeded for proper operation.

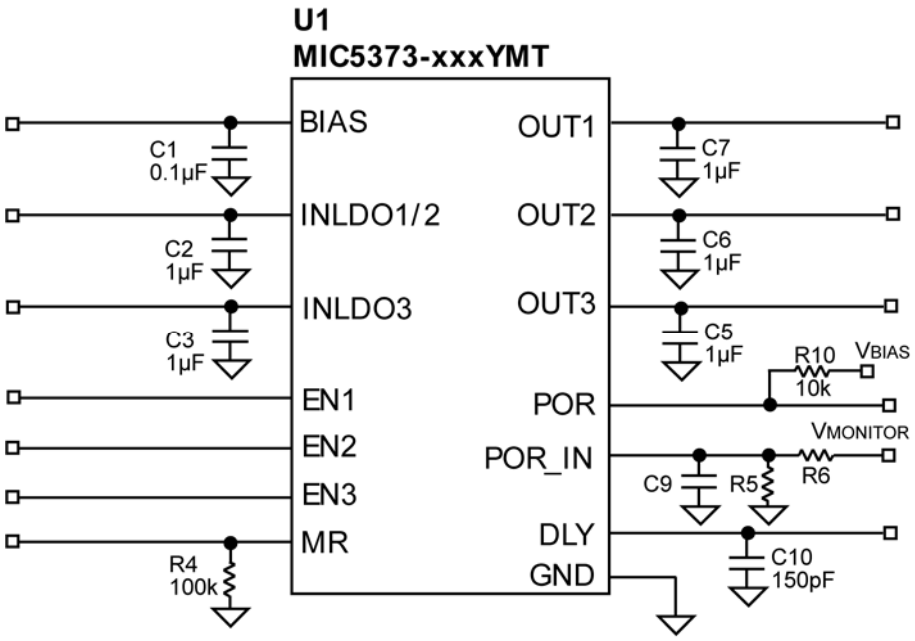
For example, when operating the MIC5373-MG4YMT at an input voltage of 3.6V and 150mA load on LDO1, LDO2 and LDO3 with a minimum layout footprint, the maximum ambient operating temperature T_A can be determined as illustrated Equation 5:

$$0.75W = (125°C – T_A) / (100°C/W)$$
$$T_A = 50°C \quad \text{Eq. 5}$$

Therefore the maximum ambient operating temperature of 50°C is allowed in a 2.5mm x 2.5mm Thin MLF package for the voltage options specified and at the maximum load of 150mA on each output. For a full discussion of heat sinking and thermal effects on voltage regulators, refer to the “Regulator Thermals” section of *Micrel’s Designing with Low-Dropout Voltage Regulators* handbook. This information can be found on Micrel's website at:

http://www.micrel.com/_PDF/other/LDOBk_ds.pdf

Typical Circuit (MIC5373-xxxYMT)



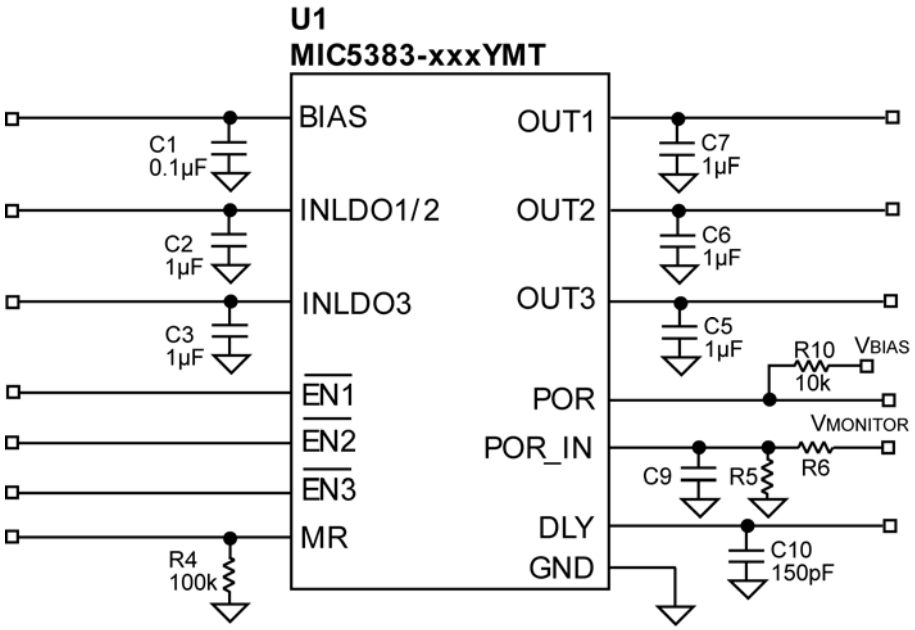
Bill of Materials

Item	Part Number	Manufacturer	Description	Qty.
C1	C1005X5R1A104K	TDK[1]	Capacitor, 0.1µF Ceramic, 10V, X5R, Size 0402	1
C2,C3, C5, C6, C7	C1005X5R1A105K	TDK	Capacitor, 1µF Ceramic, 10V, X5R, Size 0402	5
C9	Optional			1
C10	C1005C0G1H151J	TDK	Capacitor, 150pF Cermaic, 50V, C0G, Size 0402	1
R4	CRCW0402100KFKED	Vishay[2]	100kΩ, 1%, 0402	1
R5, R6	Optional	Vishay	Optional	2
R10	CRCW040210KFKED	Vishay	10kΩ, 1%, 0402	1
U1	**MIC5373-xxxYMT**	**Micrel, Inc.[3]**	**High-Performance Active-High Enable Triple LDO**	**1**

Notes:

1. TDK: www.tdk.com.
2. Vishay: www.vishay.com.
3. **Micrel, Inc.: www.micrel.com.**

Typical Circuit (MIC5383-xxxYMT)



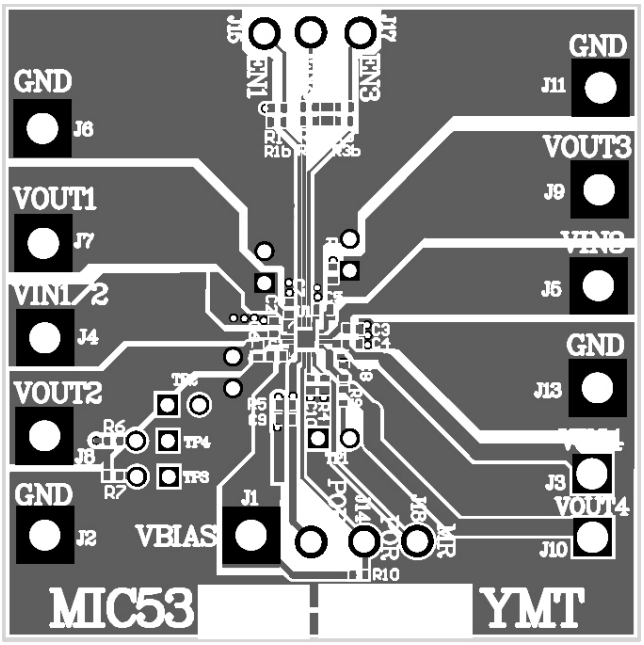
Bill of Materials

Item	Part Number	Manufacturer	Description	Qty.
C1	C1005X5R1A104K	TDK[1]	Capacitor, 0.1µF Ceramic, 10V, X5R, Size 0402	1
C2,C3, C5, C6, C7	C1005X5R1A105K	TDK	Capacitor, 1µF Ceramic, 10V, X5R, Size 0402	5
C9	Optional			1
C10	C1005C0G1H151J	TDK	Capacitor, 150pF Cermaic, 50V, C0G, Size 0402	1
R4	CRCW0402100KFKED	Vishay[2]	100kΩ, 1%, 0402	1
R5, R6	Optional	Vishay	Optional	2
R10	CRCW040210KFKED	Vishay	10kΩ, 1%, 0402	1
U1	**MIC5383-xxxYMT**	**Micrel, Inc.[3]**	**High-Performance Active-Low Enable Triple LDO**	**1**

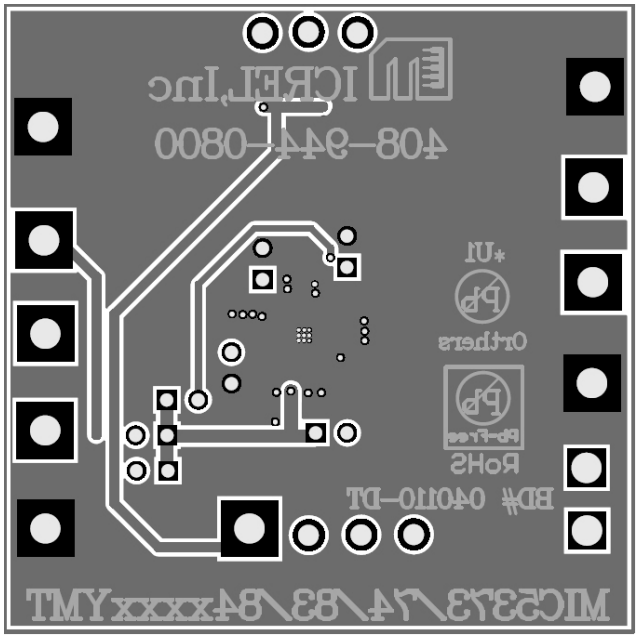
Notes:

1. TDK: www.tdk.com.
2. Vishay: www.vishay.com.
3. **Micrel, Inc.: www.micrel.com.**

PCB Layout Recommendations

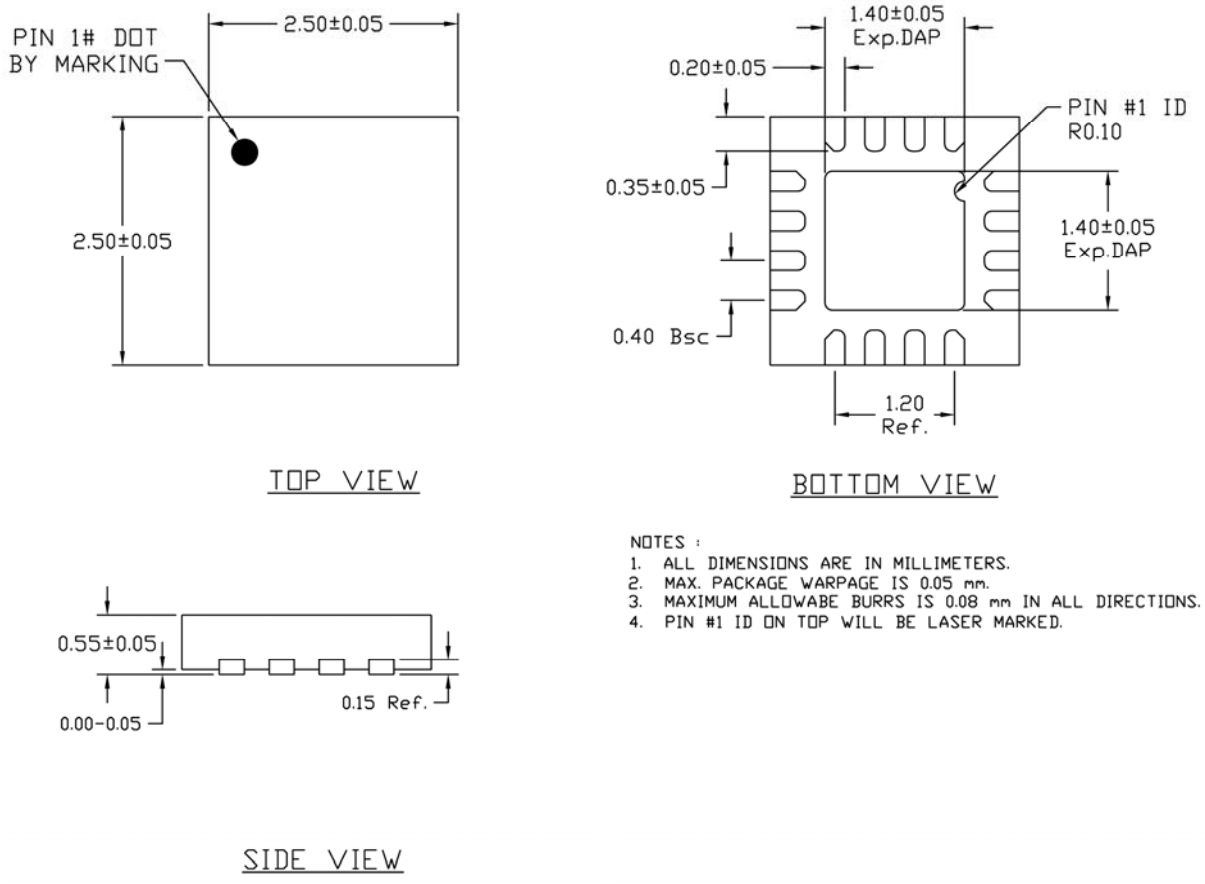


Recommended Top Layout



Recommended Bottom Layout

Package Information



16-Pin 2.5mm x 2.5mm Thin MLF (MT)

MICREL, INC. 2180 FORTUNE DRIVE SAN JOSE, CA 95131 USA
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