Current-Mode PWM Controller for Off-line Power Supplies

NCP1253

The NCP1253 is a highly integrated PWM controller capable of delivering a rugged and high performance offline power supply in a tiny TSOP−6 package. With a supply range up to 28 V, the controller hosts a jittered 65 kHz or 100 kHz switching circuitry operated in peak current mode control. When the power on the secondary side starts to decrease, the controller automatically folds back its switching frequency down to a minimum level of 26 kHz. As the power further goes down, the part enters skip cycle while limiting the peak current. To avoid sub harmonic oscillations in CCM operation, adjustable slope compensation is available via the series inclusion of a simple resistor in the current sense signal.

Besides the auto−recovery timer−based short−circuit protection, an Over Voltage Protection on the V_{CC} pin protects the whole circuitry in case of optocoupler destruction or adverse open loop operation.

Features

- Fixed−Frequency 65 kHz or 100 kHz Current−Mode Control Operation
- Frequency Foldback Down to 26 kHz and Skip−Cycle in Light Load Conditions
- Adjustable Ramp Compensation
- Internally Fixed 4 ms soft−start
- Timer−based Auto−Recovery or Latched Short−Circuit Protection
- Frequency Jittering in Normal and Frequency Foldback Modes
- Latched OVP on V_{CC}
- Up to 28 V V_{CC} Operation
- Extremely Low No−load Standby Power
- These are Pb−Free Devices

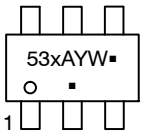
Typical Applications

- Ac−dc Converters for TVs, Set−top Boxes and Printers
- Offline Adapters for Notebooks and Netbooks



TSOP−6
CASE 318G
STYLE 13

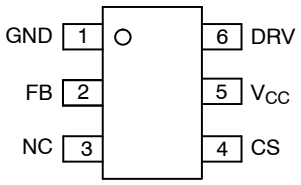
MARKING DIAGRAM



53	= Specific Device Code
x	= A, 2, C, or D
A	= Assembly Location
Y	= Year
W	= Work Week
▪	= Pb−Free Package

(Note: Microdot may be in either location)

PIN CONNECTIONS



(Top View)

ORDERING INFORMATION

See detailed ordering and shipping information on page 2 of this data sheet.

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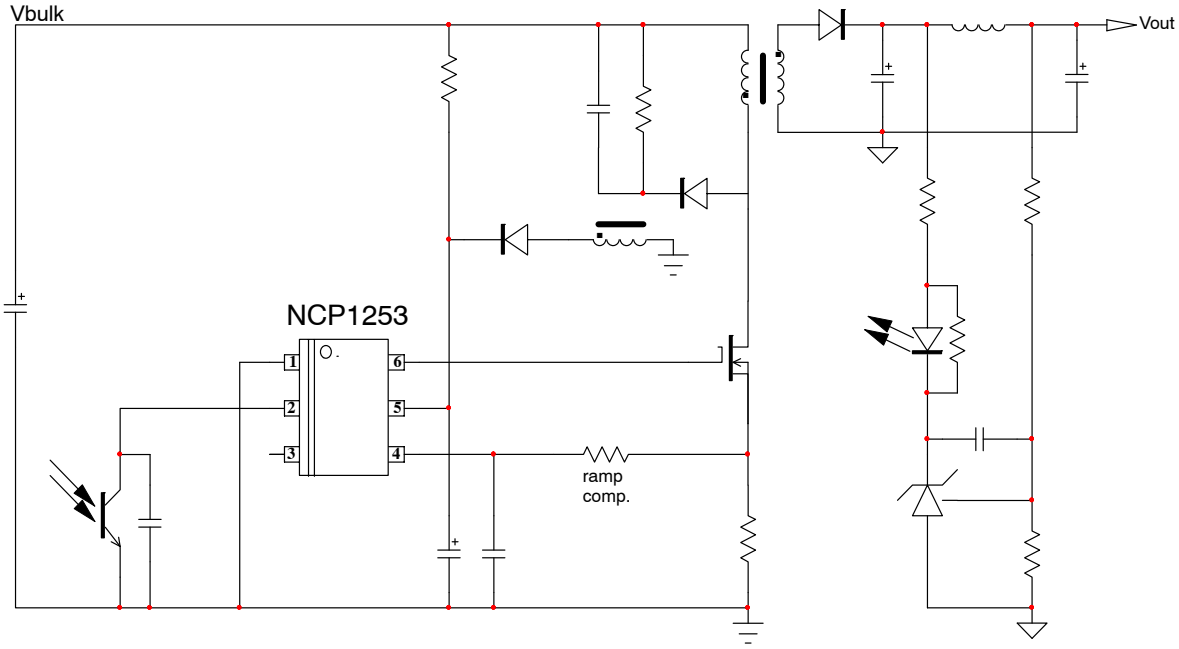

Figure 1. Typical Application Schematic

PIN FUNCTION DESCRIPTION

Pin No.	Pin Name	Function	Description
1	GND	–	The controller ground.
2	FB	Feedback pin	Hooking an optocoupler collector to this pin will allow regulation.
3	NC	Non−connected pin	The pin is electrically inert and can be grounded if necessary
4	CS	Current sense + ramp compensation	This pin monitors the primary peak current but also offers a means to introduce slope compensation.
5	V_{CC}	Supplies the controller – protects the IC	This pin is connected to an external auxiliary voltage. An OVP comparator monitors this pin and offers a means to latch the converter in fault conditions.
6	DRV	Driver output	The driver's output to an external MOSFET gate.

OPTIONS

Controller	Frequency	OCP Latched	OCP Auto−Recovery
NCP1253ASN65T1G	65 kHz	Yes	No
NCP1253BSN65T1G	65 kHz	No	Yes
NCP1253ASN100T1G	100 kHz	Yes	No
NCP1253BSN100T1G	100 kHz	No	Yes

ORDERING INFORMATION

Device	Package Marking	OCP Protection	Switching Frequency (kHz)	Package	Shipping†
NCP1253ASN65T1G	53A	Latch	65	TSOP−6 (Pb−Free)	3000 / Tape & Reel
NCP1253BSN65T1G	532	Auto Recovery	65		
NCP1253ASN100T1G	53C	Latch	100		
NCP1253BSN100T1G	53D	Auto Recovery	100		

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

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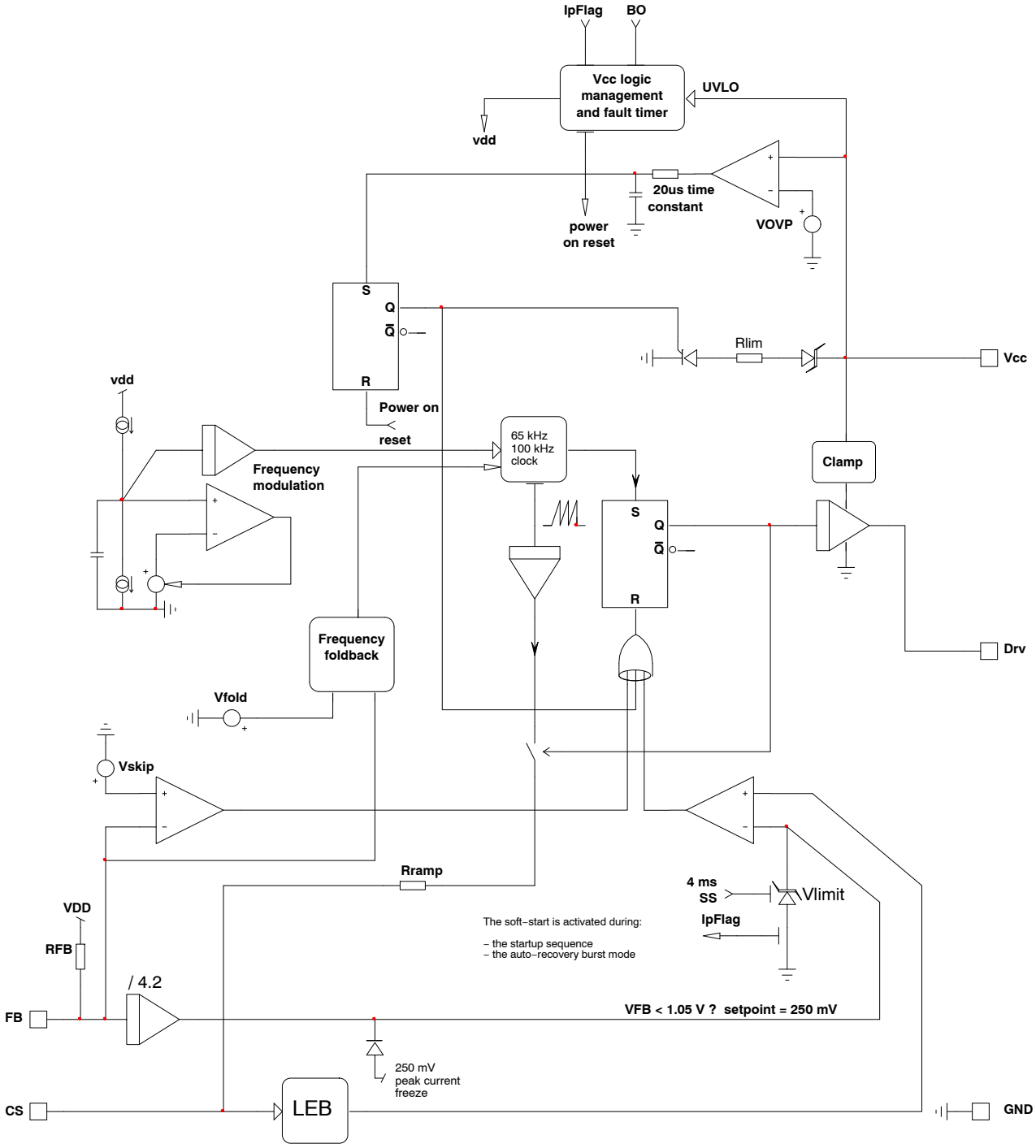

Figure 2. Internal Circuit Architecture

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MAXIMUM RATINGS TABLE

Symbol	Rating	Value	Unit
V_{CC}	Power Supply voltage, V_{cc} pin, continuous voltage	28	V
	Maximum voltage on low power pins CS, and FB	−0.3 to 10	V
$R_{\theta J-A}$	Thermal Resistance Junction−to−Air	360	°C/W
$T_{J,max}$	Maximum Junction Temperature	150	°C
	Storage Temperature Range	−60 to +150	°C
	ESD Capability, Human Body Model, all pins	2	kV
	ESD Capability, Machine Model	200	V

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. This device series contains ESD protection and exceeds the following tests: Human Body Model 2000 V per JESD22, Method A114E. Machine Model Method 200 V per JESD22, Method A115A.
2. This device contains latch−up protection and exceeds 100 mA per JEDEC Standard JESD78.

ELECTRICAL CHARACTERISTICS

(For typical values T_J = 25°C, for min/max values T_J = −40°C to +125°C, Max T_J = 150°C, V_{CC} = 12 V unless otherwise noted)

Symbol	Rating	Pin	Min	Typ	Max	Unit
VCC_{ON}	V_{CC} increasing level at which driving pulses are authorized	5	16	18	20	V
$VCC_{(min)}$	V_{CC} decreasing level at which driving pulses are stopped	5	8.2	8.8	9.4	V
VCC_{HYST}	Hysteresis VCC_{ON}−$VCC_{(min)}$	5	6	–	–	V
V_{ZENER}	Clamped V_{CC} when latched off @ I_{CC} = 500 μA	5	–	7	–	V
ICC1	Start−up current	5	–	–	15	μA
ICC2	Internal IC consumption with I_{FB} = 50 μA, F_{SW} = 65 kHz and C_L = 0	5	–	1.4	2.2	mA
ICC3	Internal IC consumption with I_{FB} = 50 μA, F_{SW} = 65 kHz and C_L = 1 nF	5	–	2.1	3.0	mA
ICC2	Internal IC consumption with I_{FB} = 50 μA, F_{SW} = 100 kHz and C_L = 0	5	–	1.7	2.5	mA
ICC3	Internal IC consumption with I_{FB} = 50 μA, F_{SW} = 100 kHz and C_L = 1 nF	5	–	3.1	4.0	mA
ICCstby	Internal IC consumption while in skip mode (V_{CC} = 12 V, driving a typical 6 A/600 V MOSFET)	5		550		μA
ICC_{LATCH}	Current flowing into V_{CC} pin that keeps the controller latched – T_J = 0 to 125°C	5	32			μA
ICC_{LATCH}	Current flowing into V_{CC} pin that keeps the controller latched – T_J = −40°C to 125°C	5	40			μA
DRIVE OUTPUT						
T_r	Output voltage rise−time @ C_L = 1 nF, 10−90% of output signal	6	–	40	–	ns
T_f	Output voltage fall−time @ C_L = 1 nF, 10−90% of output signal	6	–	30	–	ns
R_{OH}	Source resistance	6	–	13	–	Ω
R_{OL}	Sink resistance	6	–	6	–	Ω
I_{source}	Peak source current, V_{GS} = 0 V (Note 3)	6		300		mA
I_{sink}	Peak sink current, V_{GS} = 12 V (Note 3)	6		500		mA
V_{DRVlow}	DRV pin level at V_{CC} close to $VCC_{(min)}$ with a 33 kΩ resistor to GND	6	8	–	–	V
$V_{DRVhigh}$	DRV pin level at V_{CC}= 28 V – DRV unloaded	6	10	12	14	V

3. Guaranteed by design

CURRENT COMPARATOR						
I_{IB}	Input Bias Current @ 0.8 V input level on pin 4	4		0.02		μA
V_{Limit1}	Maximum internal current setpoint – T_J = 25 °C	4	0.744	0.8	0.856	V
V_{Limit2}	Maximum internal current setpoint – T_J = −40° to 125 °C	4	0.72	0.8	0.88	V

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ELECTRICAL CHARACTERISTICS

(For typical values T_J = 25°C, for min/max values T_J = −40°C to +125°C, Max T_J = 150°C, V_{CC} = 12 V unless otherwise noted)

Symbol	Rating	Pin	Min	Typ	Max	Unit
CURRENT COMPARATOR						
V_{fold}	Default internal voltage set point for frequency foldback trip point − 45% of V_{limit}	4		357		mV
V_{freeze}	Internal peak current setpoint freeze (≈31% of V_{limit})	4		250		mV
T_{DEL}	Propagation delay from current detection to gate off−state	4		100	150	ns
T_{LEB}	Leading Edge Blanking Duration	4		300		ns
TSS	Internal soft−start duration activated upon startup, auto−recovery	−		4		ms
INTERNAL OSCILLATOR						
f_{OSC}	Oscillation frequency (65 kHz version)	−	61	65	71	kHz
f_{OSC}	Oscillation frequency (100 kHz version)	−	92	100	108	kHz
D_{max}	Maximum duty−ratio	−	76	80	84	%
f_{jitter}	Frequency jittering in percentage of f_{OSC}	−		±5		%
f_{swing}	Swing frequency	−		240		Hz
Feedback Section						
R_{up}	Internal pull−up resistor	2		20		kΩ
R_{eq}	Equivalent ac resistor from FB to GND	2		16		kΩ
I_{ratio}	Pin 2 to current setpoint division ratio	−		4.2		
V_{freeze}(FB)	Feedback voltage below which the peak current is frozen	2		1.05		V
FREQUENCY FOLDBACK						
V_{fold}	Frequency foldback level on the feedback pin − ≈45% of maximum peak current	−		1.5		V
F_{trans}	Transition frequency below which skip−cycle occurs	−	22	26	30	kHz
$V_{fold,end}$	End of frequency foldback feedback level, F_{sw} = F_{min}			350		mV
V_{skip}	Skip−cycle level voltage on the feedback pin	−		300		mV
Skip hysteresis	Hysteresis on the skip comparator	−		30		mV
INTERNAL SLOPE COMPENSATION						
V_{ramp}	Internal ramp level @ 25°C (Note 4)	4		2.5		V
R_{ramp}	Internal ramp resistance to CS pin	4		20		kΩ

4. A 1 MΩ resistor is connected from pin 4 to the ground for the measurement.

PROTECTIONS						
V_{OVP}	Latched Overvoltage Protection on the V_{CC} rail	5	24	25.5	27	V
T_{OVPdel}	Delay before OVP confirmation on the V_{CC} rail	5		20		µs
Timer	Internal auto−recovery fault timer duration	−	100	130	160	ms

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

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TYPICAL CHARACTERISTICS

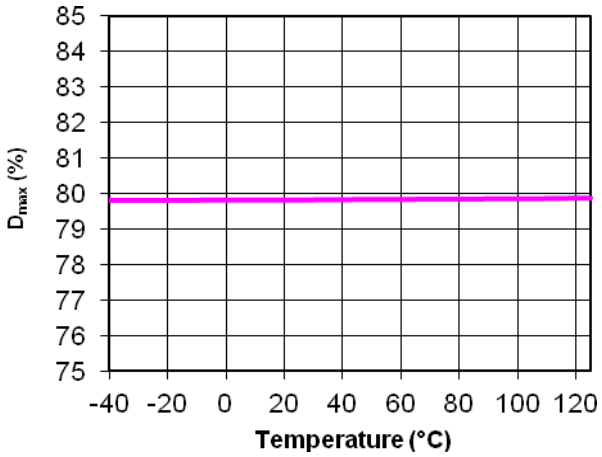

Figure 3. D_{max} vs. Junction Temperature

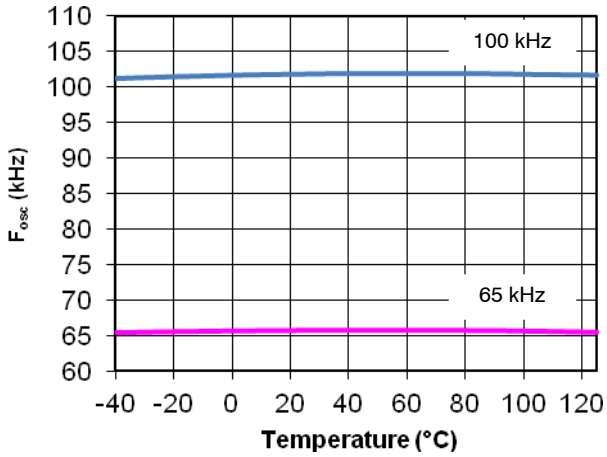

Figure 4. F_{osc} vs. Junction Temperature

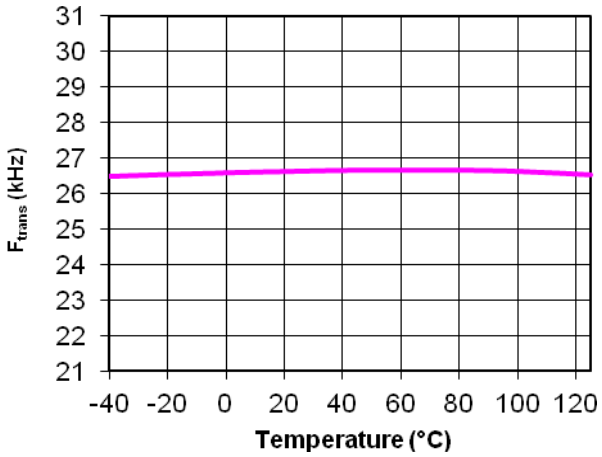

Figure 5. F_{trans} vs. Junction Temperature

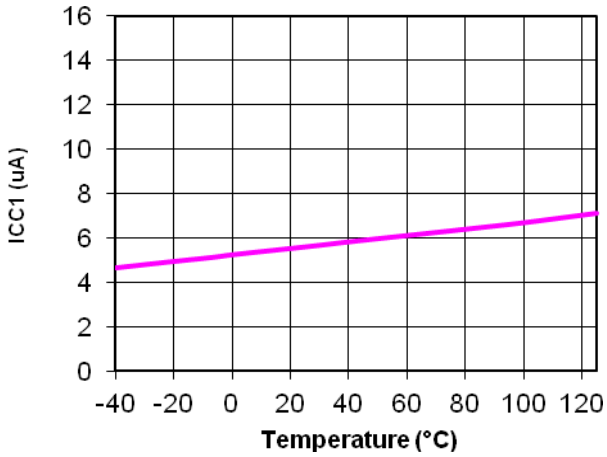

Figure 6. ICC1 vs. Junction Temperature

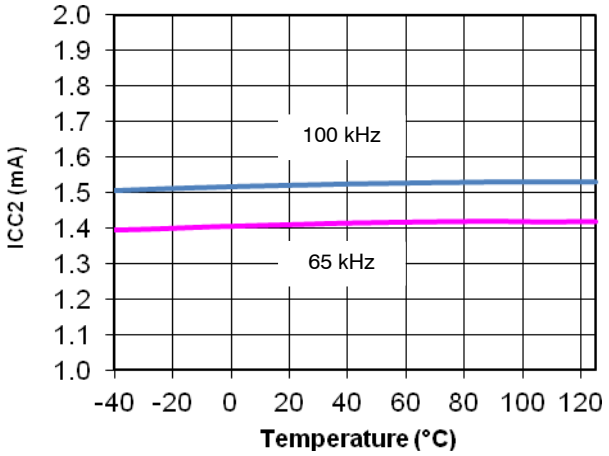

Figure 7. ICC2 vs. Junction Temperature

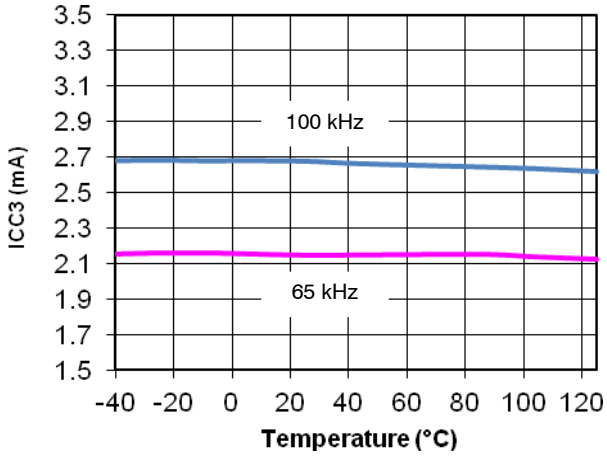

Figure 8. ICC3 vs. Junction Temperature

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TYPICAL CHARACTERISTICS

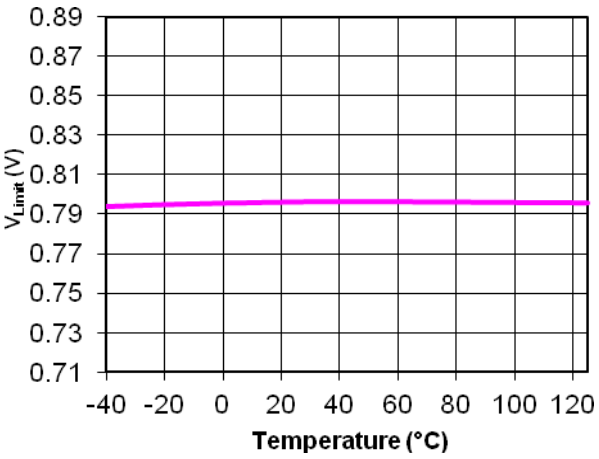

Figure 9. V_{Limit} vs. Junction Temperature

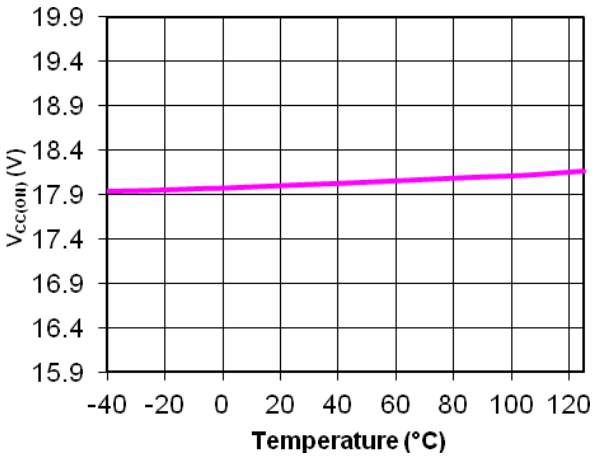

Figure 10. $V_{CC(ON)}$ vs. Junction Temperature

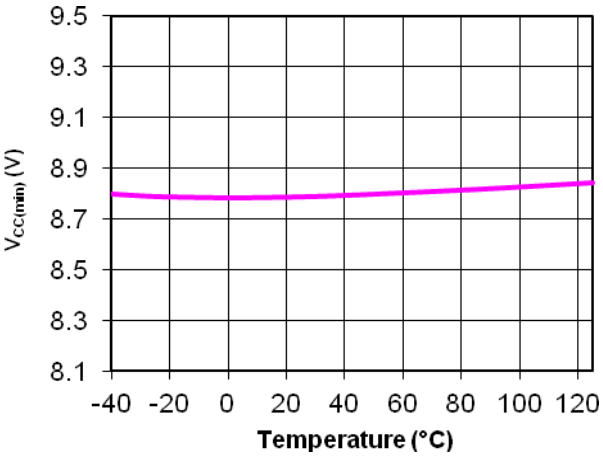

Figure 11. $V_{CC(min)}$ vs. Junction Temperature

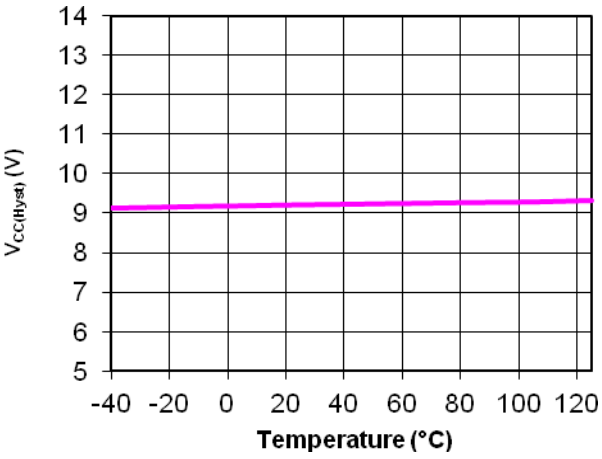

Figure 12. $V_{CC(Hyst)}$ vs. Junction Temperature

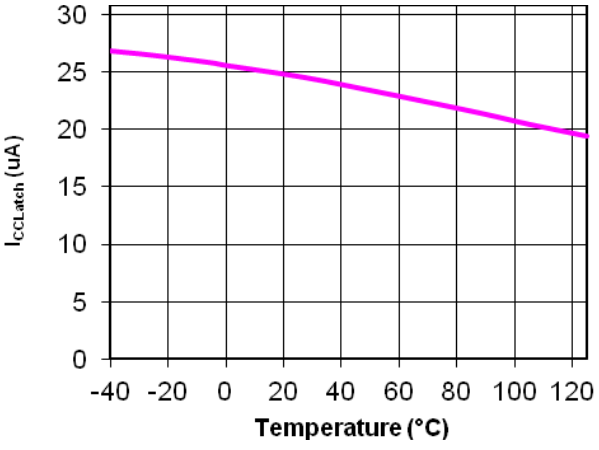

Figure 13. $I_{CCLatch}$ vs. Junction Temperature

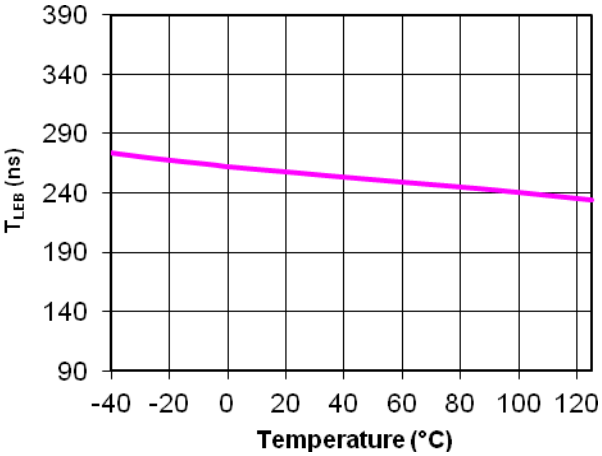

Figure 14. T_{LEB} vs. Junction Temperature

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TYPICAL CHARACTERISTICS

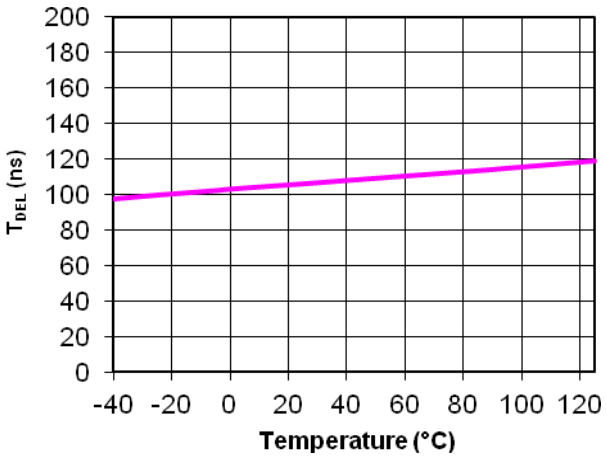

Figure 15. T_{DEL} vs. Junction Temperature

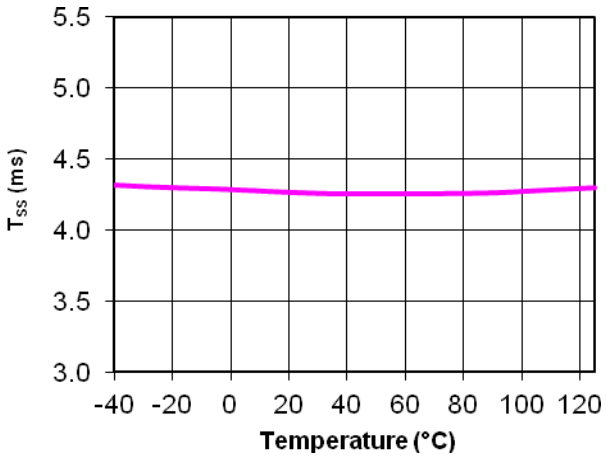

Figure 16. T_{SS} vs. Junction Temperature

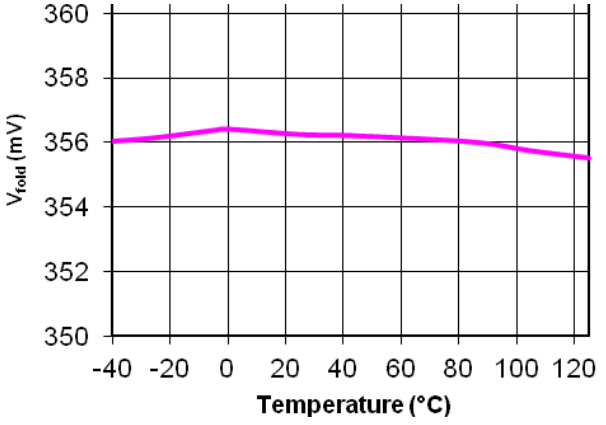

Figure 17. V_{fold} vs. Junction Temperature

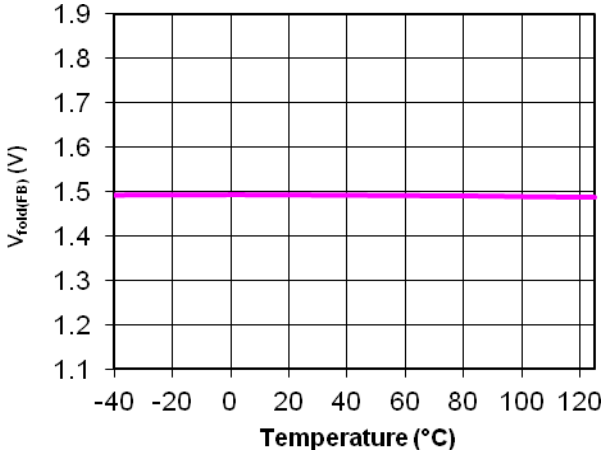

Figure 18. $V_{fold(FB)}$ vs. Junction Temperature

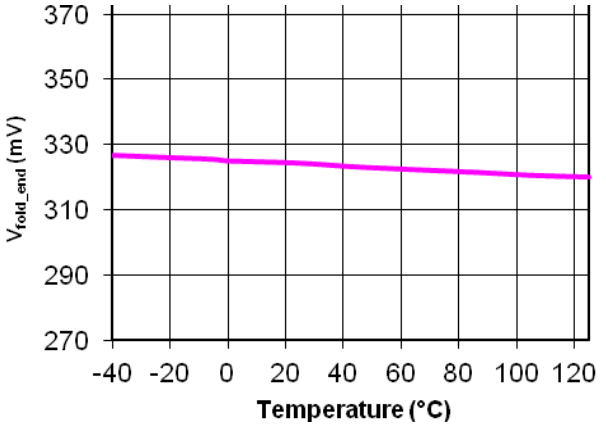

Figure 19. V_{fold_end} vs. Junction Temperature

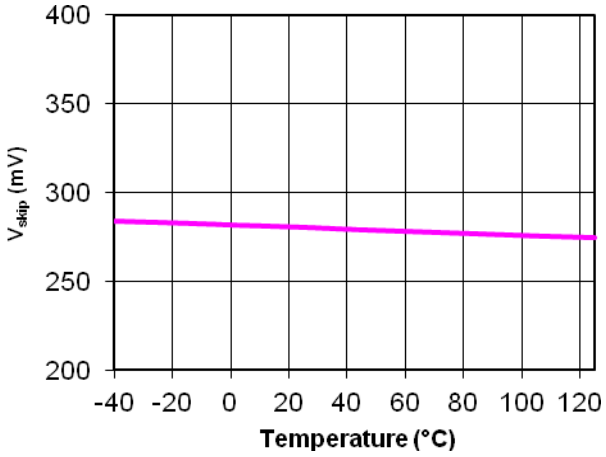

Figure 20. V_{skip} vs. Junction Temperature

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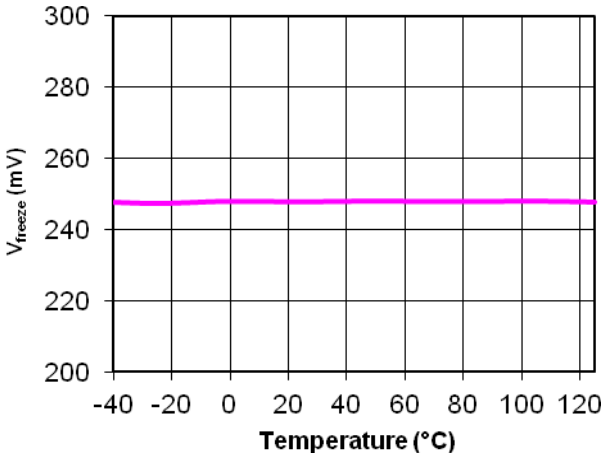

Figure 21. V_{freeze} vs. Junction Temperature

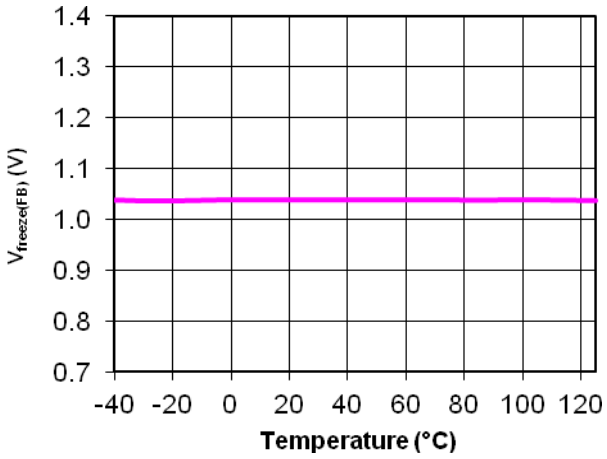

Figure 22. $V_{freeze(FB)}$ vs. Junction Temperature

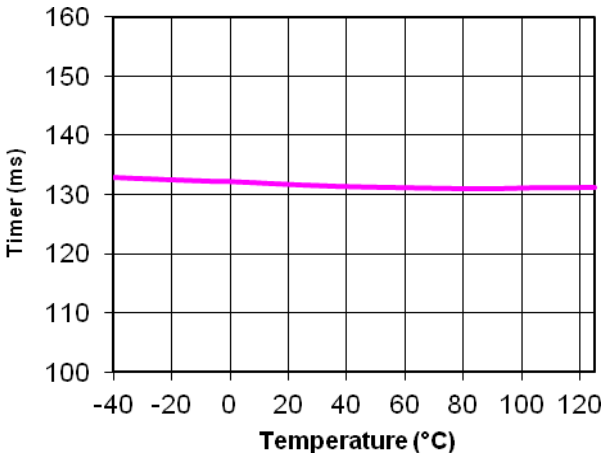

Figure 23. Timer vs. Junction Temperature

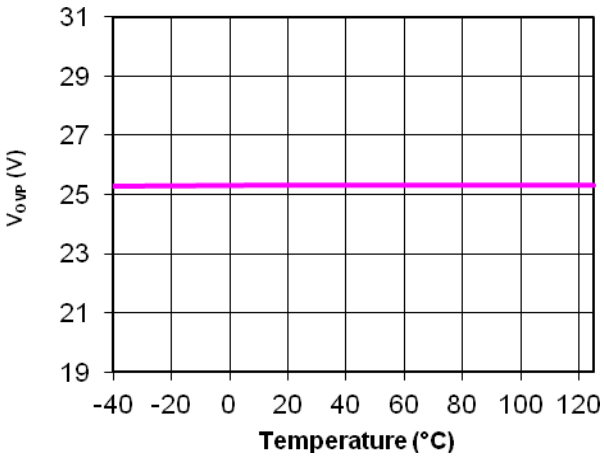

Figure 24. V_{OVP} vs. Junction Temperature

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APPLICATION INFORMATION

Introduction

The NCP1253 implements a standard current mode architecture where the switch−off event is dictated by the peak current setpoint. This component represents the ideal candidate where low part−count and cost effectiveness are the key parameters, particularly in low−cost ac−dc adapters, open−frame power supplies etc. Capitalizing on the NCP1200 series success, the NCP1253 brings all the necessary components normally needed in today modern power supply designs, bringing several enhancements such as a V_{CC} OVP or an adjustable slope compensation signal.

- Current−mode operation with internal ramp compensation: implementing peak current mode control at a fixed 65 kHz or 100 kHz frequency, the NCP1253 offers an internal ramp compensation signal that can easily by summed up to the sensed current. Sub harmonic oscillations can thus be compensated via the inclusion of a simple resistor in series with the current−sense information.
- Low startup current: reaching a low no−load standby power always represents a difficult exercise when the controller draws a significant amount of current during start−up. Thanks to its proprietary architecture, the NCP1253 is guaranteed to draw less than 15 μA maximum, easing the design of low standby power adapters.
- EMI jittering: an internal low−frequency modulation signal varies the pace at which the oscillator frequency is modulated. This helps spreading out energy in conducted noise analysis. To improve the EMI signature at low power levels, the jittering will not be disabled in frequency foldback mode (light load conditions).
- Frequency foldback capability: a continuous flow of pulses is not compatible with no−load/light−load standby power requirements. To excel in this domain, the controller observes the feedback pin and when it reaches a level of 1.5 V, the oscillator then starts to reduce its switching frequency as the feedback level continues to decrease. When the feedback pin reaches 1.05 V, the peak current setpoint is internally frozen and the frequency continues to decrease. It can go down to 26 kHz (typical) reached for a feedback level of 350 mV roughly. At this point, if the power continues to drop, the controller enters classical skip−cycle mode.
- Internal soft−start: a soft−start precludes the main power switch from being stressed upon start−up. In this controller, the soft−start is internally fixed to 4 ms. Soft−start is activated when a new startup sequence occurs or during an auto−recovery hiccup.
- Latched OVP on V_{cc}: it is sometimes interesting to implement a circuit protection by sensing the V_{CC} level. This is what NCP1253 does by monitoring its V_{CC} pin. When the voltage on this pin exceeds 25.5 V typical, the pulses are immediately stopped and the part latches off. When the user cycles the V_{CC} down or the converter recovers from a brown−out event, the circuit is reset and the part enters a new start−up sequence.
- Short−circuit protection: short−circuit and especially over−load protections are difficult to implement when a strong leakage inductance between auxiliary and power windings affects the transformer (the aux winding level does not properly collapse in presence of an output short). Here, every time the internal 0.8 V maximum peak current limit is activated, an error flag is asserted and a time period starts, thanks to an internal timer. When the fault is validated, all pulses are stopped and the controller enters an auto−recovery burst mode, with a soft−start sequence at the beginning of each cycle. As soon as the fault disappears, the SMPS resumes operation. Please note that some version offers an auto−recovery mode as we just described, some do not and latch off in case of a short circuit.

Start−up Sequence

The NCP1253 start−up voltage is made purposely high to permit large energy storage in a small V_{CC} capacitor value. This helps to operate with a small start−up current which, together with a small V_{cc} capacitor, will not hamper the start−up time. To further reduce the standby power, the start−up current of the controller is extremely low, below 15 μA. The start−up resistor can therefore be connected to the bulk capacitor or directly to the mains input voltage if you wish to save a few more mW.

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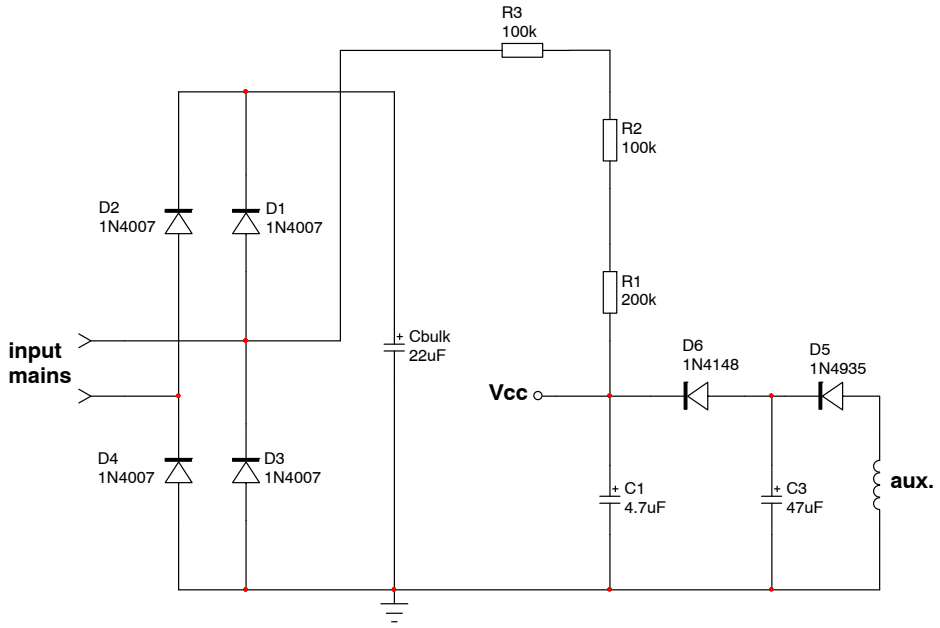

Figure 25. The Startup Resistor Can Be Connected to the Input Mains for Further Power Dissipation Reduction

The first step starts with the calculation of the needed V_{CC} capacitor which will supply the controller until the auxiliary winding takes over. Experience shows that this time t_1 can be between 5 and 20 ms. Considering that we need at least an energy reservoir for a t_1 time of 10 ms, the V_{cc} capacitor must be larger than:

$$CV_{CC} \geq \frac{I_{CC}t_1}{VCC_{on} - VCC_{min}} \geq \frac{3m \times 10m}{9} \geq 3.3\ \mu F \quad \text{(eq. 1)}$$

Let us select a 4.7 µF capacitor at first and experiments in the laboratory will let us know if we were too optimistic for t_1. The V_{CC} capacitor being known, we can now evaluate the charging current we need to bring the V_{cc} voltage from 0 to the VCC_{on} of the IC, 18 V typical. This current has to be selected to ensure a start−up at the lowest mains (85 V rms) to be less than 3 s (2.5 s for design margin):

$$I_{charge} \geq \frac{VCC_{On}C_{VCC}}{2.5} \geq \frac{18 \times 4.7\mu}{2.5} \geq 34\ \mu A \quad \text{(eq. 2)}$$

If we account for the 15 µA that will flow inside the controller, then the total charging current delivered by the start−up resistor must be 49 µA. If we connect the start−up network to the mains (half−wave connection then), we know that the average current flowing into this start−up resistor will be the smallest when V_{CC} reaches the VCC_{on} of the controller:

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$$I_{CVCC,min} = \frac{\frac{V_{ac,rms}\sqrt{2}}{\pi} - VCC_{on}}{R_{start-up}} \quad \text{(eq. 3)}$$

To make sure this current is always greater than 49 µA, the maximum value for $R_{start-up}$ can be extracted:

$$R_{start-up} \leq \frac{\frac{V_{ac,rms}\sqrt{2}}{\pi} - VCC_{on}}{I_{CVCC,min}} \leq \frac{\frac{85 \times 1.414}{\pi} - 18}{49\mu} \leq 413\ k\Omega \quad \text{(eq. 4)}$$

This calculation is purely theoretical, considering a constant charging current. In reality, the take over time can be shorter (or longer!) and it can lead to a reduction of the V_{cc} capacitor. This brings a decrease in the charging current and an increase of the start−up resistor, for the benefit of standby power. Laboratory experiments on the prototype are thus mandatory to fine tune the converter. If we chose the 400k resistor as suggested by Equation 4, the dissipated power at high line amounts to:

$$P_{Rstart,max} = \frac{V_{ac,peak}^{\ 2}}{4R_{start-up}} = \frac{\left(320 \times \sqrt{2}\right)^2}{4 \times 400k} = \frac{105k}{1.6Meg} \quad \text{(eq. 5)}$$

$$= 66\ mW$$

Now that the first V_{CC} capacitor has been selected, we must ensure that the self−supply does not disappear when in no−load conditions. In this mode, the skip−cycle can be so deep that refreshing pulses are likely to be widely spaced, inducing a large ripple on the V_{CC} capacitor. If this ripple is too large, chances exist to touch the VCC_{min} and reset the controller into a new start−up sequence. A solution is to grow this capacitor but it will obviously be detrimental to the start−up time. The option offered in Figure 25 elegantly

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solves this potential issue by adding an extra capacitor on the auxiliary winding. However, this component is separated from the V_{CC} pin via a simple diode. You therefore have the ability to grow this capacitor as you need to ensure the self−supply of the controller without jeopardizing the start−up time and standby power.

Triggering the SCR

The latched−state of the NCP1253 is maintained via an internal thyristor (SCR). When the voltage on the V_{cc} pin exceeds the internal latch voltage, the SCR is fired and immediately stops the output pulses. When this happens, all pulses are stopped and V_{CC} is discharged to a fix level of 7 V typically: the circuit is latched and the converter no longer delivers pulses. To maintain the latched−state, a permanent current must be injected in the part. If too low of a current, the part de−latches and the converter resumes operation. This current is characterized to 32 μA as a minimum but we recommend including a design margin and select a value around 60 μA. The test is to latch the part and reduce the input voltage until it de−latches. If you de−latch at V_{in} = 70 Vrms for a minimum voltage of 85 Vrms, you are fine. If it precociously recovers, you will have to increase the start−up current, unfortunately to the detriment of standby power.

The most sensitive configuration is actually that of the half−wave connection proposed in Figure 25. As the current disappears 5 ms for a 10 ms period (50 Hz input source), the latch can potentially open at low line. If you really reduce the start−up current for a low standby power design, you must ensure enough current in the SCR in case of a faulty event. An alternate connection to the above is shown below (Figure 26):

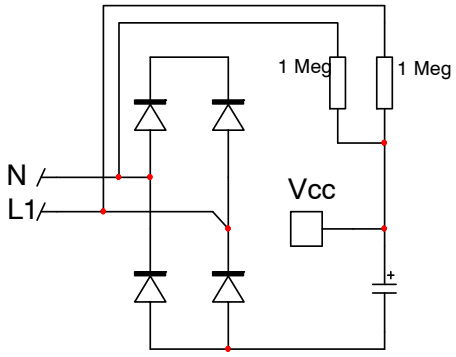

Figure 26. The Full−wave Connection Ensures Latch Current Continuity as well as a X2−Discharge Path.

In this case, the current is no longer made of 5 ms “holes” and the part can be maintained at a low input voltage. Experiments show that these 2 MΩ resistor help to maintain the latch down to less than 50 Vrms, giving an excellent design margin. Standby power with this approach was also improved compared to Figure 25 solution. Please note that these resistors also ensure the discharge of the X2−capacitor up to a 0.47 μF type.

The de−latch of the SCR occurs when the injected current in the V_{CC} pin falls below the minimum stated in the data−sheet (32 μA at room temp).

Frequency Foldback

The reduction of no−load standby power associated with the need for improving the efficiency, requires a change in the traditional fixed−frequency type of operation. This controller implements a switching frequency foldback when the feedback voltage passes below a certain level, V_{fold}, set around 1.5 V. At this point, the oscillator enters frequency foldback and reduces its switching frequency. The peak current setpoint is following the feedback pin until its level reaches 1.05 V. Below this value, the peak current freezes to V_{fold}/4.2 (250 mV or 31% of the maximum 0.8−V setpoint) and the only way to further reduce the transmitted power is to diminish the operating frequency down to 26 kHz. This value is reached at a feedback voltage level of 350 mV typically. Below this point, if the output power continues to decrease, the part enters skip cycle for the best noise−free performance in no−load conditions. depicts the adopted scheme for the part.

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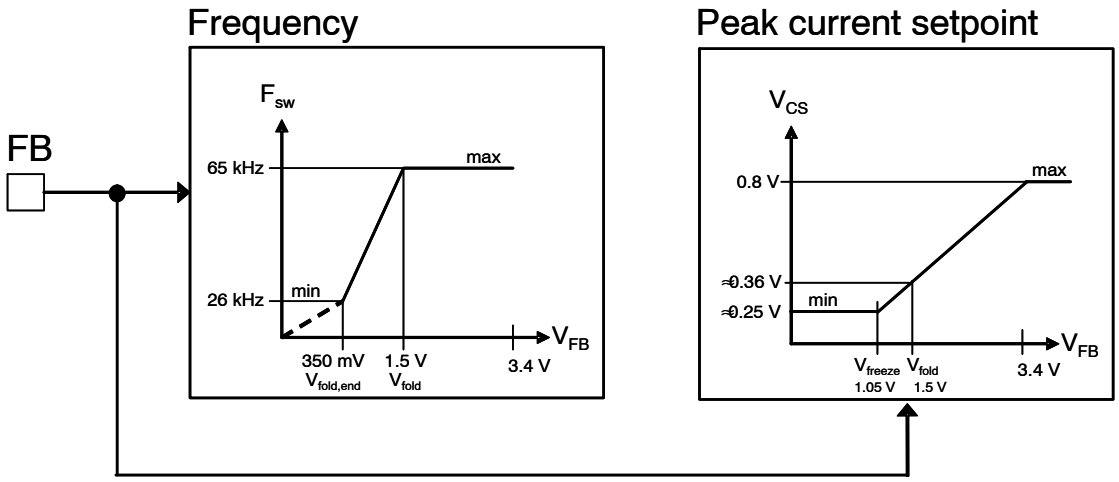

Figure 27. By Observing the Voltage on the Feedback Pin, the Controller Reduces its Switching Frequency for an Improved Performance at Light Load

Auto−recovery Short−Circuit Protection

In case of output short−circuit or if the power supply experiences a severe overloading situation, an internal error flag is raised and starts a countdown timer. If the flag is asserted longer than 100 ms, the driving pulses are stopped and V_{CC} falls down as the auxiliary pulses are missing. When it crosses $VCC_{(min)}$, the controller consumption is down to a few μA and the V_{CC} slowly builds up again thanks to the resistive starting network. When V_{CC} reaches VCC_{ON}, the controller attempts to re−start, checking for the absence of the fault. If the fault is still there, the supply enters another cycle of so−called hiccup. If the fault has disappeared, the power supply resumes operations. Please note that the soft−start is activated during each of the re−start sequence.

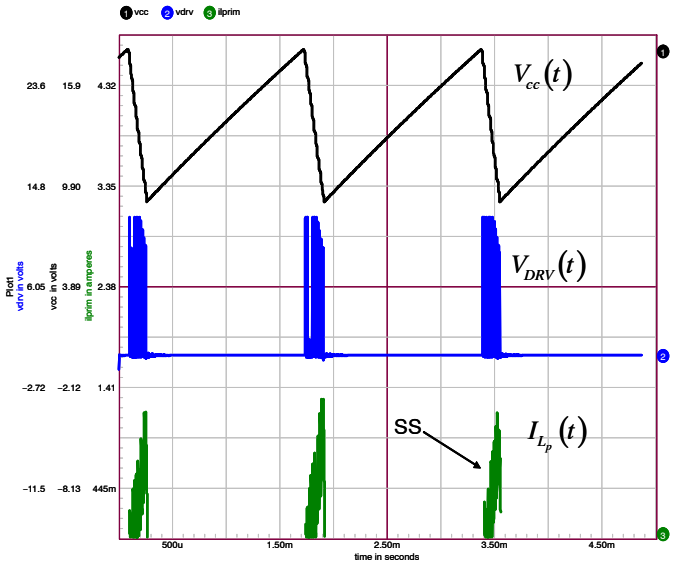

Figure 28. An Auto−Recovery Hiccup Mode is Entered in Case a Faulty Event Longer Than 100 ms is Acknowledged by the Controller

Ramp compensation

The NCP1253 includes an internal ramp compensation signal. This is the buffered oscillator clock delivered during the on time only. Its amplitude is around 2.5 V at the maximum duty−cycle. Ramp compensation is a known means used to cure sub harmonic oscillations in CCM−operated current−mode converters. These oscillations take place at half the switching frequency and occur only during Continuous Conduction Mode (CCM) with a duty−cycle greater than 50%. To lower the current loop gain, one usually injects between 50% and 100% of the inductor downslope.

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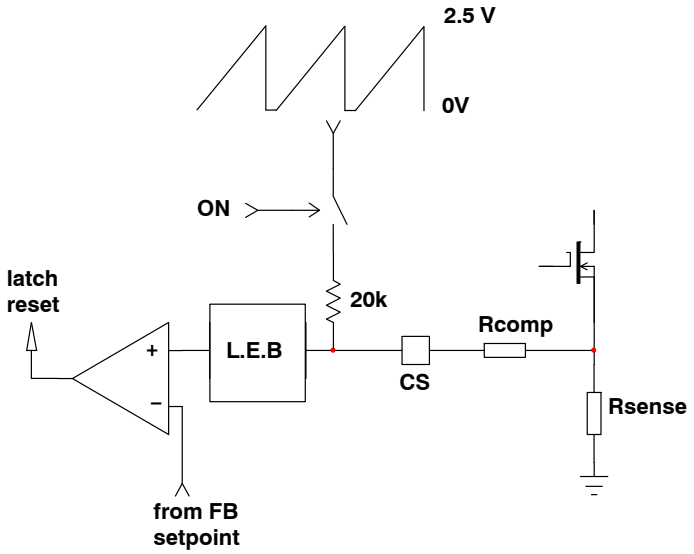

Figure 29. Inserting a Resistor in Series with the Current Sense Information Brings Ramp Compensation and Stabilizes the Converter in CCM Operation

In the NCP1253 controller, the oscillator ramp features a 2.5 V swing. If the clock operates at a 65 kHz frequency, then the available oscillator slope corresponds to:

$$S_{ramp} = \frac{V_{ramp,peak} D_{max}}{T_{SW}} = \frac{2.5 \times 0.8}{15\mu} \quad \text{(eq. 6)}$$

$$= 133\ \text{kV/s or } 133\ \text{mV/}\mu\text{s}$$

In our flyback design, let's assume that our primary inductance L_p is 770 µH, and the SMPS delivers 19 V with a N_p:N_s ratio of 1:0.25. The off−time primary current slope S_p is thus given by:

$$S_P = \frac{(V_{out} + V_f)\frac{N_s}{N_P}}{L_P} = \frac{(19 + 0.8) \times 4}{770\mu} = 103\ \text{kA/s} \quad \text{(eq. 7)}$$

Given a sense resistor of 330 mΩ, the above current ramp turns into a voltage ramp of the following amplitude:

$$S_{sense} = S_P R_{sense} = 103\text{k} \times 0.33 \quad \text{(eq. 8)}$$

$$= 34\ \text{kV/s or } 34\ \text{mV/}\mu\text{s}$$

If we select 50% of the downslope as the required amount of ramp compensation, then we shall inject a ramp whose slope is 17 mV/µs. Our internal compensation being of 133 mV/µs, the divider ratio (*divratio*) between R_{comp} and the internal 20 kΩ resistor is:

$$\text{divratio} = \frac{17\text{m}}{133\text{m}} = 0.127 \quad \text{(eq. 9)}$$

The series compensation resistor value is thus:

$$R_{comp} = R_{ramp}\text{divratio} = 20\text{k} \times 0.127 \approx 2.5\ \text{k}\Omega \quad \text{(eq. 10)}$$

A resistor of the above value will then be inserted from the sense resistor to the current sense pin. We recommend adding a small 100 pF capacitor, from the current sense pin to the controller ground for improved noise immunity. Please make sure both components are located very close to the controller.

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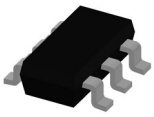

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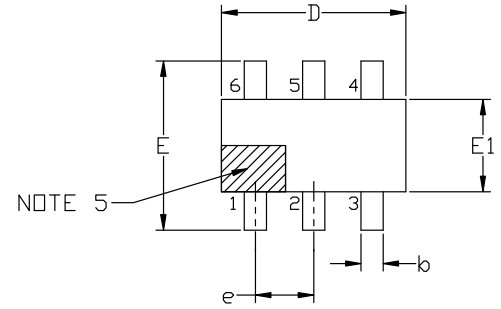
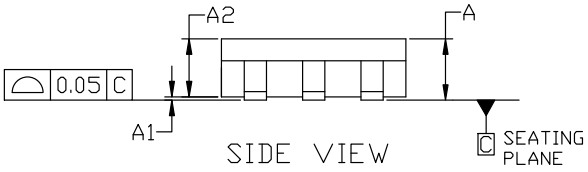
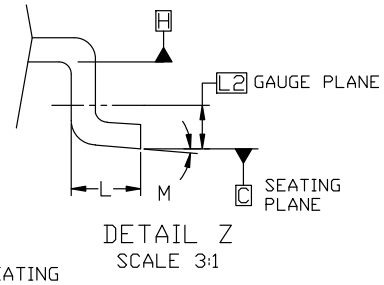
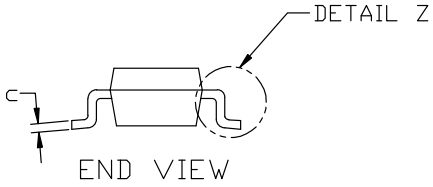


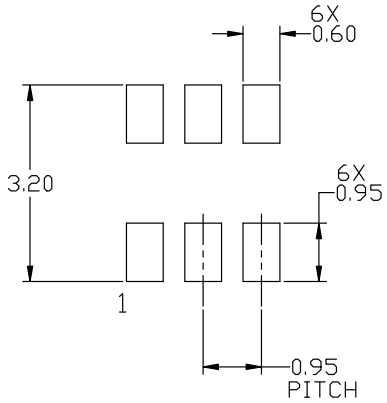






NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 2018.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. MAXIMUM LEAD THICKNESS INCLUDES LEAD FINISH. MINIMUM LEAD THICKNESS IS THE MINIMUM THICKNESS OF BASE MATERIAL.
4. DIMENSIONS D AND E1 DO NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR GATE BURRS. MOLD FLASH, PROTRUSIONS, OR GATE BURRS SHALL NOT EXCEED 0.15 PER SIDE. DIMENSIONS D AND E1 ARE DETERMINED AT DATUM H.
5. PIN 1 INDICATOR MUST BE LOCATED IN THE INDICATED ZONE

MILLIMETERS			
DIM	MIN	NOM	MAX
A	0.90	1.00	1.10
A1	0.01	0.06	0.10
A2	0.80	0.90	1.00
b	0.25	0.38	0.50
c	0.10	0.18	0.26
D	2.90	3.00	3.10
E	2.50	2.75	3.00
E1	1.30	1.50	1.70
e	0.85	0.95	1.05
L	0.20	0.40	0.60
L2	0.25 BSC		
M	0°	---	10°



RECOMMENDED MOUNTING FOOTPRINT

*For additional information on our Pb-Free strategy and soldering details, please download th e ON Semiconductor Soldering and Mounting Techniques Reference manual, SOLDERRM/D.

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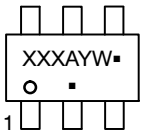
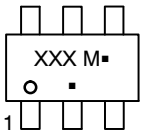
GENERIC MARKING DIAGRAM*



IC

XXX = Specific Device Code
A = Assembly Location
Y = Year
W = Work Week
▪ = Pb−Free Package



STANDARD

XXX = Specific Device Code
M = Date Code
▪ = Pb−Free Package

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, “G” or microdot “▪”, may or may not be present. Some products may not follow the Generic Marking.

STYLE 1:
PIN 1. DRAIN
2. DRAIN
3. GATE
4. SOURCE
5. DRAIN
6. DRAIN

STYLE 2:
PIN 1. EMITTER 2
2. BASE 1
3. COLLECTOR 1
4. EMITTER 1
5. BASE 2
6. COLLECTOR 2

STYLE 3:
PIN 1. ENABLE
2. N/C
3. R BOOST
4. Vz
5. V in
6. V out

STYLE 4:
PIN 1. N/C
2. V in
3. NOT USED
4. GROUND
5. ENABLE
6. LOAD

STYLE 5:
PIN 1. EMITTER 2
2. BASE 2
3. COLLECTOR 1
4. EMITTER 1
5. BASE 1
6. COLLECTOR 2

STYLE 6:
PIN 1. COLLECTOR
2. COLLECTOR
3. BASE
4. EMITTER
5. COLLECTOR
6. COLLECTOR

STYLE 7:
PIN 1. COLLECTOR
2. COLLECTOR
3. BASE
4. N/C
5. COLLECTOR
6. EMITTER

STYLE 8:
PIN 1. Vbus
2. D(in)
3. D(in)+
4. D(out)+
5. D(out)
6. GND

STYLE 9:
PIN 1. LOW VOLTAGE GATE
2. DRAIN
3. SOURCE
4. DRAIN
5. DRAIN
6. HIGH VOLTAGE GATE

STYLE 10:
PIN 1. D(OUT)+
2. GND
3. D(OUT)−
4. D(IN)−
5. VBUS
6. D(IN)+

STYLE 11:
PIN 1. SOURCE 1
2. DRAIN 2
3. DRAIN 2
4. SOURCE 2
5. GATE 1
6. DRAIN 1/GATE 2

STYLE 12:
PIN 1. I/O
2. GROUND
3. I/O
4. I/O
5. VCC
6. I/O

STYLE 13:
PIN 1. GATE 1
2. SOURCE 2
3. GATE 2
4. DRAIN 2
5. SOURCE 1
6. DRAIN 1

STYLE 14:
PIN 1. ANODE
2. SOURCE
3. GATE
4. CATHODE/DRAIN
5. CATHODE/DRAIN
6. CATHODE/DRAIN

STYLE 15:
PIN 1. ANODE
2. SOURCE
3. GATE
4. DRAIN
5. N/C
6. CATHODE

STYLE 16:
PIN 1. ANODE/CATHODE
2. BASE
3. EMITTER
4. COLLECTOR
5. ANODE
6. CATHODE

STYLE 17:
PIN 1. EMITTER
2. BASE
3. ANODE/CATHODE
4. ANODE
5. CATHODE
6. COLLECTOR

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