3.0 A, Very Low-Dropout (VLDO) Fast Transient Response Regulator

NCP57302, NCV57302

The NCP57302 is a high precision, very low dropout (VLDO), low minimum input voltage and low ground current positive voltage regulator that is capable of providing an output current in excess of 3.0 A with a typical dropout voltage of 315 mV at 3.0 A load current and input voltage from 1.8 V and up. The device is stable with ceramic output capacitors. The device can withstand up to 18 V max input voltage.

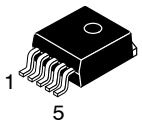
Internal protection features consist of output current limiting, built-in thermal shutdown and reverse output current protection. Logic level enable pin is available. The NCP57302 is an adjustable voltage device and is available in D2PAK-5 package.

Features

- Output Current in Excess of 3.0 A
- Minimum Operating Input Voltage 1.8 V for Full 3 A Output Current
- 315 mV Typical Dropout Voltage at 3.0 A
- Adjustable Output Voltage Range from 1.24 V to 13 V
- Low Ground Current
- Fast Transient Response
- Stable with Ceramic Output Capacitor
- Logic Compatible Enable Pin
- Current Limit, Reverse Current and Thermal Shutdown Protection
- Operation up to 13.5 V Input Voltage
- NCV Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC-Q100 Qualified and PPAP Capable
- These are Pb-Free Devices

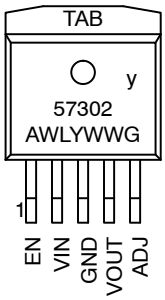
Applications

- Consumer and Industrial Equipment Point of Regulation
- Servers and Networking Equipment
- FPGA, DSP and Logic Power supplies
- Switching Power Supply Post Regulation
- Battery Chargers
- Functional Replacement for Industry Standard MIC29300, MIC39300, MIC37300 with Improved Minimum Input Voltage Specification



D²PAK
CASE 936A

MARKING DIAGRAMS



y	= P (NCP), V (NCV)
A	= Assembly Location
WL	= Wafer Lot
Y	= Year
WW	= Work Week
G	= Pb-Free Package

ORDERING INFORMATION

See detailed ordering and shipping information on page 9 of this data sheet.

NOTE: Some of the devices on this data sheet have been **DISCONTINUED**. Please refer to the table on page 9.

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TYPICAL APPLICATIONS

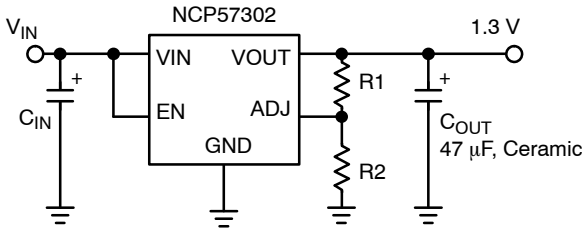

Figure 1. Adjustable Regulator

PIN FUNCTION DESCRIPTION

Pin Number	Pin Name	Pin Function
1	EN	Enable Input: CMOS and TTL logic compatible. Logic high = enable; Logic low = shutdown.
2	VIN	Input voltage which supplies both the internal circuitry and the current to the output load
3	GND	Ground
TAB	TAB	TAB is connected to ground.
4	VOUT	Linear Regulator Output.
5	ADJ	Adjustable Regulator Feedback Input. Connect to output voltage resistor divider central node.

ABSOLUTE MAXIMUM RATINGS

Symbol	Rating	Value	Unit
V_{IN}	Supply Voltage	0 to 18	V
V_{EN}	Enable Input Voltage	0 to 18	V
$V_{OUT} - V_{IN}$	Reverse $V_{OUT} - V_{IN}$ Voltage (EN = Shutdown or V_{IN} = 0 V) (Note 1)	0 to 6.5	V
P_D	Power Dissipation (Notes 2 and 3)	Internally Limited	
T_J	Junction Temperature	$-40 \le T_J \le +125$	°C
T_S	Storage Temperature	$-65 \le T_J \le +150$	°C
	ESD Rating (Notes 4 and 5) Human Body Model Machine Model	2000 200	V

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

NOTE: All voltages are referenced to GND pin unless otherwise noted.

1. The ENABLE pin input voltage must be ≤ 0.8 V or V_{IN} must be connected to ground potential.
2. $P_{D(max)} = (T_{J(max)} - T_A) / R_{\theta JA}$, where $R_{\theta JA}$ depends upon the printed circuit board layout.
3. This protection is not guaranteed outside the Recommended Operating Conditions.
4. Devices are ESD sensitive. Handling precautions recommended..
5. This device series incorporates ESD protection and is tested by the following methods:
   ESD Human Body Model (HBM) tested per AEC-Q100-002 (EIA/JESD22-A114C)
   ESD Machine Model (MM) tested per AEC-Q100-003 (EIA/JESD22-A115C)
   This device contains latch-up protection and exceeds 100 mA per JEDEC Standard JESD78.

RECOMMENDED OPERATING CONDITIONS (Note 6)

Symbol	Rating	Value	Unit
V_{IN}	Supply Voltage	1.8 to 13.5	V
V_{EN}	Enable Input Voltage	0 to 13.5	V
T_J	Junction Temperature	$-40 \le T_J \le +125$	°C

Functional operation above the stresses listed in the Recommended Operating Ranges is not implied. Extended exposure to stresses beyond the Recommended Operating Ranges limits may affect device reliability.

6. The device is not guaranteed to function outside it's Recommended operating conditions.

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ELECTRICAL CHARACTERISTICS

T_J = 25 °C with V_{IN} = $V_{OUT\ nominal}$ + 0.6 V; V_{EN} = V_{IN}; I_L = 10 mA; bold values indicate −40 °C < T_J < +125 °C, unless noted. (Note 7)

Parameter	Conditions	Min	Typ	Max	Unit
Output Voltage Accuracy	I_L = 10 mA	−1.5		+1.5	%
	10 mA < I_{OUT} < 3 A , $V_{OUT\ nominal}$ + 0.6 V ≤ V_{IN} ≤ 13.5 V	**−2.5**		**+2.5**	%
Output Voltage Line Regulation	V_{IN} = $V_{OUT\ nominal}$ + 0.6 V to 13.5 V; I_L = 10 mA		0.02	0.5	%
Output Voltage Load Regulation	I_L = 10 mA to 3 A		0.2	1	%
V_{IN} − V_{OUT} Dropout Voltage (Note 8)	I_L = 1.0 A (Note 10)		182	**295**	mV
	I_L = 1.5 A		220	**350**	mV
	I_L = 2.0 A (Note 10)		250	**410**	mV
	I_L = 3.0 A		315	**520**	mV
Ground Pin Current (Note 9)	I_L = 3.0 A		60	90 **120**	mA
Ground Pin Current in Shutdown	V_{EN} ≤ 0.5 V		1.0	5	μA
Overload Protection Current Limit	V_{OUT} = 0 V		3.5	**5**	A
Start-up Time	V_{EN} = V_{IN}, V_{OUT} nominal = 2.5 V, I_{OUT} = 10 mA, C_{OUT} = 47 μF		100	500	μs
Reference Voltage		1.221 **1.209**	1.240	1.259 **1.271**	V
Adjust Pin Bias Current			100	200 **350**	nA
ENABLE INPUT					
Enable Input Signal Levels	Regulator enable	**1.4**			V
	Regulator shutdown			**0.8**	V
Enable pin Input Current	V_{EN} ≤ 0.8 V (Regulator shutdown)			2 **4**	μA
	6.5 V > V_{EN} ≥ 1.4 V (Regulator enable)		15	30 **40**	μA

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

7. $V_{OUTnominal}$ can be set by external resistor divider in the application. Tested for $V_{OUTnominal}$ = 1.240 V unless noted.
8. V_{DO} = V_{IN} − V_{OUT} when V_{OUT} decreases to 98% of its nominal output voltage with V_{IN} = V_{OUT} + 1 V. Tested for $V_{OUTnominal}$ = 2.5 V.
9. I_{IN} = I_{GND} + I_{OUT}.
10. Guaranteed by design.

Package	Conditions / PCB Footprint	Thermal Resistance
D2PAK-5, Junction-to-Case		$R_{\theta JC}$ = 2.1 °C/W
D2PAK-5, Junction-to-Air	PCB with 100 mm^2 2.0 oz Copper Heat Spreading Area	$R_{\theta JA}$ = 52 °C/W

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TYPICAL CHARACTERISTICS

T_J = 25 °C if not otherwise noted

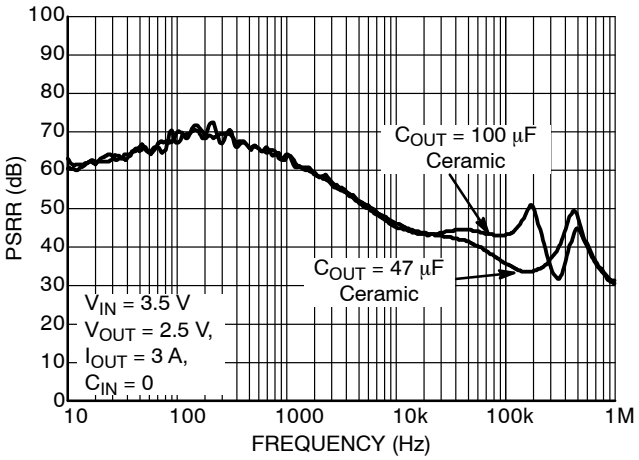

Figure 2. Power Supply Rejection Ratio

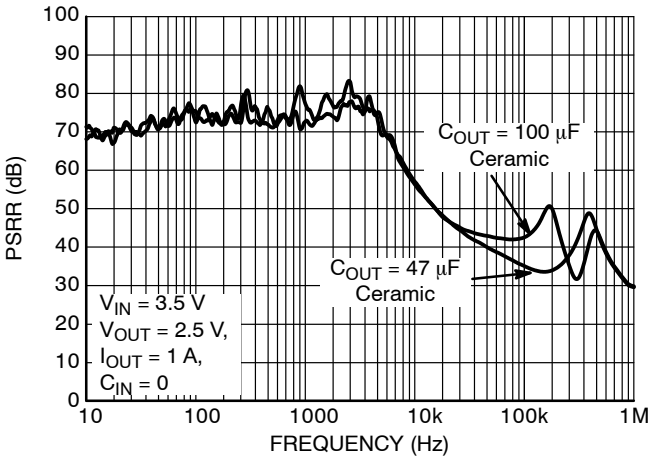

Figure 3. Power Supply Rejection Ratio

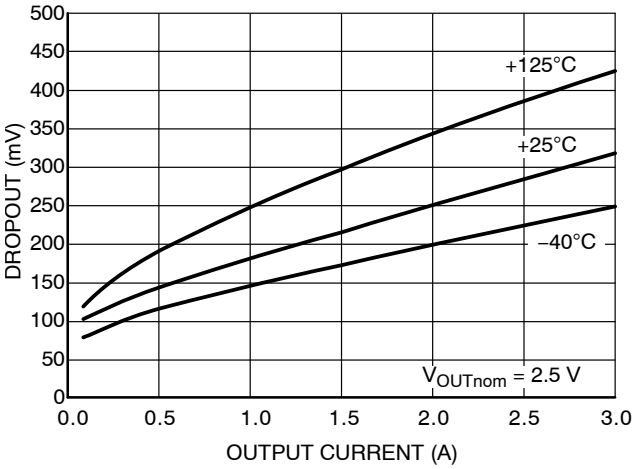

Figure 4. Dropout Voltage vs. Output Current

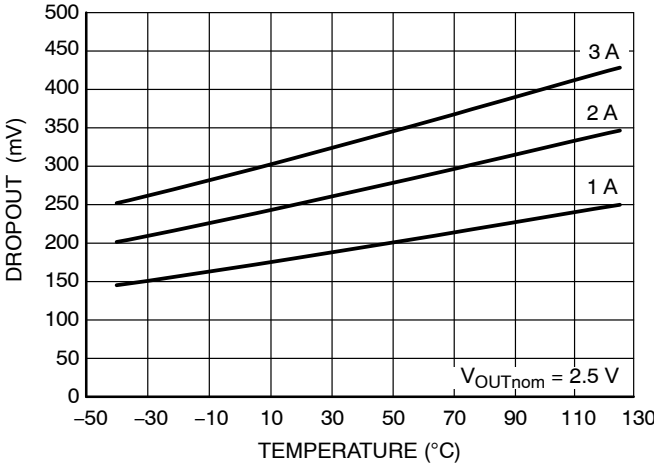

Figure 5. Dropout Voltage vs. Temperature

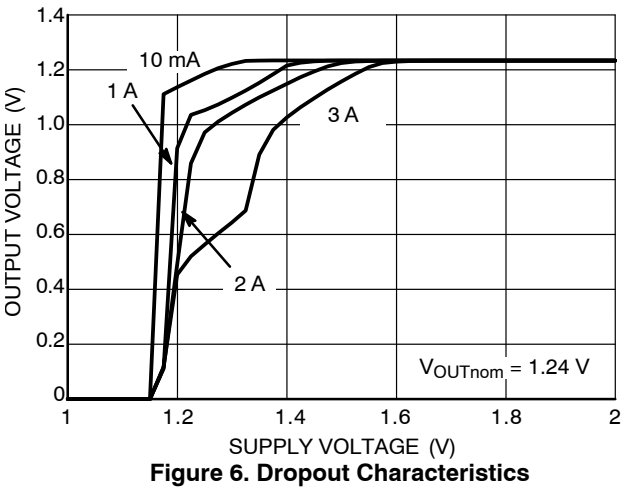

Figure 6. Dropout Characteristics

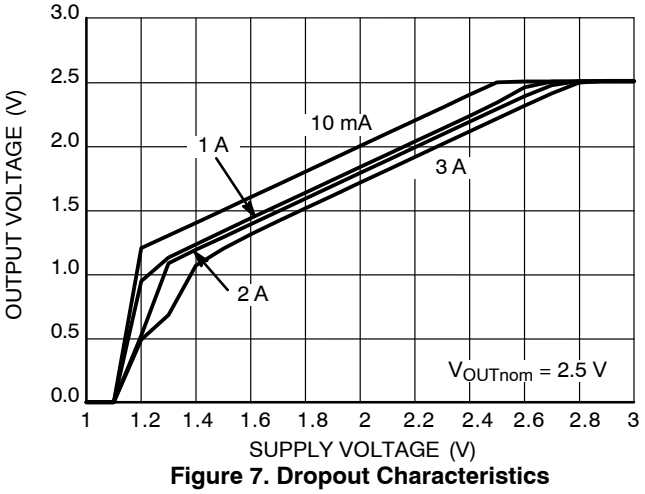

Figure 7. Dropout Characteristics

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TYPICAL CHARACTERISTICS

T_J = 25 °C if not otherwise noted

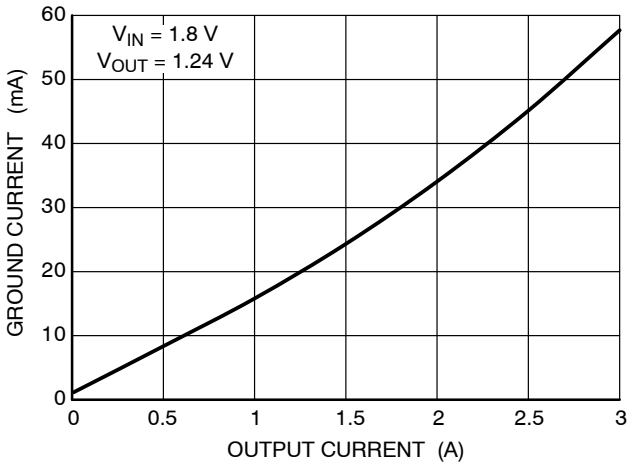

Figure 8. Ground Current vs. Output Current

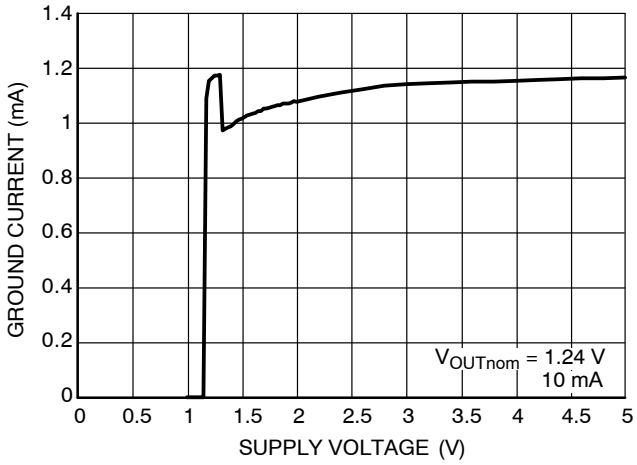

Figure 9. Ground Current vs. Supply Voltage

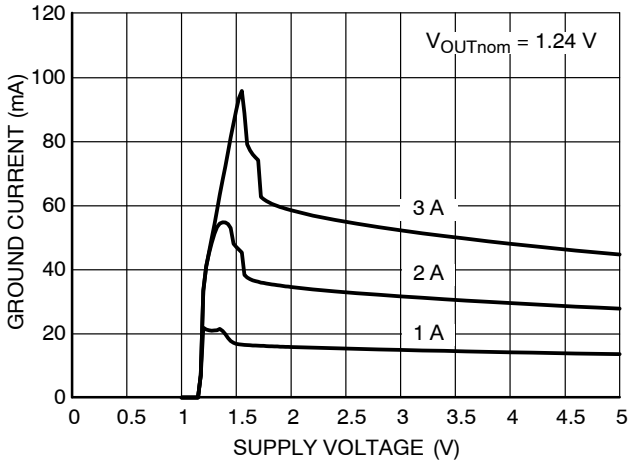

Figure 10. Ground Current vs. Supply Voltage

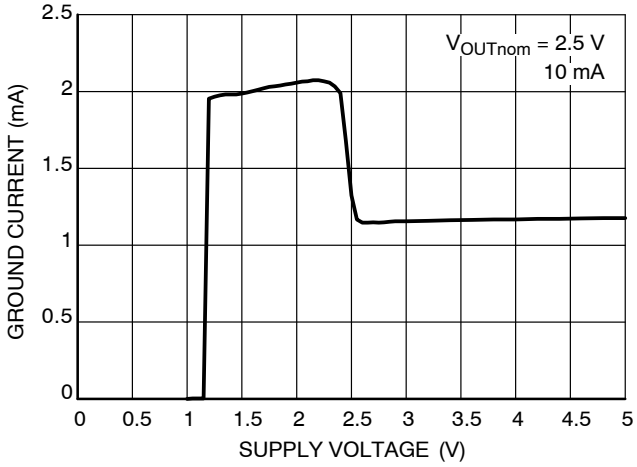

Figure 11. Ground Current vs. Supply Voltage

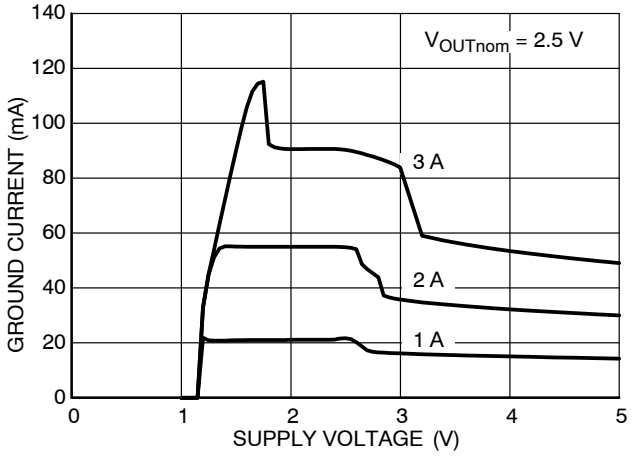

Figure 12. Ground Current vs. Supply Voltage

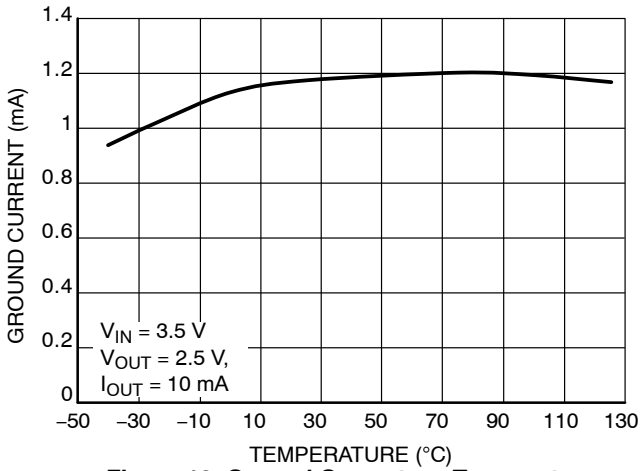

Figure 13. Ground Current vs. Temperature

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TYPICAL CHARACTERISTICS

T_J = 25 °C if not otherwise noted

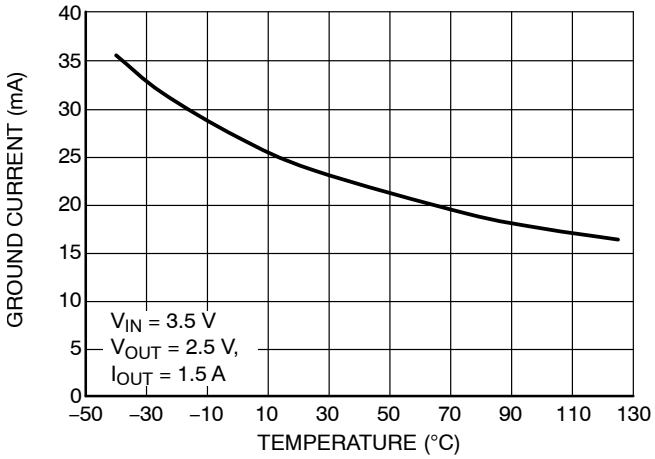

Figure 14. Ground Current vs. Temperature

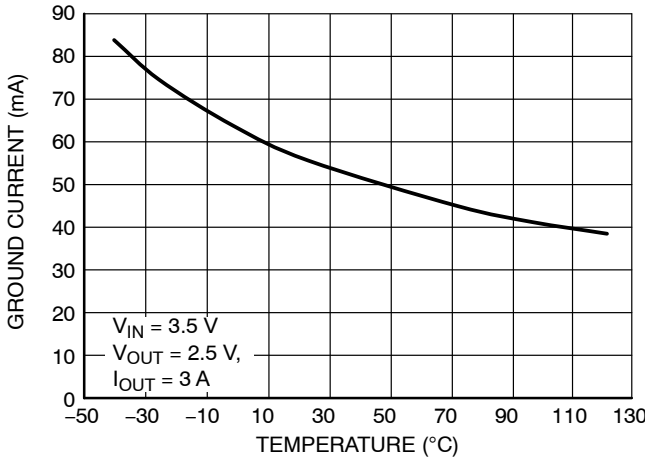

Figure 15. Ground Current vs. Temperature

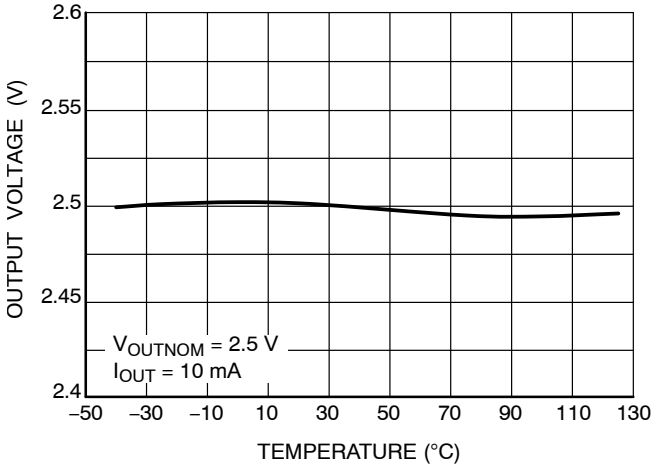

Figure 16. Output Voltage vs. Temperature

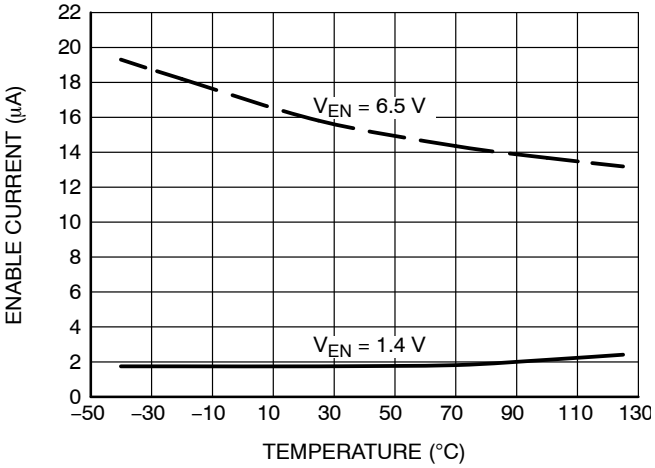

Figure 17. Enable Pin Input Current vs. Temperature

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FUNCTIONAL CHARACTERISTICS

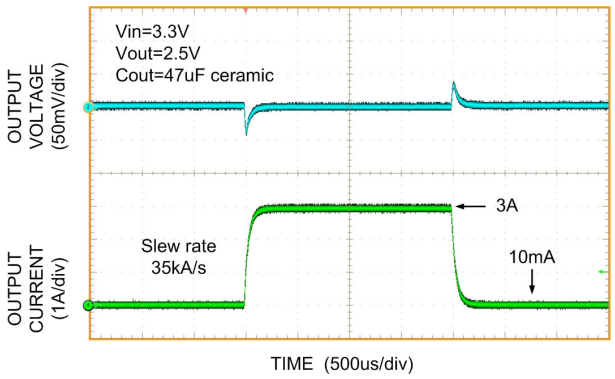

Figure 18. Load Transient Response

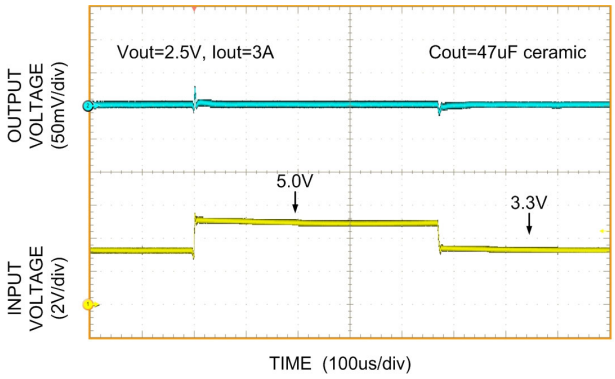

Figure 19. Line Transient Response

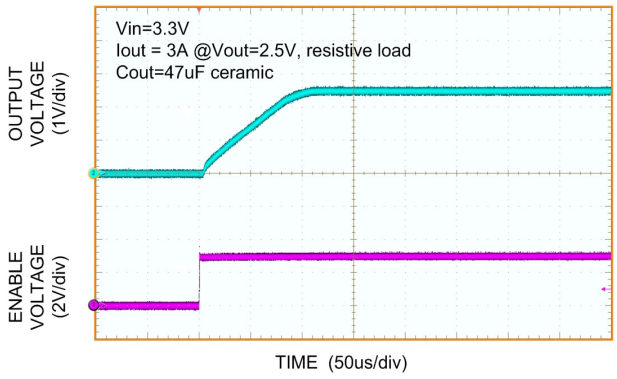

Figure 20. Enable Transient Response

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APPLICATIONS INFORMATION

Output Capacitor and Stability

The NCP57302 device requires an output capacitor for stable operation. The NCP57302 is designed to operate with ceramic output capacitors. The recommended output capacitance value is 47 μF or greater. Such capacitors help to improve transient response and noise reduction at high frequency.

Input Capacitor

An input capacitor of 1.0 μF or greater is recommended when the device is more than 4 inches away from the bulk supply capacitance, or when the supply is a battery. Small, surface-mount chip capacitors can be used for the bypassing. The capacitor should be place within 1 inch of the device for optimal performance. Larger values will help to improve ripple rejection by bypassing the input of the regulator, further improving the integrity of the output voltage.

Minimum Load Current

The NCP57302 regulator is specified between finite loads. A 10 mA minimum load current is necessary for proper operation.

Enable Input

NCP57302 regulators also feature an enable input for on/off control of the device. It's shutdown state draws "zero" current from input voltage supply (only microamperes of leakage). The enable input is TTL/CMOS compatible for simple logic interface, but can be connected up to V_{IN}.

Overcurrent and Reverse Output Current Protection

The NCP57302 regulator is fully protected from damage due to output current overload and output short conditions. When NCP57302 output is overloaded, Output Current limiting is provided. This limiting is linear; output current during overload or output short conditions is constant. These features are advantageous for powering FPGAs and other ICs having current consumption higher than nominal during their startup.

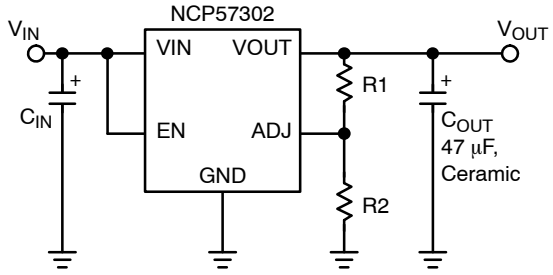
Thermal shutdown disables the NCP57302 device when the die temperature exceeds the maximum safe operating temperature.

When NCP57302 is disabled and (V_{OUT} − V_{IN}) voltage difference is less than 6.5 V in the application, the output structure of these regulators is able to withstand output voltage (backup battery as example) to be applied without reverse current flow.

Adjustable Voltage Design

The NCP/NCV57302 Adjustable voltage Device Output voltage is set by the ratio of two external resistors as shown in Figure 21.

The device maintains the voltage at the ADJ pin at 1.24 V referenced to ground. The current in R2 is then equal to 1.24 V / R2, and the current in R1 is the current in R2 plus the ADJ pin bias current. The ADJ pin bias current flows from V_{OUT} through R1 into the ADJ pin.



$$V_{OUT} = 1.24\ V \cdot \left(1 + \frac{R1}{R2}\right) + I_{ADJ} \cdot R1$$

Figure 21. Adjustable Voltage Operation

For the R2 resistor value up to 15 kΩ the I_{ADJ} current impact can be neglected and the R1 resistor value can be calculated y:

$$R1 = R2 \times \left(\frac{V_{OUT}}{1.24} - 1\right) \quad \text{(eq. 1)}$$

Where V_{OUT} is the desired nominal output voltage.

Thermal Considerations

The power handling capability of the device is limited by the maximum rated junction temperature (125 °C). The P_D total power dissipated by the device has two components, Input to output voltage differential multiplied by Output current and Input voltage multiplied by GND pin current.

$$P_D = (V_{IN} - V_{OUT}) \cdot I_{OUT} + V_{IN} \cdot I_{GND} \quad \text{(eq. 2)}$$

The GND pin current value can be found in Electrical Characteristics table and in Typical Characteristics graphs.

The Junction temperature T_J is

$$T_J = T_A + P_D \cdot R_{\theta JA} \quad \text{(eq. 3)}$$

where T_A is ambient temperature and $R_{\theta JA}$ is the Junction to Ambient Thermal Resistance of the NCP/NCV57302 device mounted on the specific PCB.

To maximize efficiency of the application and minimize thermal power dissipation of the device it is convenient to use the Input to output voltage differential as low as possible.

The static typical dropout characteristics for various output voltage and output current can be found in the Typical Characteristics graphs.

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ORDERING INFORMATION

Device	Output Current	Output Voltage	Junction Temp. Range	Package	Shipping†
NCV57302DSADJR4G*	3.0 A	ADJ	−40 °C to +125 °C	D2PAK-5 (Pb-Free)	800 / Tape & Reel

DISCONTINUED (Note 11)

NCP57302DSADJR4G	3.0 A	ADJ	−40 °C to +125 °C	D2PAK-5 (Pb-Free)	800 / Tape & Reel

† For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

* NCV Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC-Q100 Qualified and PPAP Capable.

11. **DISCONTINUED:** This device is not available. Please contact your **onsemi** representative for information. The most current information on this device may be available on www.onsemi.com.

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REVISION HISTORY

Revision	Description of Changes	Date
3	Rebranded the Data Sheet to **onsemi** format. NCP57302DSADJR4G OPN Marked as Discontinued.	2/2/2026

This document has undergone updates prior to the inclusion of this revision history table. The changes tracked here only reflect updates made on the noted approval dates.

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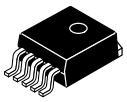
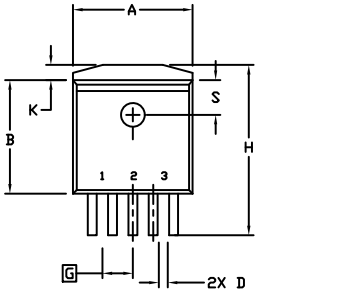


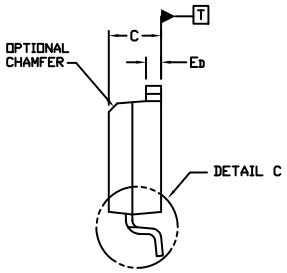
D²PAK 5–LEAD
CASE 936A–02
ISSUE E

DATE 28 JUL 2021

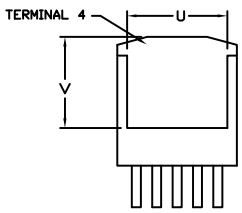
SCALE 1:1



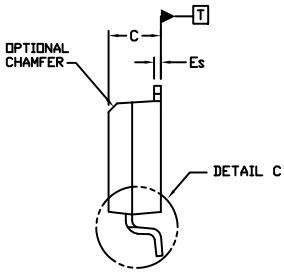
TOP VIEW



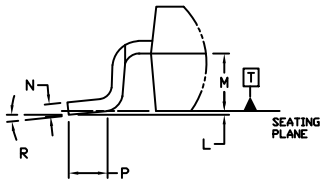
SIDE VIEW
DUAL GUAGE CONSTRUCTION



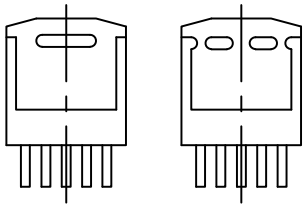
BOTTOM VIEW



SIDE VIEW
SINGLE GUAGE CONSTRUCTION



DETAIL C
TIP LEADFORM
ROTATED 90° CW



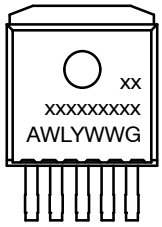
BOTTOM VIEW
OPTIONAL CONSTRUCTIONS

NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCHES
3. TAB CONTOUR OPTIONAL WITHIN DIMENSIONS A AND K.
4. DIMENSIONS U AND V ESTABLISH A MINIMUM MOUNTING SURFACE FOR TERMINAL 4.
5. DIMENSIONS A AND B DO NOT INCLUDE MOLD FLASH OR GATE PROTRUSIONS. MOLD FLASH AND GATE PROTRUSIONS NOT TO EXCEED 0.025 (0.635) MAXIMUM.

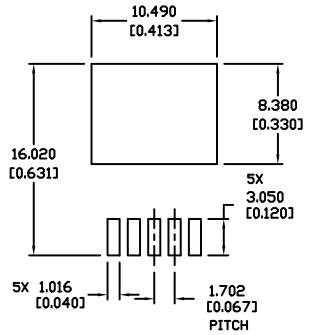
	INCHES		MILLIMETERS	
DIM	MIN.	MAX.	MIN.	MAX.
A	0.396	0.403	9.804	10.236
B	0.356	0.368	9.042	9.347
C	0.170	0.180	4.318	4.572
D	0.026	0.036	0.660	0.914
ED	0.045	0.055	1.143	1.397
ES	0.018	0.026	0.457	0.660
G	0.067 BSC		1.702 BSC	
H	0.539	0.579	13.691	14.707
K	0.050 REF		1.270 REF	
L	0.000	0.010	0.000	0.254
M	0.088	0.102	2.235	2.591
N	0.018	0.026	0.457	0.660
P	0.058	0.078	1.473	1.981
R	0°	8°	0°	8°
S	0.116 REF		2.946 REF	
U	0.200 MIN		5.080 MIN	
V	0.250 MIN		6.350 MIN	

GENERIC MARKING DIAGRAM*



XXXXXX	= Device Code
A	= Assembly Location
WL	= Wafer Lot
Y	= Year
WW	= Work Week
G	= Pb–Free Package

*This information is generic. Please refer to device data sheet for actual part marking. Pb–Free indicator, “G” or microdot “▪”, may or may not be present. Some products may not follow the Generic Marking.



RECOMMENDED
MOUNTING FOOTPRINT *

* For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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DESCRIPTION:	**D2PAK 5–LEAD**		**PAGE 1 OF 1**

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