Wide Input Voltage Low Dropout, Ultra-Low Iq Regulator

NCP716B

The NCP716B is 150 mA LDO Linear Voltage Regulator. It is a very stable and accurate device with ultra-low ground current consumption (4.7 μA over the full output load range) and a wide input voltage range (up to 24 V). The regulator incorporates several protection features such as Thermal Shutdown and Current Limiting.

Features

- Operating Input Voltage Range: 2.5 V to 24 V
- Fixed Voltage Options Available: 3.0 V, 3.3 V and 5.0 V
- Ultra Low Quiescent Current: Max. 4.7 μA over Temperature
- ±2% Accuracy over Full Temperature Range
- Noise: 115 μV_{RMS} from 200 Hz to 100 kHz
- Thermal Shutdown and Current Limit Protection
- Available in TSOP-5 Package
- This is a Pb-Free Device

Typical Applications

- Portable Equipment
- Communication Systems
- Industrial Measurement Systems
- Home Automation Devices

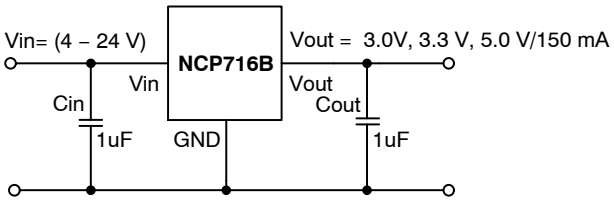
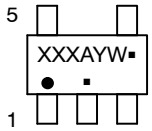


Figure 1. Typical Application Schematic

MARKING DIAGRAM



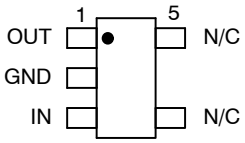
TSOP-5
CASE 483



XXX = Specific Device Code
A = Assembly Location
Y = Year
W = Work Week
▪ = Pb-Free Package

(Note: Microdot may be in either location)

PIN CONNECTIONS



TSOP-5
(Top View)

ORDERING INFORMATION

See detailed ordering, marking and shipping information on page 7 of this data sheet.

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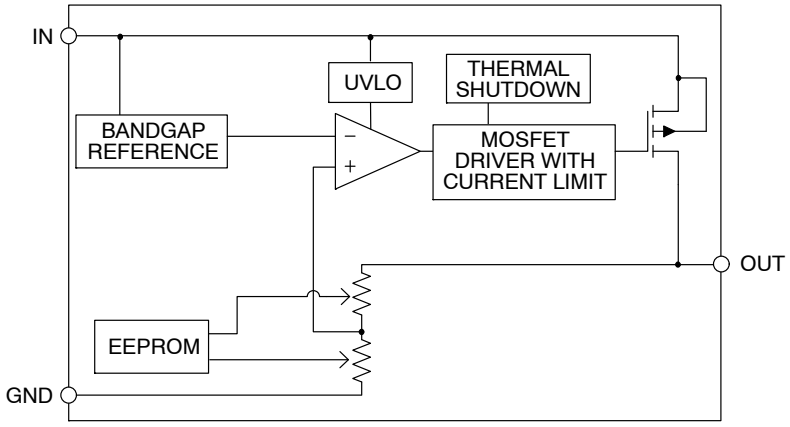

Figure 2. Simplified Block Diagram

Table 1. PIN FUNCTION DESCRIPTION

Pin No.	Pin Name	Description
1	OUT	Regulated output voltage pin. A small 1.0 μF ceramic capacitor is needed from this pin to ground to assure stability.
2	GND	Power supply ground.
3	IN	Input pin. A small capacitor is needed from this pin to ground to assure stability.
4	N/C	No connection. This pin can be tied to ground to improve thermal dissipation or left disconnected.
5	N/C	No connection. This pin can be tied to ground to improve thermal dissipation or left disconnected.

Table 2. ABSOLUTE MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Input Voltage (Note 1)	V_{IN}	−0.3 to 24	V
Output Voltage	V_{OUT}	−0.3 to 6	V
Output Short Circuit Duration	t_{SC}	Indefinite	s
Maximum Junction Temperature	$T_{J(MAX)}$	150	°C
Storage Temperature	T_{STG}	−55 to 150	°C
ESD Capability, Human Body Model (Note 2)	ESD_{HBM}	2000	V
ESD Capability, Machine Model (Note 2)	ESD_{MM}	200	V

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. Refer to ELECTRICAL CHARACTERISTICS and APPLICATION INFORMATION for Safe Operating Area.
2. This device series incorporates ESD protection and is tested by the following methods:
   ESD Human Body Model tested per EIA/JESD22-A114
   ESD Machine Model tested per EIA/JESD22-A115
   ESD Charged Device Model tested per EIA/JESD22-C101E
   Latchup Current Maximum Rating tested per JEDEC standard: JESD78.

Table 3. THERMAL CHARACTERISTICS

Rating	Symbol	Value	Unit
Thermal Characteristics, TSOP-5 Thermal Resistance, Junction-to-Air	$R_{\theta JA}$	250	°C/W

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Table 4. ELECTRICAL CHARACTERISTICS Voltage version 3.0 V

$-40\ °C \le T_J \le 125\ °C$; V_{IN} = 4.0 V; I_{OUT} = 1 mA, $C_{IN} = C_{OUT}$ = 1.0 μF, unless otherwise noted. Typical values are at T_J = +25 °C. (Note 5)

Parameter	Test Conditions	Symbol	Min	Typ	Max	Unit
Operating Input Voltage		V_{IN}	2.5		24	V
Output Voltage Accuracy	$-40\ °C \le T_J \le 125\ °C$	V_{OUT}	2.94	3.0	3.06	V
Line Regulation	V_{OUT} + 1 V ≤ V_{IN} ≤ 24 V, I_{OUT} = 0.1 mA	Reg_{LINE}		4	10	mV
Load Regulation	I_{OUT} = 0.1 mA to 150 mA	Reg_{LOAD}		0.0013	0.007	%/mA
Dropout Voltage (Note 3)	V_{OUT} = 0.97 $V_{OUT(NOM)}$, I_{OUT} = 150 mA	V_{DO}		700	1100	mV
Maximum Output Current	(Note 6)	I_{OUT}	150			mA
Ground Current	I_{OUT} = 0 mA, $-40\ °C < T_A < 125\ °C$	I_{GND}		3.2	4.7	μA
Power Supply Rejection Ratio	V_{IN} = 4.0 V, V_{OUT} = 3.0 V + 200 mVpp modulation, I_{OUT} = 1 mA, C_{OUT} =10 μF; f = 100 kHz	PSRR		55		dB
Output Noise Voltage	V_{OUT} = 3.0 V, I_{OUT} = 150 mA, f = 100 Hz to 100 kHz	V_N		80		μV_{rms}
Thermal Shutdown Temperature (Note 4)	Temperature increasing from T_J = +25 °C	T_{SD}		180		°C
Thermal Shutdown Hysteresis (Note 4)	Temperature falling from T_{SD}	T_{SDH}	–	10	–	°C

3. Characterized when V_{OUT} falls 3% below the nominal V_{OUT} = 3.0 V
4. Guaranteed by design and characterization.
5. Performance guaranteed over the indicated operating temperature range by design and/or characterization production tested at $T_J = T_A$ = 25 °C. Low duty cycle pulse techniques are used during testing to maintain the junction temperature as close to ambient as possible.
6. Please follow the Safe Operating Area.

Table 5. ELECTRICAL CHARACTERISTICS Voltage version 5.0 V

$-40\ °C \le T_J \le 125\ °C$; V_{IN} = 6.0 V; I_{OUT} = 1 mA, $C_{IN} = C_{OUT}$ = 1.0 μF, unless otherwise noted. Typical values are at T_J = +25 °C. (Note 9)

Parameter	Test Conditions	Symbol	Min	Typ	Max	Unit
Operating Input Voltage		V_{IN}	2.5		24	V
Output Voltage Accuracy	$-40\ °C \le T_J \le 125\ °C$	V_{OUT}	4.90	5.0	5.10	V
Line Regulation	V_{OUT} + 1 V ≤ V_{IN} ≤ 24 V, I_{OUT} = 0.1 mA	Reg_{LINE}		4	10	mV
Load Regulation	I_{OUT} = 0.1 mA to 150 mA	Reg_{LOAD}		0.0013	0.008	%/mA
Dropout Voltage (Note 7)	V_{OUT} = 0.97 $V_{OUT(NOM)}$, I_{OUT} = 150 mA	V_{DO}		600	955	mV
Maximum Output Current	(Note 10)	I_{OUT}	150			mA
Ground Current	I_{OUT} = 0 mA, $-40\ °C < T_A < 125\ °C$	I_{GND}		3.2	4.7	μA
Power Supply Rejection Ratio	V_{IN} = 6.0 V, V_{OUT} = 5.0 V + 200 mVpp modulation, I_{OUT} = 1 mA, C_{OUT} =10 μF; f = 100 kHz	PSRR		53		dB
Output Noise Voltage	V_{OUT} = 5.0 V, I_{OUT} = 150 mA, f = 100 Hz to 100 kHz	V_N		115		μV_{rms}
Thermal Shutdown Temperature (Note 8)	Temperature increasing from T_J = +25 °C	T_{SD}		180		°C
Thermal Shutdown Hysteresis (Note 8)	Temperature falling from T_{SD}	T_{SDH}	–	10	–	°C

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

7. Characterized when V_{OUT} falls 3% below the nominal V_{OUT} = 5.0 V
8. Guaranteed by design and characterization.
9. Performance guaranteed over the indicated operating temperature range by design and/or characterization production tested at $T_J = T_A$ = 25 °C. Low duty cycle pulse techniques are used during testing to maintain the junction temperature as close to ambient as possible.
10. Please follow the Safe Operating Area.

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TYPICAL CHARACTERISTICS

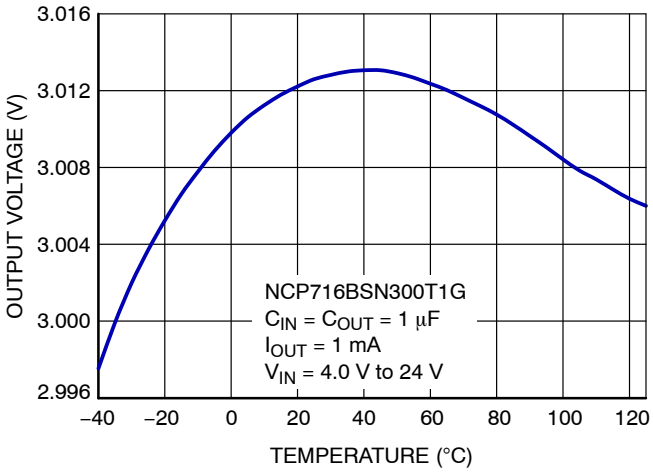

Figure 3. Output Voltage vs. Temperature

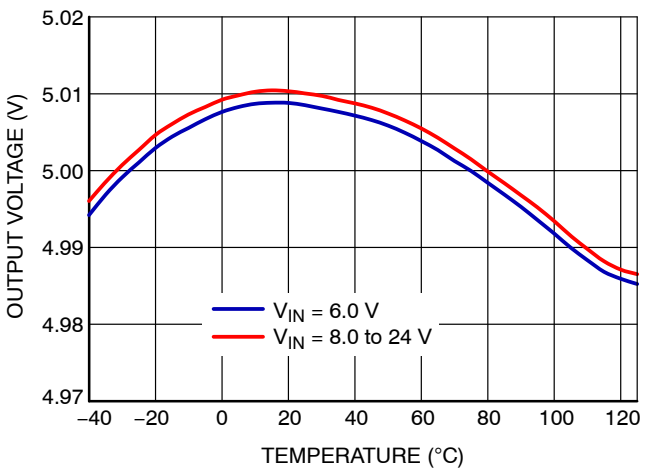

Figure 4. Output Voltage vs. Temperature

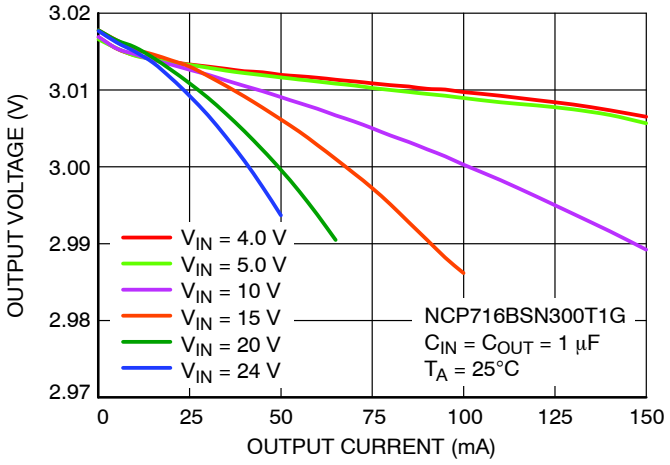

Figure 5. Output Voltage vs. Output Current

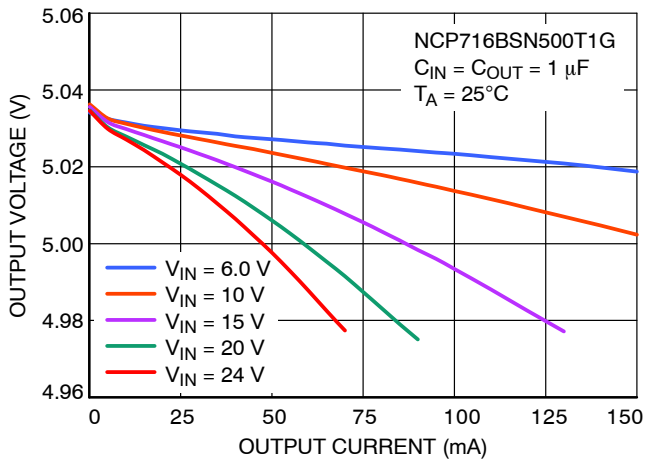

Figure 6. Output Voltage vs. Output Current

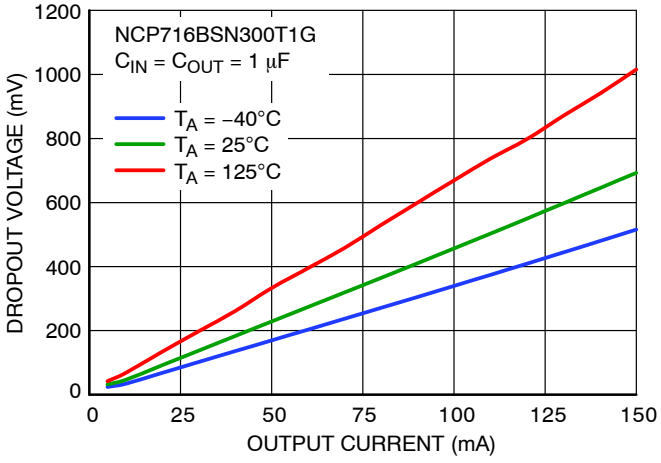

Figure 7. Dropout Voltage vs. Output Current

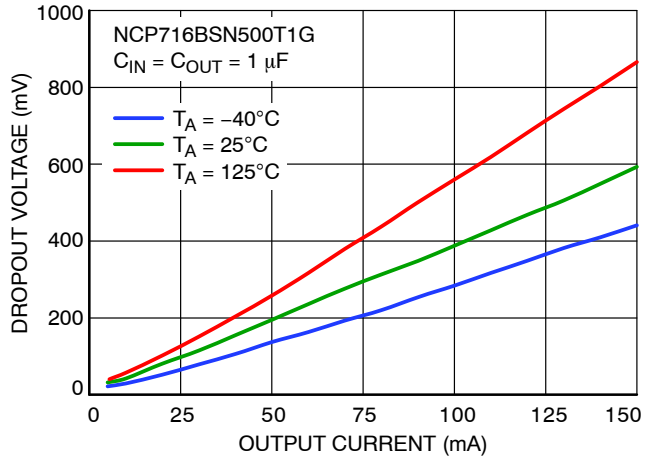

Figure 8. Dropout Voltage vs. Output Current

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TYPICAL CHARACTERISTICS

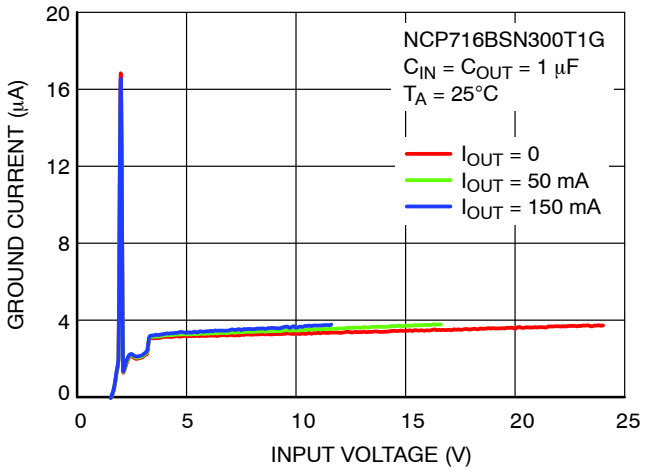

Figure 9. Ground Current vs. Input Voltage

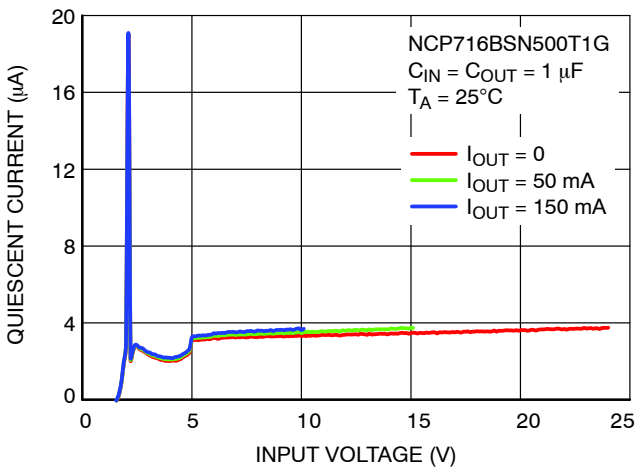

Figure 10. Ground Current vs. Input Voltage

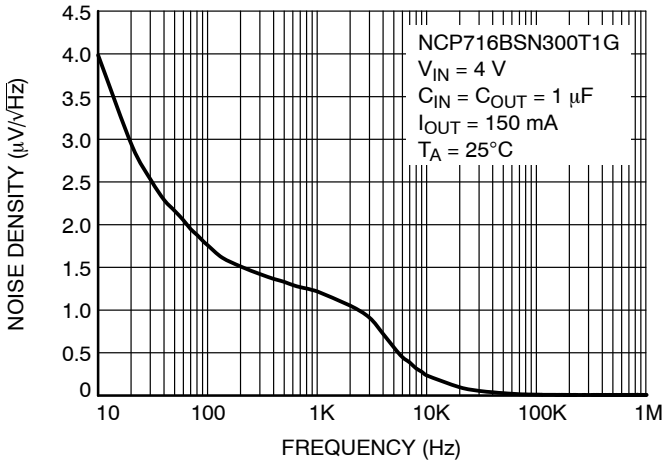

Figure 11. Spectral Noise Density vs. Frequency

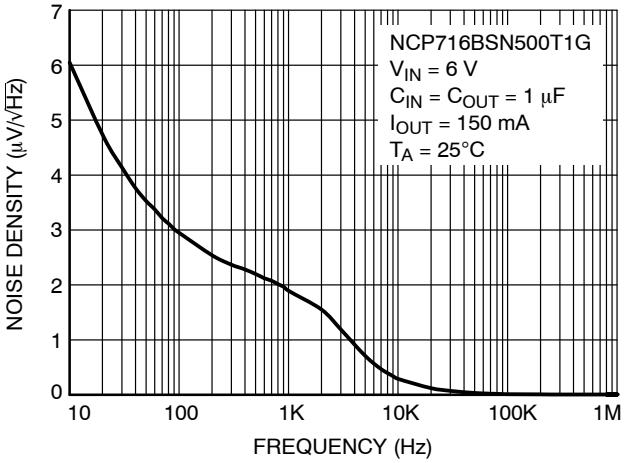

Figure 12. Spectral Noise Density vs. Frequency

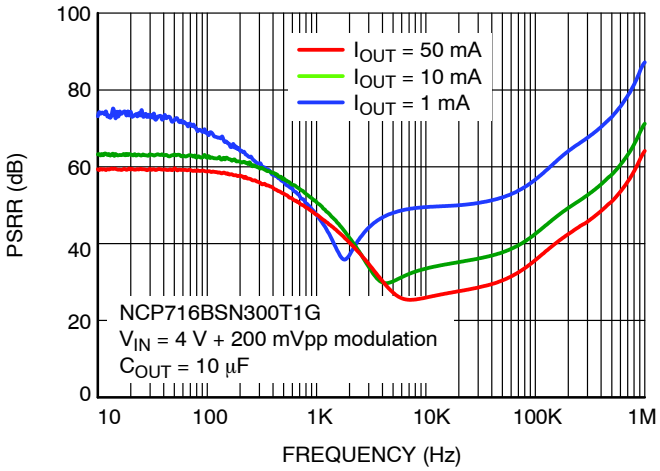

Figure 13. PSRR vs. Frequency

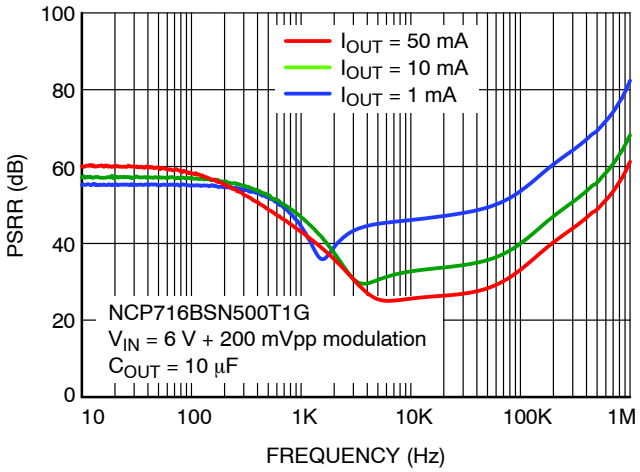

Figure 14. PSRR vs. Frequency

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TYPICAL CHARACTERISTICS

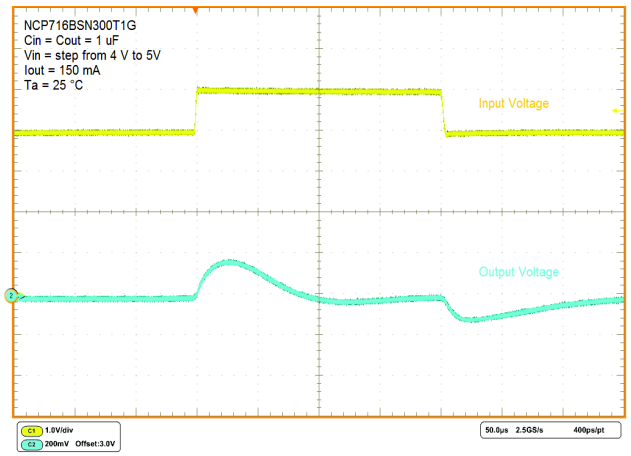

Figure 15. Line Transient Response

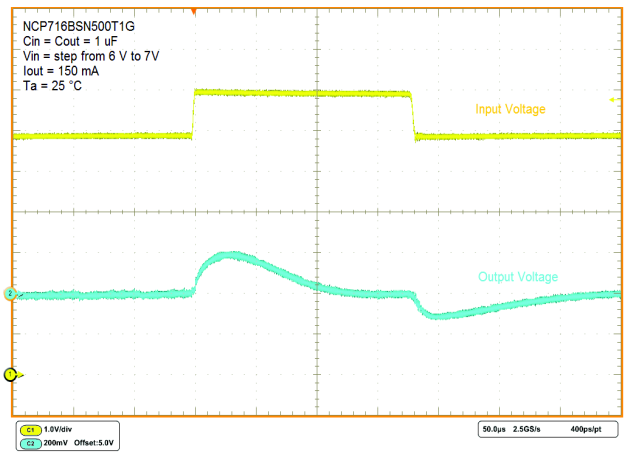

Figure 16. Line Transient Response

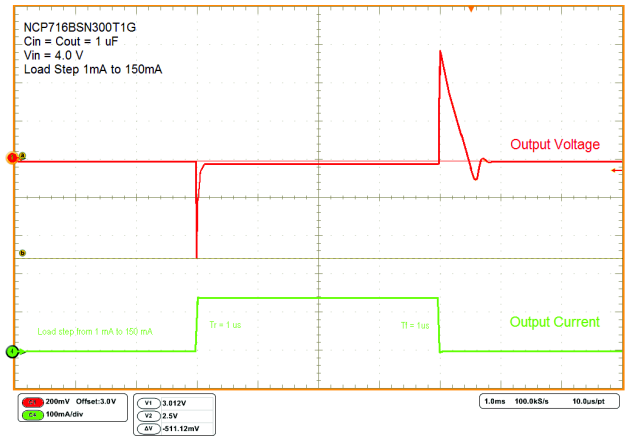

Figure 17. Load Transient Response

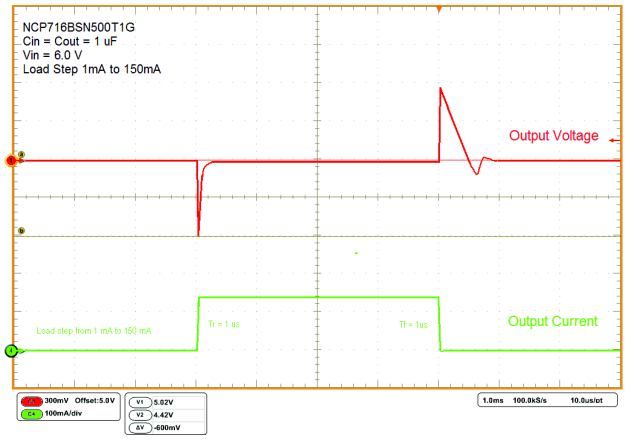

Figure 18. Load Transient Response

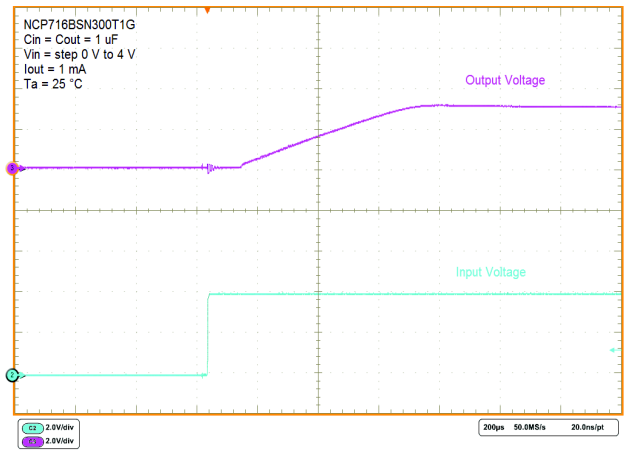

Figure 19. Turn-On Response

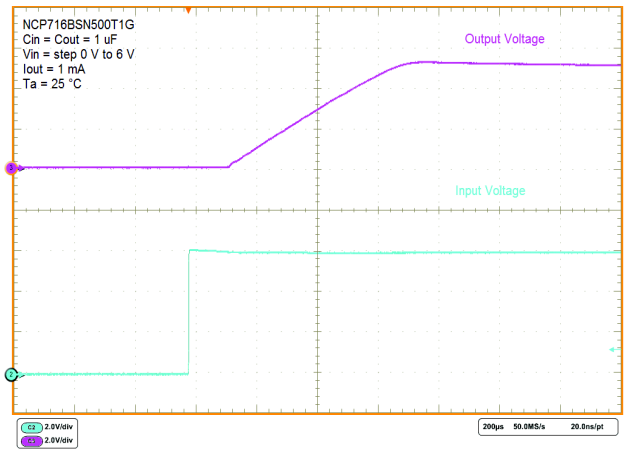

Figure 20. Turn-On Response

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APPLICATIONS INFORMATION

The NCP716B is the member of new family of Wide Input Voltage Range Low Dropout Regulators which delivers Ultra Low Ground Current consumption, Good Noise and Power Supply Rejection Ratio Performance.

Input Decoupling (C_{IN})

It is recommended to connect at least 1.0 μF Ceramic X5R or X7R capacitor between IN and GND pin of the device. This capacitor will provide a low impedance path for any unwanted AC signals or Noise superimposed onto constant Input Voltage. The good input capacitor will limit the influence of input trace inductances and source resistance during sudden load current changes.

Higher capacitance and lower ESR Capacitors will improve the overall line transient response.

Output Decoupling (C_{OUT})

The NCP716B does not require a minimum Equivalent Series Resistance (ESR) for the output capacitor. The device is designed to be stable with standard ceramics capacitors with values of 1.0 μF or greater up to 10 μF. The X5R and X7R types have the lowest capacitance variations over temperature thus they are recommended.

Power Dissipation and Heat sinking

The maximum power dissipation supported by the device is dependent upon board design and layout. Mounting pad configuration on the PCB, the board material, and the ambient temperature affect the rate of junction temperature rise for the part. The maximum power dissipation the NCP716B can handle is given by:

$$P_{D(MAX)} = \frac{\left[T_{J(MAX)} - T_A\right]}{R_{\theta JA}} \quad \text{(eq. 1)}$$

The power dissipated by the NCP716B for given application conditions can be calculated from the following equations:

$$P_D \approx V_{IN}\left(I_{GND}(I_{OUT})\right) + I_{OUT}\left(V_{IN} - V_{OUT}\right) \quad \text{(eq. 2)}$$

or

$$V_{IN(MAX)} \approx \frac{P_{D(MAX)} + \left(V_{OUT} \times I_{OUT}\right)}{I_{OUT} + I_{GND}} \quad \text{(eq. 3)}$$

For reliable operation, junction temperature should be limited to +125 °C maximum.

Hints

VIN and GND printed circuit board traces should be as wide as possible. When the impedance of these traces is high, there is a chance to pick up noise or cause the regulator to malfunction. Place external components, especially the output capacitor, as close as possible to the NCP716B, and make traces as short as possible.

ORDERING INFORMATION

Device	Voltage Option	Marking	Package	Shipping†
NCP716BSN300T1G	3.0 V	6AA	TSOP-5 (Pb-Free)	3000 / Tape & Reel
NCP716BSN330T1G	3.3 V	6AC	TSOP-5 (Pb-Free)	3000 / Tape & Reel
NCP716BSN500T1G	5.0 V	6AV	TSOP-5 (Pb-Free)	3000 / Tape & Reel

† For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

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REVISION HISTORY

Revision	Description of Changes	Date
2	Rebranded the Data Sheet to **onsemi** format.	2/4/2026

This document has undergone updates prior to the inclusion of this revision history table. The changes tracked here only reflect updates made on the noted approval dates.

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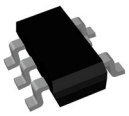
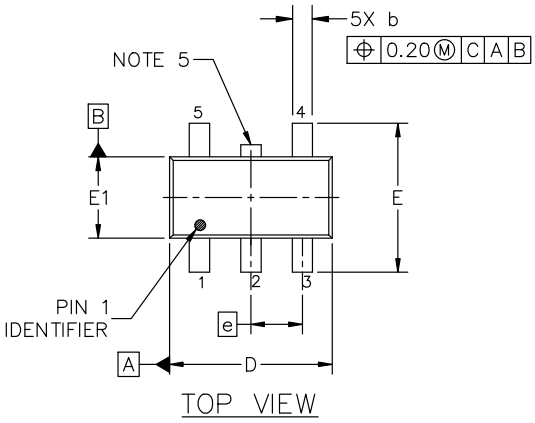
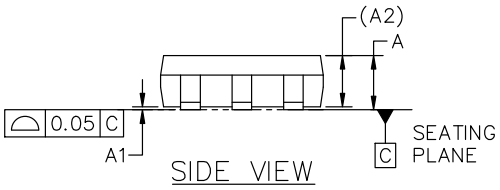


TSOP−5 3.00x1.50x0.95, 0.95P
CASE 483
ISSUE P

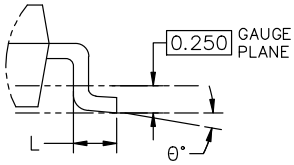
DATE 01 APR 2024



TOP VIEW



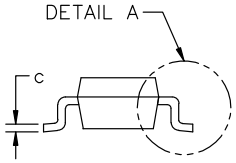
SIDE VIEW



DETAIL "A"
SCALE 2:1

NOTES:

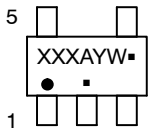
1. DIMENSIONING AND TOLERANCING CONFORM TO ASME Y14.5−2018.
2. ALL DIMENSION ARE IN MILLIMETERS (ANGLES IN DEGREES).
3. MAXIMUM LEAD THICKNESS INCLUDES LEAD FINISH THICKNESS. MINIMUM LEAD THICKNESS IS THE MINIMUM THICKNESS OF BASE MATERIAL.
4. DIMENSIONS D AND E1 DO NOT INCLUDE MOLD FLASH, PROTRUSIONS OF GATE BURRS. MOLD FLASH, PROTRUSIONS, OR GATE BURRS SHALL NOT EXCEED 0.15 PER SIDE. DIMENSION D.
5. OPTIONAL CONSTRUCTION: AN ADDITIONAL TRIMMED LEAD IS ALLOWED IN THIS LOCATION. TRIMMED LEAD NOT TO EXTEND MORE THAN 0.2 FROM BODY.



END VIEW

DIM	MILLIMETERS		
	MIN.	NOM.	MAX.
A	0.900	1.000	1.100
A1	0.010	0.055	0.100
A2		0.950 REF.	
b	0.250	0.375	0.500
c	0.100	0.180	0.260
D	2.850	3.000	3.150
E	2.500	2.750	3.000
E1	1.350	1.500	1.650
e		0.950 BSC	
L	0.200	0.400	0.600
θ	0°	5°	10°

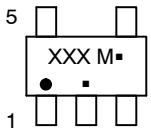
GENERIC
MARKING DIAGRAM*



Analog

XXX = Specific Device Code
A = Assembly Location
Y = Year
W = Work Week
▪ = Pb−Free Package

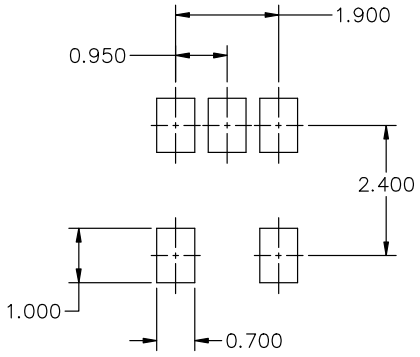
(Note: Microdot may be in either location)



Discrete/Logic

XXX = Specific Device Code
M = Date Code
▪ = Pb−Free Package

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, "G" or microdot "▪", may or may not be present. Some products may not follow the Generic Marking.



RECOMMENDED MOUNTING FOOTPRINT*

* FOR ADDITIONAL INFORMATION ON OUR Pb−FREE STRATEGY AND SOLDERING DETAILS, PLEASE DOWNLOAD THE ON SEMICONDUCTOR SOLDERING AND MOUNTING TECHNIQUES REFERENCE MANUAL, SOLDERRM/D.

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