200 mA, Ultra-Low Quiescent Current, I_Q 12 μA, Ultra-Low Noise, Low Dropout Regulator

NCP752



XDFN6
CASE 711AE



TSOP−5
CASE 483

Noise sensitive RF applications such as Power Amplifiers in satellite radios, infotainment equipment, and precision instrumentation require very clean power supplies. The NCP752 is 200 mA LDO that provides the engineer with a very stable, accurate voltage with ultra low noise and very high Power Supply Rejection Ratio (PSRR) suitable for RF applications. The device doesn't require any additional noise bypass capacitor to achieve ultra low noise performance. In order to optimize performance for battery operated portable applications, the NCP752 employs the Auto Low−Power Function for Ultra Low Quiescent Current consumption.

Features

- Operating Input Voltage Range: 2.0 V to 5.5 V
- Available in Fixed Voltage Options: 0.8 to 3.5 V
  Contact Factory for Other Voltage Options
- Ultra Low Quiescent Current of Typ. 12 μA
- Ultra Low Noise: 11.5 μV_{RMS} from 100 Hz to 100 kHz
- Very Low Dropout: 130 mV Typical at 200 mA
- ±2% Accuracy Over Load/Line/Temperature
- High PSRR: 68 dB at 1 kHz
- Power Good Output
- Internal Soft−Start to Limit the Inrush Current
- Thermal Shutdown and Current Limit Protections
- Stable with a 1 μF Ceramic Output Capacitor
- Available in TSOP−5 and XDFN 1.5 x 1.5 mm Package
- Active Output Discharge for Fast Turn−Off
- These are Pb−Free Devices

Typical Applications

- PDAs, Mobile phones, GPS, Smartphones
- Wireless Handsets, Wireless LAN, Bluetooth®, Zigbee®
- Portable Medical and Other Battery Powered Devices

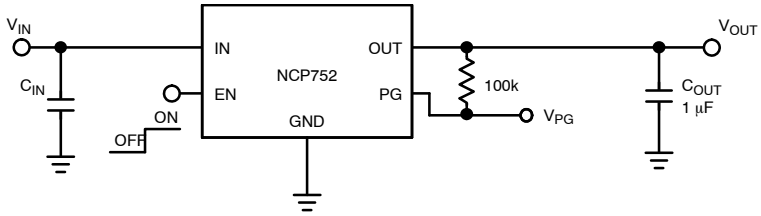
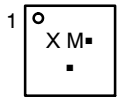
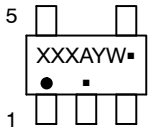


Figure 1. Typical Application Schematic

MARKING DIAGRAMS



XDFN6

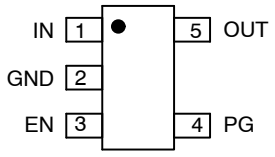


TSOP−5

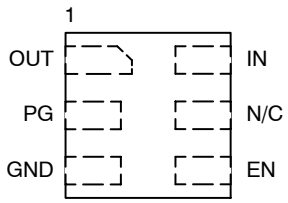
XXX = Specific Device Code
A = Assembly Location
M = Date Code
Y = Year
W = Work Week
▪ = Pb−Free Package

(Note: Microdot may be in either location)

PIN CONNECTIONS



TSOP−5



XDFN6
(Top view)

ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 19 of this data sheet.

NOTE: Some of the devices on this data sheet have been **DISCONTINUED**. Please refer to the table on page 19.

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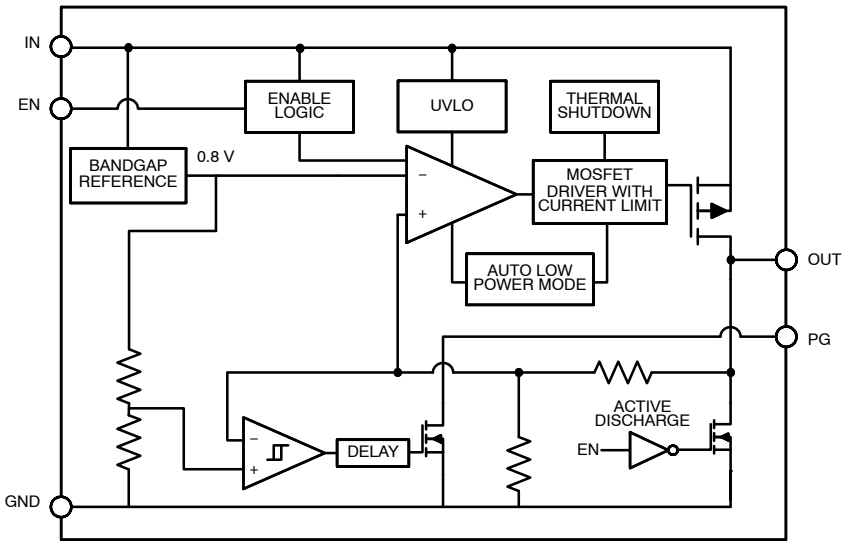


Figure 2. Simplified Schematic Block Diagram

PIN FUNCTION DESCRIPTION

Pin No. XDFN 6	Pin No. TSOP−5	Pin Name	Description
1	5	OUT	Regulated output voltage pin. A small 1 μF ceramic capacitor is needed from this pin to ground to assure stability.
2	4	PG	Open Drain Power Good Output.
3	2	GND	Power supply ground. Connected to the die through the lead frame. Soldered to the copper plane allows for effective heat dissipation.
4	3	EN	Enable pin. Driving EN over 0.9 V turns on the regulator. Driving EN below 0.4 V puts the regulator into shutdown mode.
5		N/C	Not connected. This pin can be tied to ground to improve thermal dissipation.
6	1	IN	Input pin. A small capacitor is needed from this pin to ground to assure stability.

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ABSOLUTE MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Input Voltage (Note 1)	V_{IN}	−0.3 V to 6 V	V
Output Voltage	V_{OUT}	−0.3 V to V_{IN} + 0.3 V	V
Enable Input	V_{EN}	−0.3 V to V_{IN} + 0.3 V	V
Power Good Output	V_{PG}	−0.3 V to V_{IN} + 0.3 V	V
Output Short Circuit Duration	t_{SC}	Indefinite	s
Maximum Junction Temperature	$T_{J(MAX)}$	150	°C
Storage Temperature	T_{STG}	−55 to 150	°C
ESD Capability, Human Body Model (Note 2)	ESD_{HBM}	2000	V
ESD Capability, Machine Model (Note 2)	ESD_{MM}	200	V

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. Refer to ELECTRICAL CHARACTERISTIS and APPLICATION INFORMATION for Safe Operating Area.
2. This device series incorporates ESD protection and is tested by the following methods:
   ESD Human Body Model tested per JESD22−A114
   ESD Machine Model tested per JESD22−A115
   Latchup Current Maximum Rating tested per JEDEC standard: JESD78.

THERMAL CHARACTERISTICS (Note 3)

Rating	Symbol	Value	Unit
Thermal Characteristics, TSOP−5, Thermal Resistance, Junction−to−Air	$R_{\theta JA}$	224	°C/W
Thermal Characteristics, XDFN6 1.5x1.5mm Thermal Resistance, Junction−to−Air	$R_{\theta JA}$	149	°C/W

3. Single component mounted on 1 oz FR 4 PCB with 645 mm^2 cu area.

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ELECTRICAL CHARACTERISTICS

$-40°C \le T_J \le 125$ °C; $V_{IN} = V_{OUT(NOM)} + 0.3$ V or 2.0 V, whichever is greater; I_{OUT} = 10 mA, $C_{IN} = C_{OUT}$ = 1 μF, unless otherwise noted. Typical values are at T_J = +25°C (Note 4)

Parameter	Test Conditions	Symbol	Min	Typ	Max	Unit
Operating Input Voltage		V_{IN}	2.0		5.5	V
Undervoltage lock−out	V_{IN} rising	UVLO	1.2	1.5	1.9	V
Output Voltage Accuracy	$V_{OUT} + 0.3$ V ≤ V_{IN} ≤ 5.5 V, I_{OUT} = 0 − 200 mA	V_{OUT}	−2		+2	%
Line Regulation	$V_{OUT} + 0.3$ V ≤ V_{IN} ≤ 5.5 V, I_{OUT} = 10 mA	Reg_{LINE}		300		μV/V
Load Regulation	I_{OUT} = 0 mA to 200 mA	Reg_{LOAD}		20		μV/mA
Load Transient	I_{OUT} = 1 mA to 200 mA or 200 mA to 1 mA in 1 μs, C_{OUT} = 1 μs	$Tran_{LOAD}$		±90		mV
Dropout voltage (Note 5)	I_{OUT} = 200 mA, $V_{OUT(nom)}$ = 2.5 V	V_{DO}		130	200	mV
Output Current Limit	V_{OUT} = 90% $V_{OUT(nom)}$	I_{CL}	210	400	550	mA
Quiescent current	I_{OUT} = 0 mA	I_Q		12	25	μA
Ground current	I_{OUT} = 200 mA	I_{GND}		150		μA
Shutdown current	$V_{EN} \le 0.4$ V, T_J = +25°C	I_{DIS}		0.12		μA
	$V_{EN} \le 0$ V, V_{IN} = 5.5 V			0.55	1	μA
EN Pin Threshold Voltage High Threshold Low Threshold	 V_{EN} Voltage increasing V_{EN} Voltage decreasing	 V_{EN_HI} V_{EN_LO}	 0.9		 0.4	V
EN Pin Input Current	V_{EN} = 5.5 V	I_{EN}		100	500	nA
Turn−on Time	C_{OUT} = 1.0 μF, I_{OUT} = 0 mA to 200 mA From V_{OUT} = 10% $V_{OUT(NOM)}$ to 95% $V_{OUT(NOM)}$	t_{ON1}		80		μs
	C_{OUT} = 1.0 μF, I_{OUT} = 0 mA to 200 mA From assertion of the EN to 95% $V_{OUT(NOM)}$	t_{ON2}		200		μs
Power Supply Rejection Ratio	V_{IN} = 3 V, V_{OUT} = 2.5 V, I_{OUT} = 150 mA; f = 100 Hz / f = 1 kHz / f = 10 kHz	PSRR		70 68 53		dB
Output Noise Voltage	V_{OUT} = 2.5 V, V_{IN} = 3 V, I_{OUT} = 200 mA f = 100 Hz to 100 kHz	V_N		11.5		μV_{rms}
Thermal Shutdown Temperature	Temperature increasing from T_J = +25°C	T_{SD}		160		°C
Thermal Shutdown Hysteresis	Temperature falling from T_{SD}	T_{SDH}	−	20	−	°C

POWER GOOD OUTPUT

PG Threshold Voltage	V_{OUT} decreasing	V_{PG-}	90	92	94	$\%V_{OUT}$
PG Threshold Voltage	V_{OUT} increasing	V_{PG+}	92	94	96	$\%V_{OUT}$
Hysteresis	Measured on V_{OUT}			2		$\%V_{OUT}$
PG Output Low Voltage	$I_{OUT(PG)}$ = 1 mA			0.1	0.4	V
PG Pin Leakage	$V_{IN} = V_{OUT(NOM)} + 0.3$ V			0.002	1	μA
PG time−out delay	NCP752A NCP752B	t_{RD}		2 200		μs
PG reaction time	NCP752A NCP752B	t_{RR}		2 5		μs

4. Performance guaranteed over the indicated operating temperature range by design and/or characterization production tested at $T_J = T_A$ = 25°C. Low duty cycle pulse techniques are used during testing to maintain the junction temperature as close to ambient as possible.
5. Characterized when V_{OUT} falls 100 mV below the regulated voltage at $V_{IN} = V_{OUT(NOM)} + 0.3$ V.

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TYPICAL CHARACTERISTICS

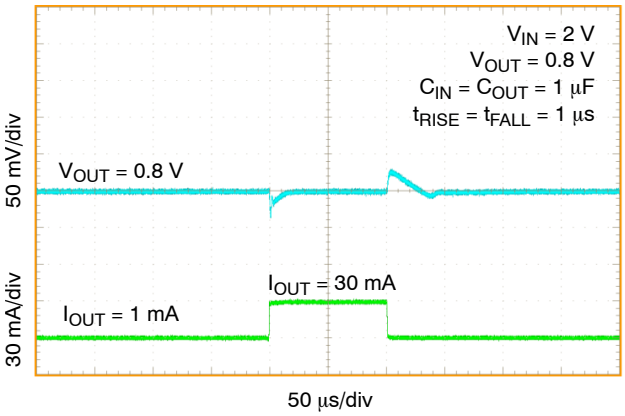


Figure 3. Load Transient Response, 1 mA – 30 mA NCP752A/B, V_{OUT} = 0.8 V

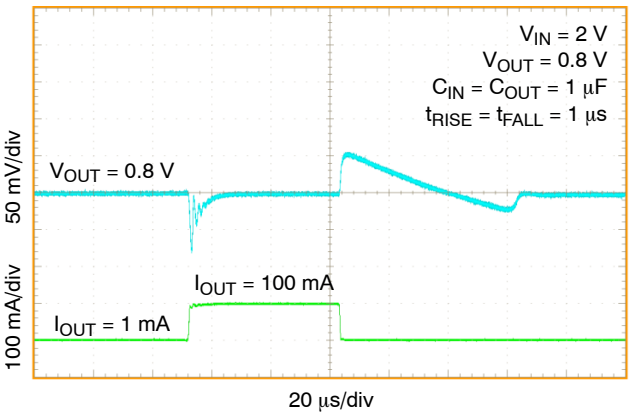


Figure 4. Load Transient Response, 1 mA – 100 mA NCP752A/B, V_{OUT} = 0.8 V

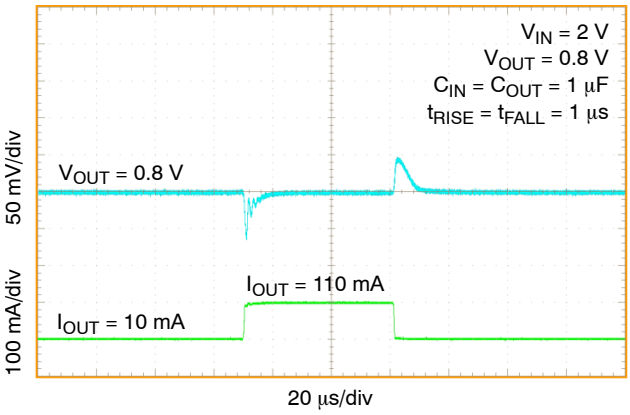


Figure 5. Load Transient Response, 10 mA – 110 mA NCP752A/B, V_{OUT} = 0.8 V

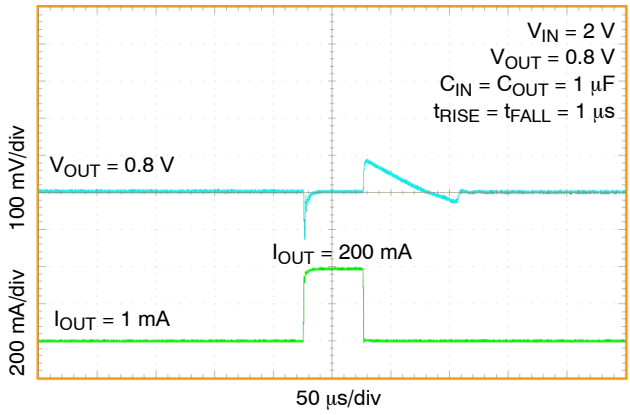


Figure 6. Load Transient Response, 1 mA – 200 mA NCP752A/B, V_{OUT} = 0.8 V

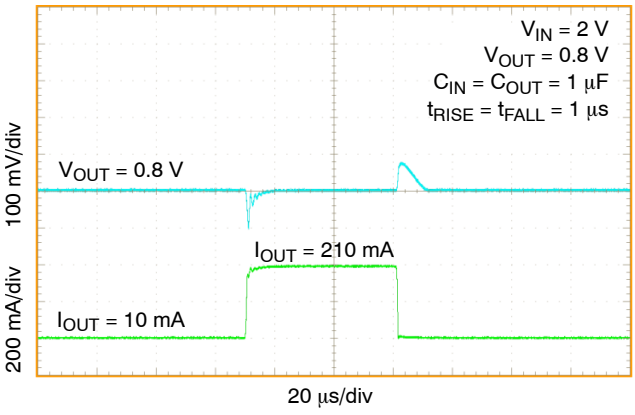


Figure 7. Load Transient Response, 10 mA – 210 mA NCP752A/B, V_{OUT} = 0.8 V

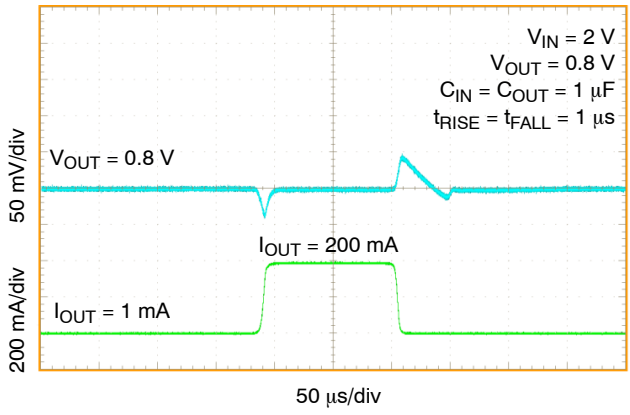


Figure 8. Load Transient Response, 1 mA – 100 mA NCP752A/B, V_{OUT} = 0.8 V

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TYPICAL CHARACTERISTICS

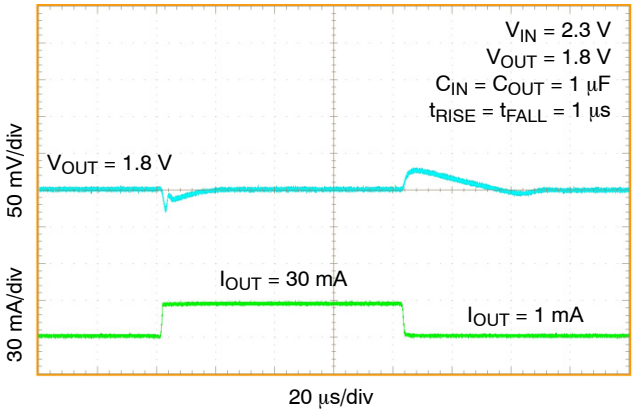


Figure 9. Load Transient Response, 1 mA – 30 mA NCP752A/B, V_{OUT} = 1.8 V

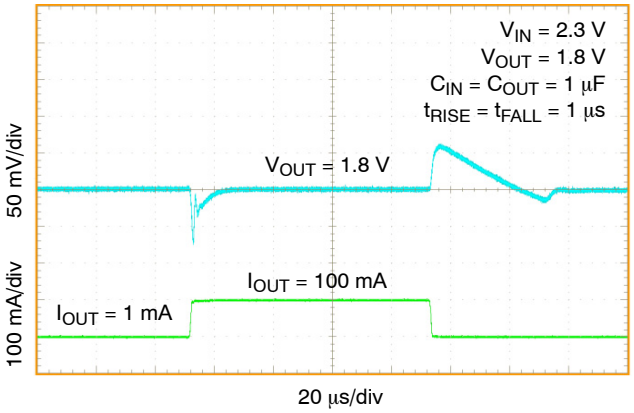


Figure 10. Load Transient Response, 1 mA – 100 mA NCP752A/B, V_{OUT} = 1.8 V

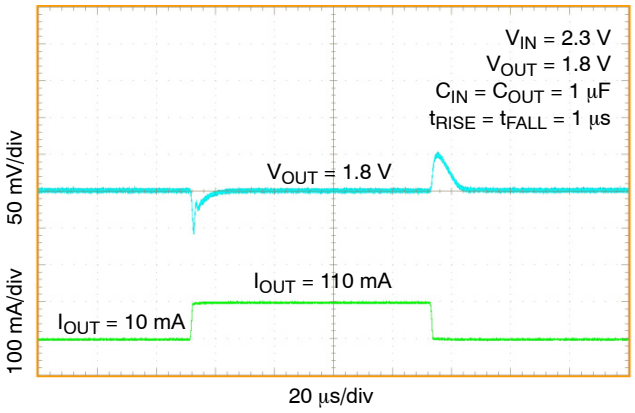


Figure 11. Load Transient Response, 1 mA – 30 mA NCP752A/B, V_{OUT} = 1.8 V

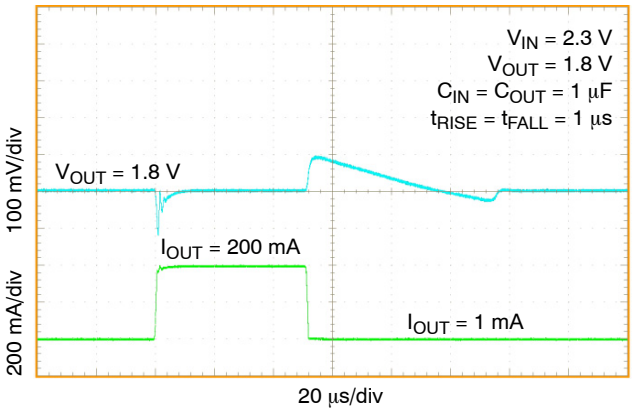


Figure 12. Load Transient Response, 1 mA – 200 mA NCP752A/B, V_{OUT} = 1.8 V

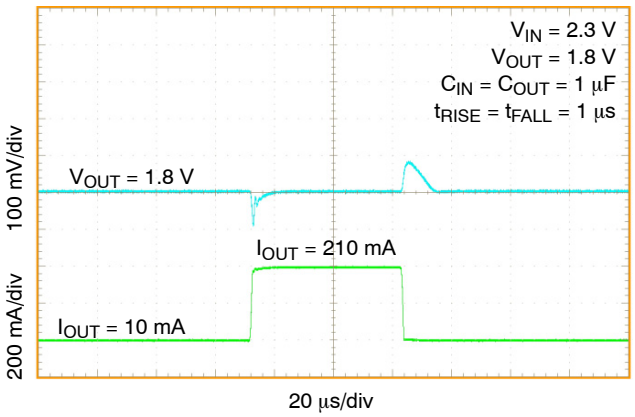


Figure 13. Load Transient Response, 10 mA – 210 mA NCP752A/B, V_{OUT} = 1.8 V

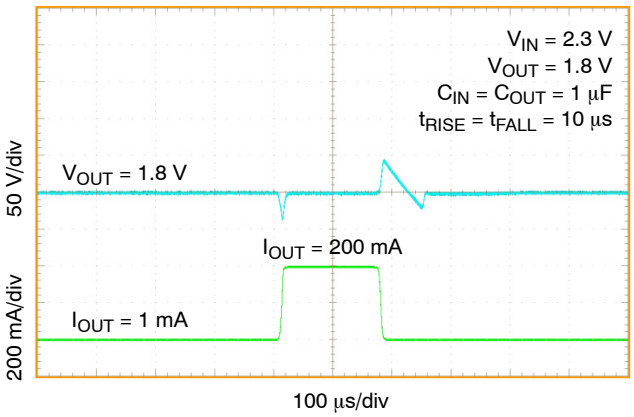


Figure 14. Load Transient Response, 1 mA – 200 mA NCP752A/B, V_{OUT} = 1.8 V

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TYPICAL CHARACTERISTICS

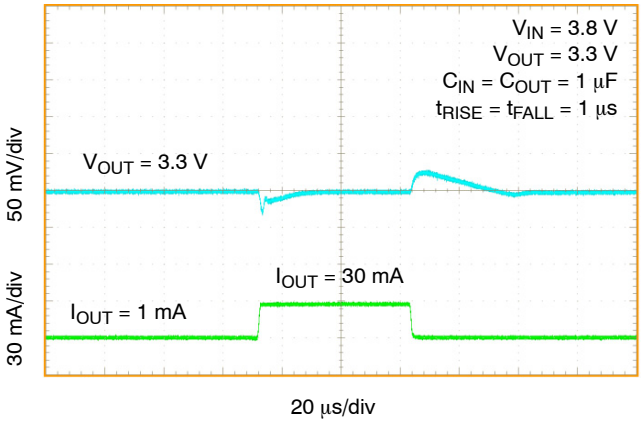


Figure 15. Load Transient Response, 1 mA – 30 mA NCP752A/B, V_{OUT} = 3.3 V

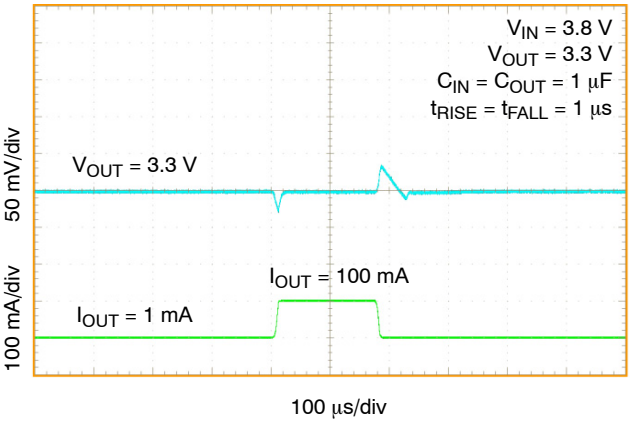


Figure 16. Load Transient Response, 1 mA – 100 mA NCP752A/B, V_{OUT} = 3.3 V

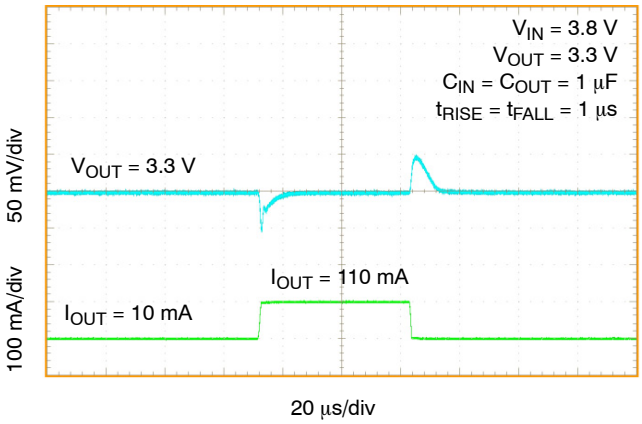


Figure 17. Load Transient Response, 10 mA – 110 mA NCP752A/B, V_{OUT} = 3.3 V

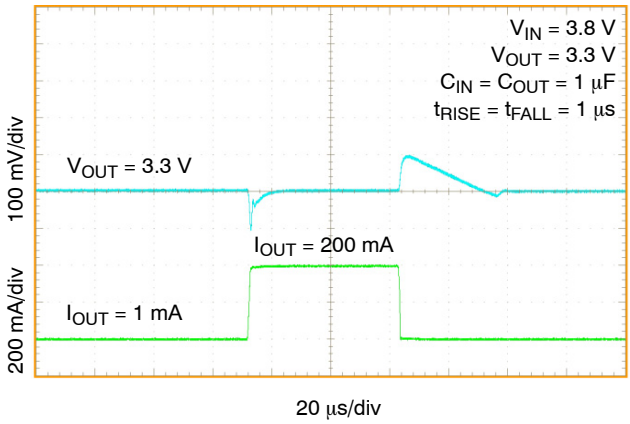


Figure 18. Load Transient Response, 1 mA – 200 mA NCP752A/B, V_{OUT} = 3.3 V

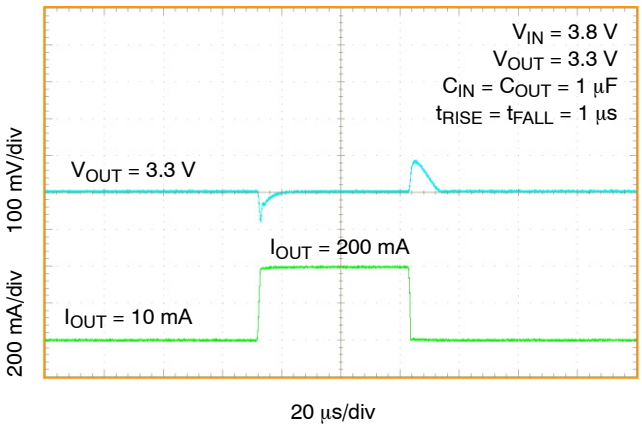


Figure 19. Load Transient Response, 10 mA – 200 mA NCP752A/B, V_{OUT} = 3.3 V

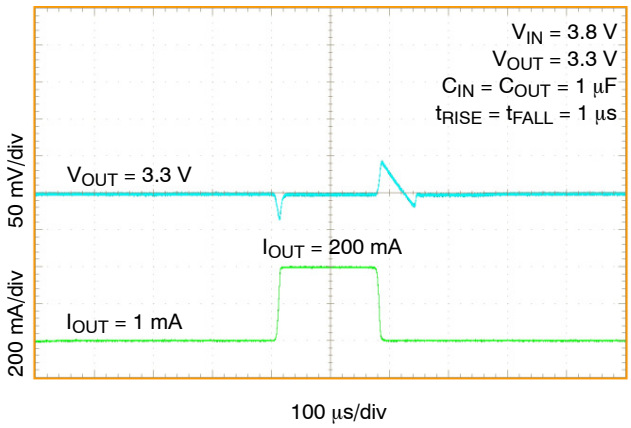


Figure 20. Load Transient Response, 1 mA – 200 mA NCP752A/B, V_{OUT} = 3.3 V

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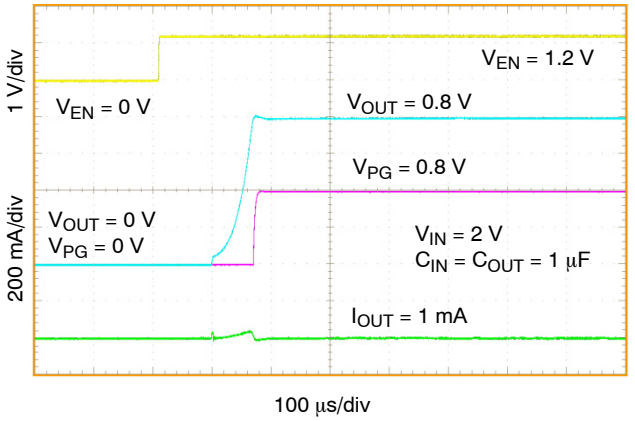


Figure 21. Turn−On Response After Asserting EN NCP752A, V_{OUT} = 0.8 V

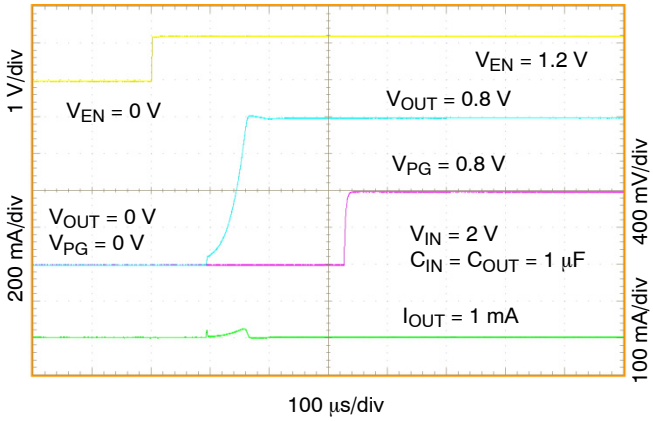


Figure 22. Turn−On Response After Asserting EN NCP752B, V_{OUT} = 0.8 V

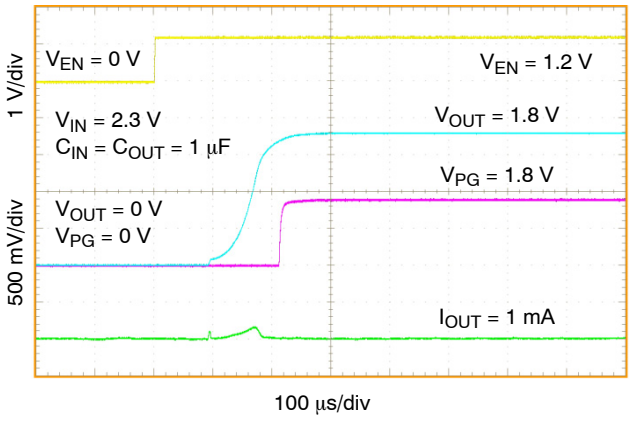


Figure 23. Turn−On Response After Asserting EN NCP752A, V_{OUT} = 1.8 V

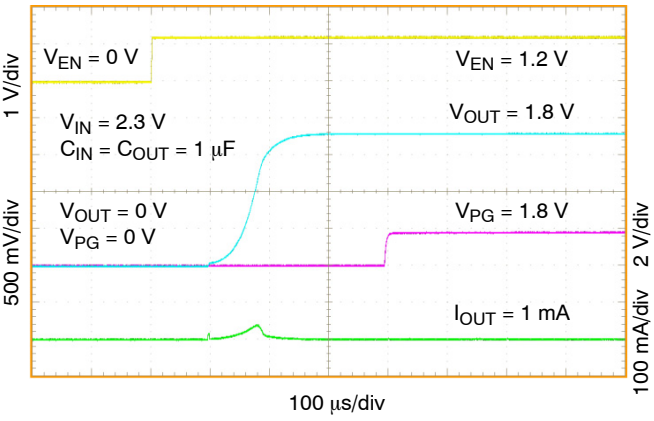


Figure 24. Turn−On Response After Asserting EN NCP752B, V_{OUT} = 1.8 V

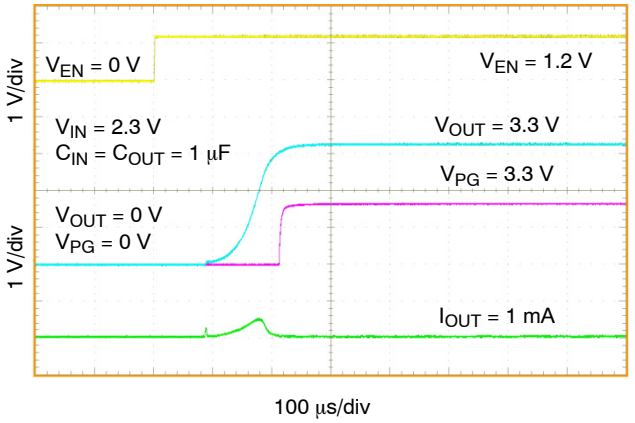


Figure 25. Turn−On Response After Asserting EN NCP752A, V_{OUT} = 3.3 V

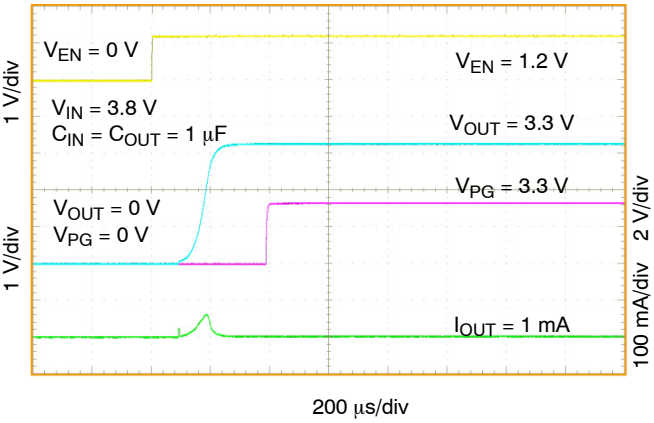


Figure 26. Turn−On Response After Asserting EN NCP752B, V_{OUT} = 3.3 V

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TYPICAL CHARACTERISTICS

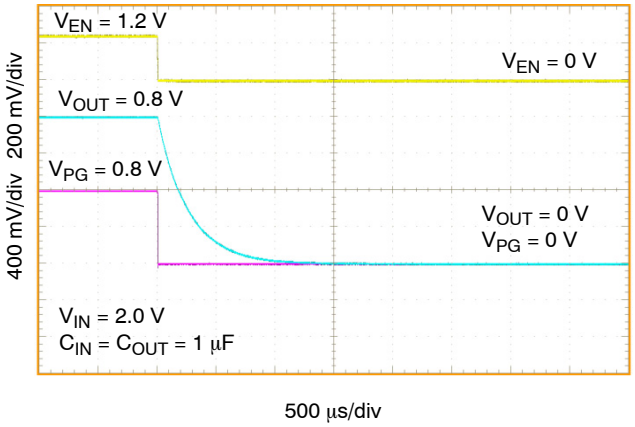


Figure 27. Turn−Off Response After De−asserting EN NCP752A/B, V_{OUT} = 0.8 V

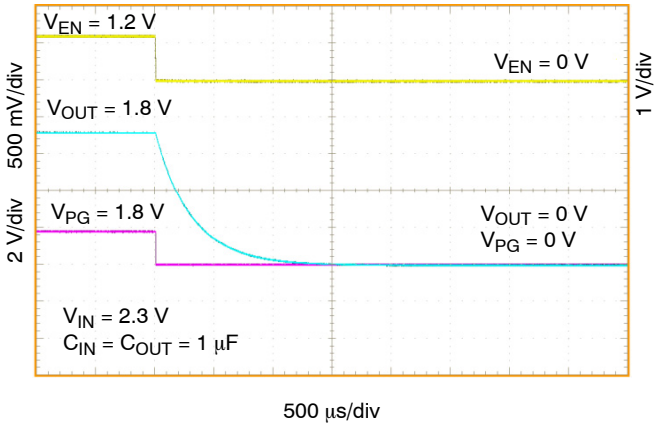


Figure 28. Turn−Off Response After De−asserting EN NCP752A/B, V_{OUT} = 1.8 V

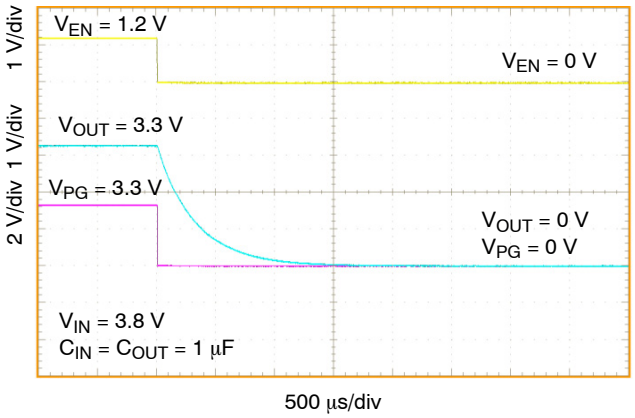


Figure 29. Turn−Off Response After De−asserting EN NCP752A/B, V_{OUT} = 3.3 V

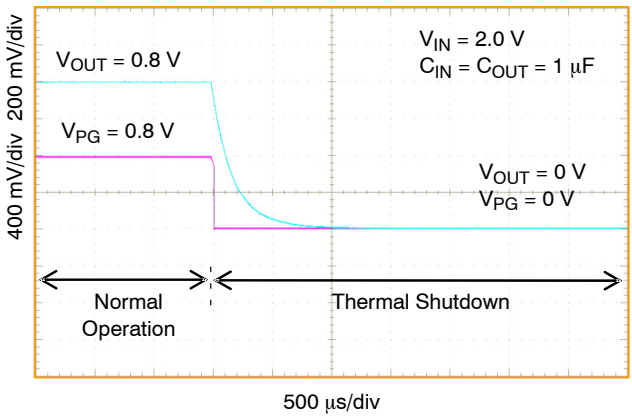


Figure 30. Turn−Off Response Due to Thermal Shutdown NCP752A/B, V_{OUT} = 0.8 V

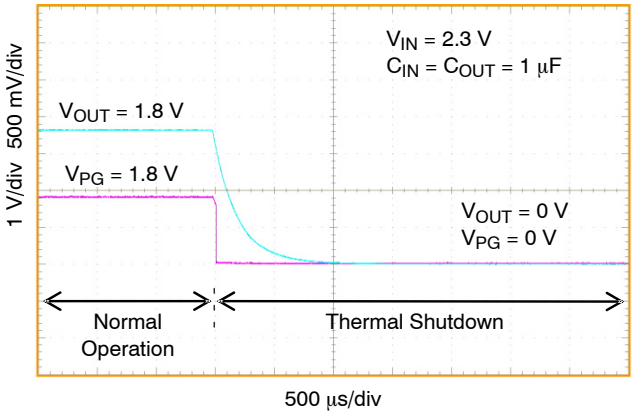


Figure 31. Turn−Off Response Due to Thermal Shutdown, V_{OUT} = 1.8 V

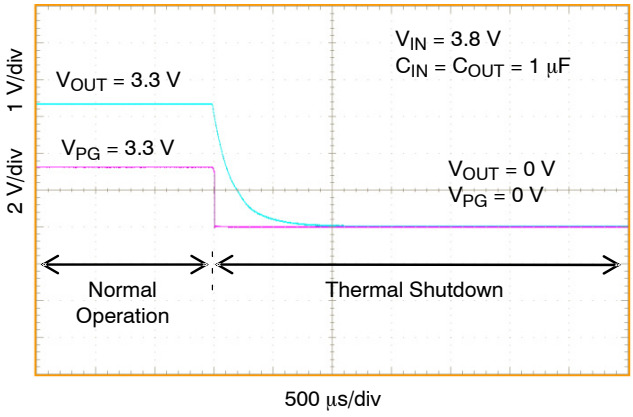


Figure 32. Turn−Off Response Due to Thermal Shutdown, V_{OUT} = 3.3 V

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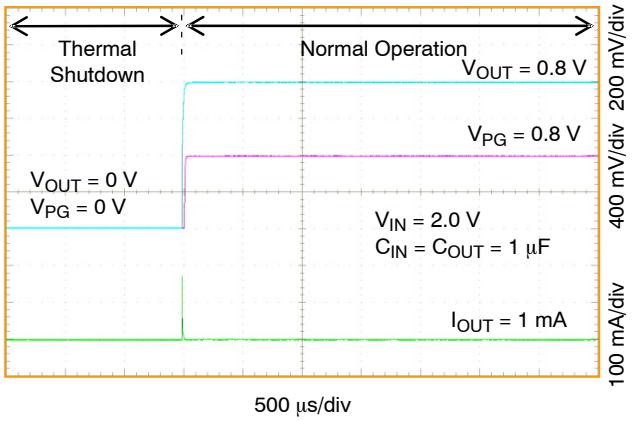


Figure 33. Recovery from Thermal Shutdown NCP752A, V_{OUT} = 0.8 V

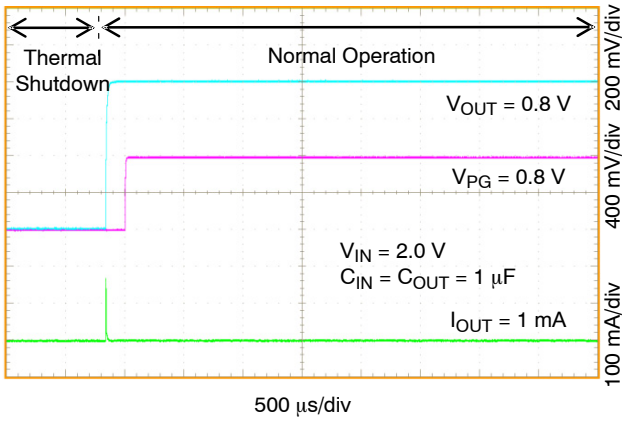


Figure 34. Recovery from Thermal Shutdown NCP752B, V_{OUT} = 0.8 V

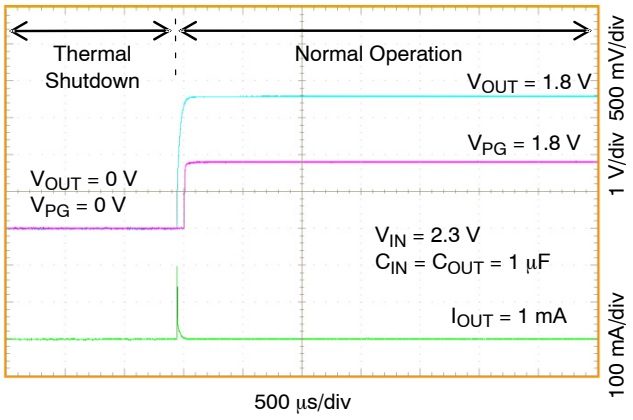


Figure 35. Recovery from Thermal Shutdown NCP752A, V_{OUT} = 1.8 V

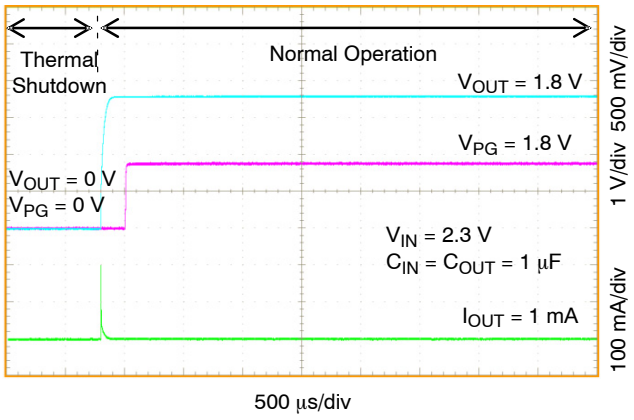


Figure 36. Recovery from Thermal Shutdown NCP752B, V_{OUT} = 1.8 V

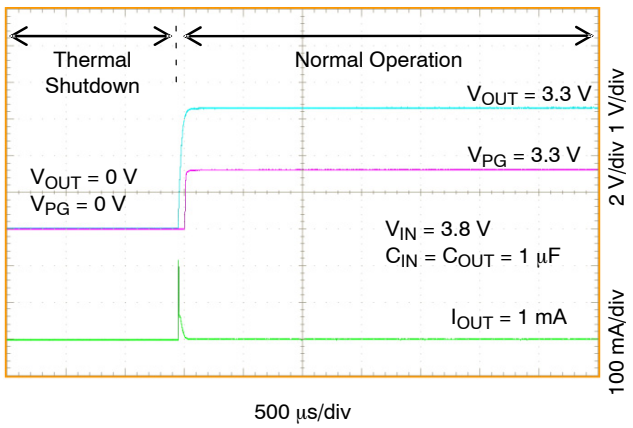


Figure 37. Recovery from Thermal Shutdown NCP752A, V_{OUT} = 3.3 V

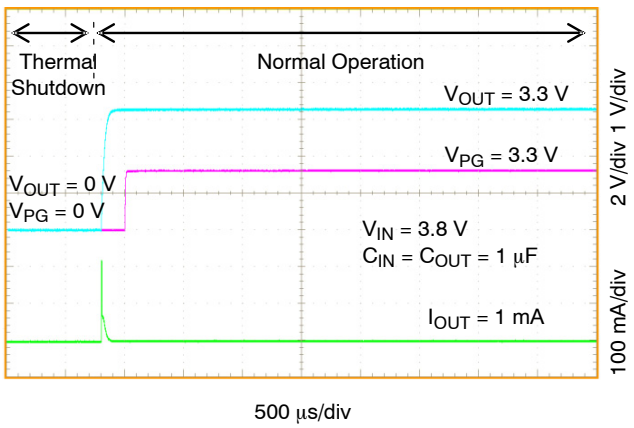


Figure 38. Recovery from Thermal Shutdown NCP752B, V_{OUT} = 3.3 V

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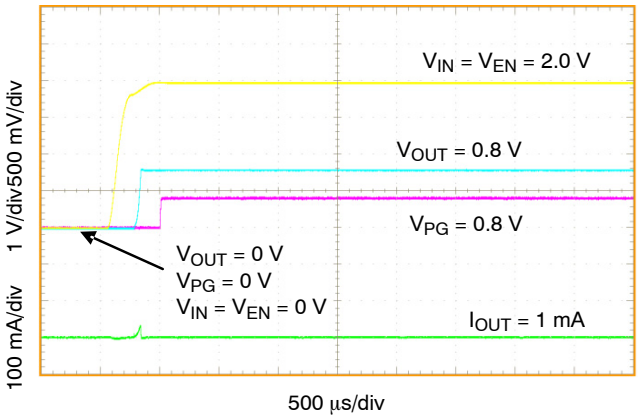


Figure 39. Input Voltage Turn−on Response NCP752B, V_{OUT} = 0.8 V

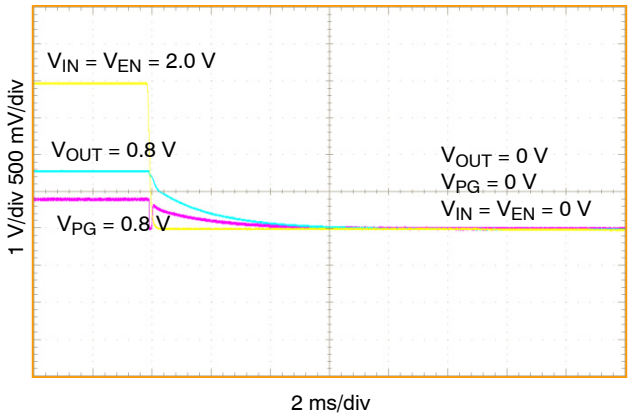


Figure 40. Input Voltage Turn−off Response NCP752B, V_{OUT} = 0.8 V

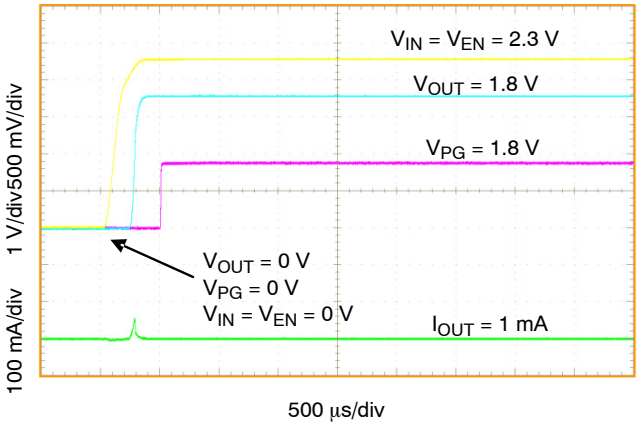


Figure 41. Input Voltage Turn−on Response NCP752B, V_{OUT} = 1.8 V

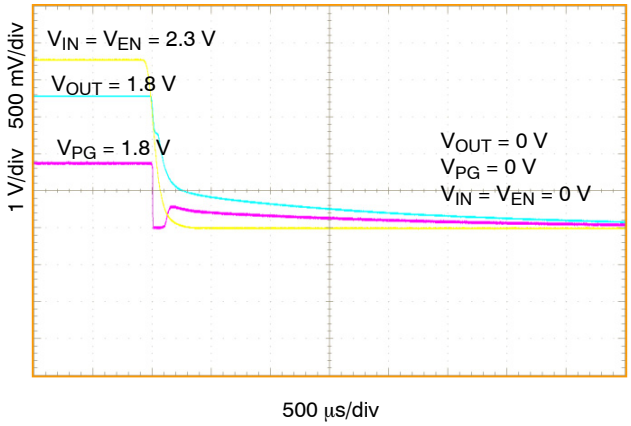


Figure 42. Input Voltage Turn−off Response NCP752B, V_{OUT} = 1.8 V

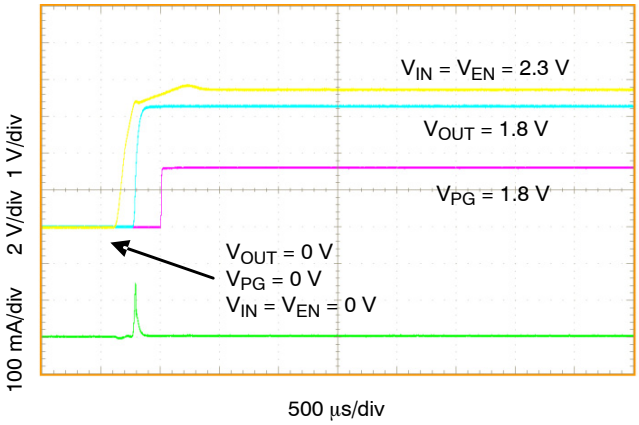


Figure 43. Input Voltage Turn−on Response NCP752B, V_{OUT} = 3.3 V

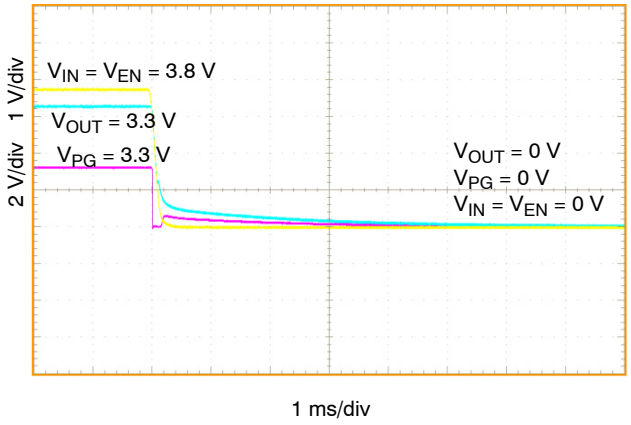


Figure 44. Input Voltage Turn−off Response NCP752B, V_{OUT} = 3.3 V

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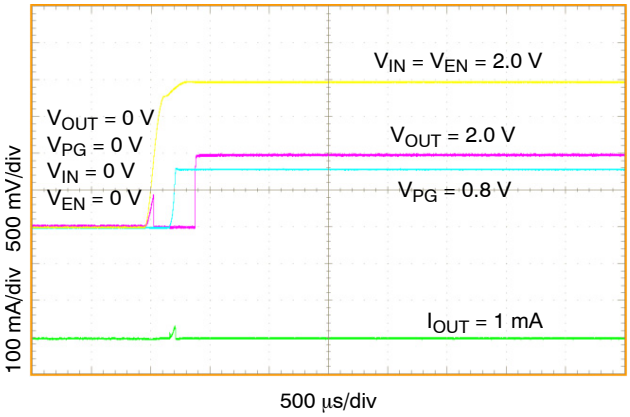


Figure 45. Input Voltage Turn−on Response NCP752B, V_{OUT} = 0.8 V

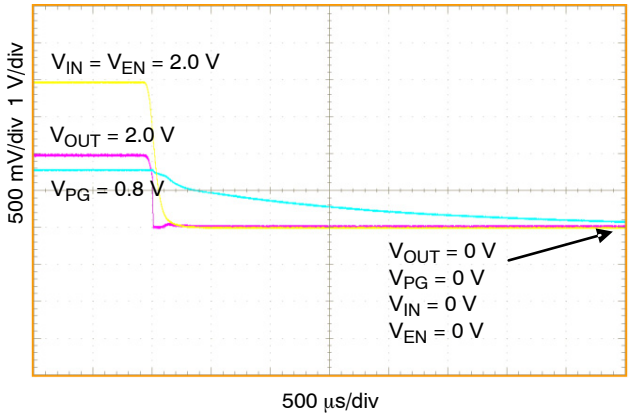


Figure 46. Input Voltage Turn−off Response NCP752B, V_{OUT} = 0.8 V

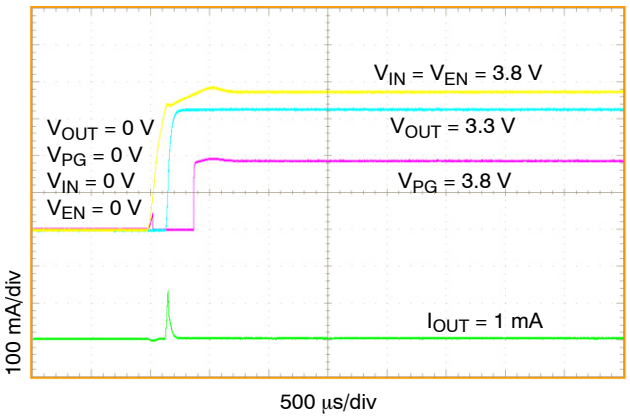


Figure 47. Input Voltage Turn−on Response NCP752B, V_{OUT} = 3.3 V

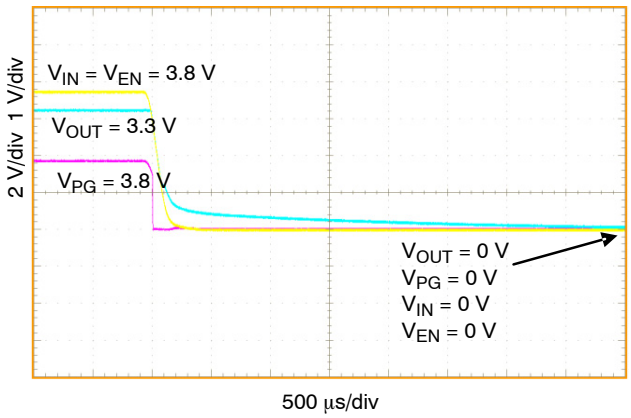


Figure 48. Input Voltage Turn−off Response NCP752B, V_{OUT} = 3.3 V

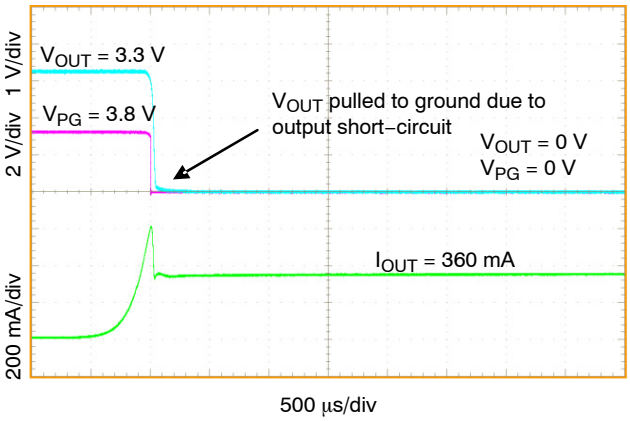


Figure 49. Short−Circuit Response NCP752B, V_{OUT} = 3.3 V

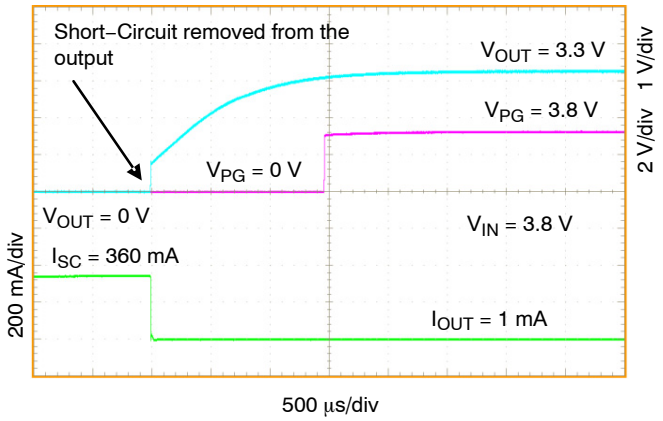


Figure 50. Recovery from Short−Circuit NCP752B, V_{OUT} = 3.3 V

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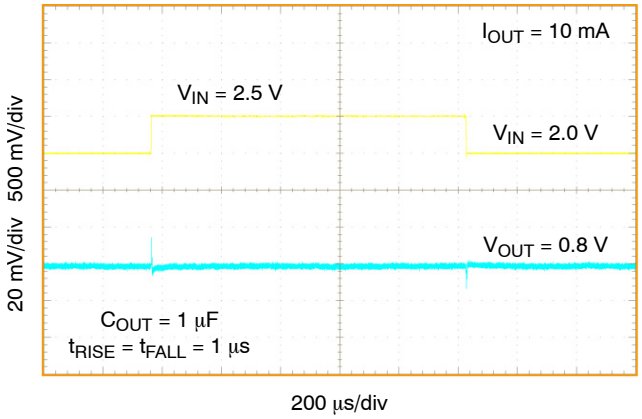


Figure 51. Line Transient 2 V – 2.5 V NCP752A/B, V_{OUT} = 0.8 V

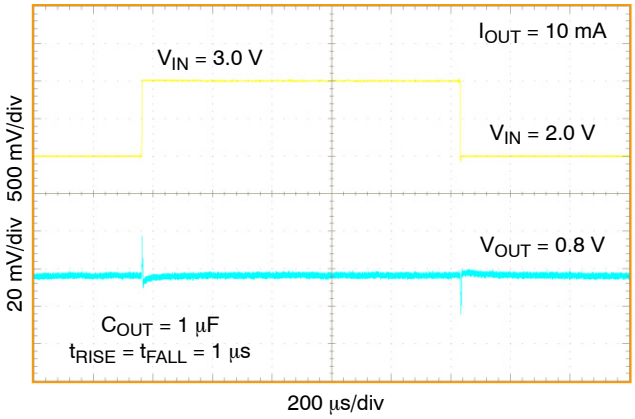


Figure 52. Line Transient 2 V – 3 V NCP752A/B, V_{OUT} = 0.8 V

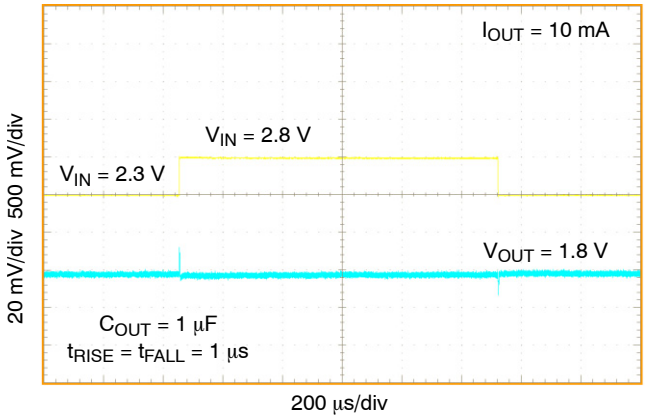


Figure 53. Line Transient 2.3 V – 2.8 V NCP752A/B, V_{OUT} = 1.8 V

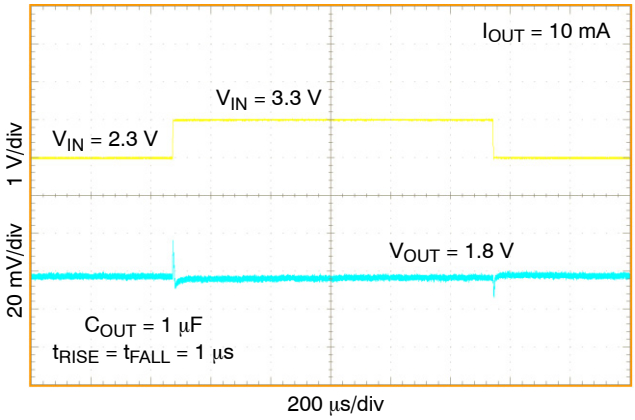


Figure 54. Line Transient 2.3 V – 3.3 V NCP752A/B, V_{OUT} = 1.8 V

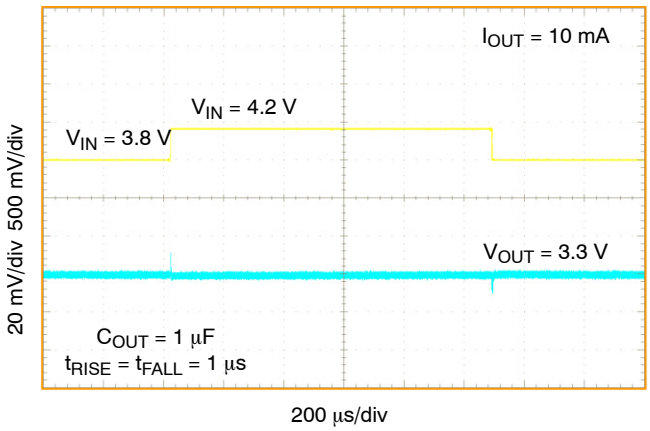


Figure 55. Line Transient 3.8 V – 4.2 V NCP752A/B, V_{OUT} = 3.3 V

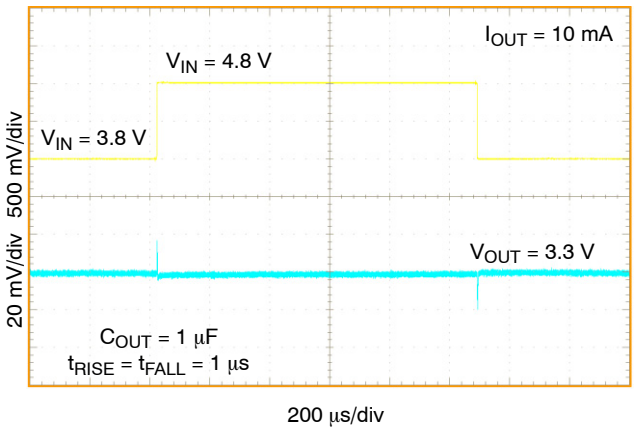


Figure 56. Line Transient 3.8 V – 4.8 V NCP752A/B, V_{OUT} = 3.3 V

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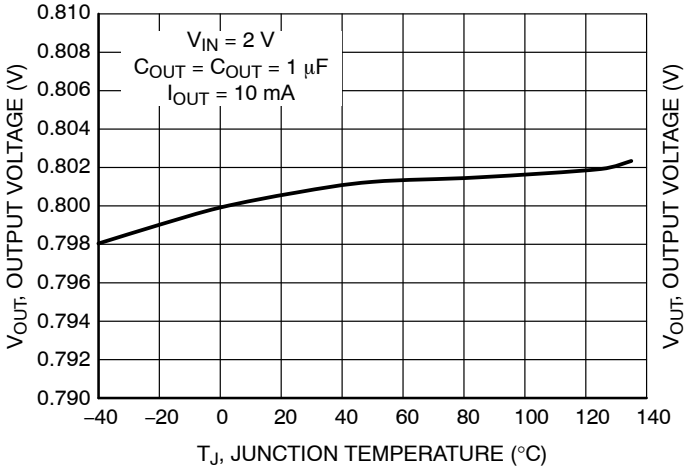


Figure 57. Output Voltage vs. Temperature
V_{OUT} = 0.8 V

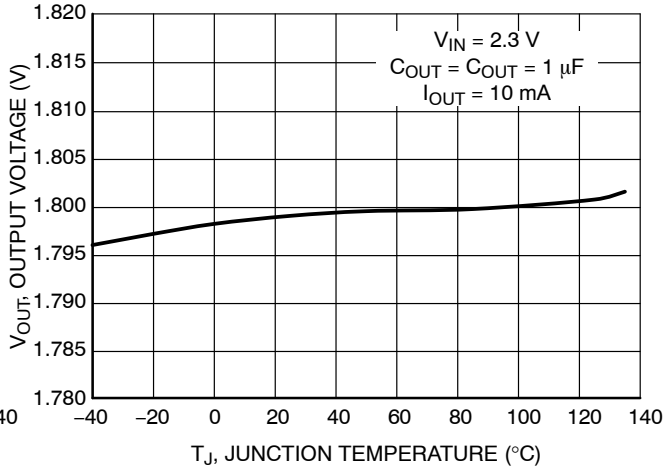


Figure 58. Output Voltage vs. Temperature
V_{OUT} = 1.8 V

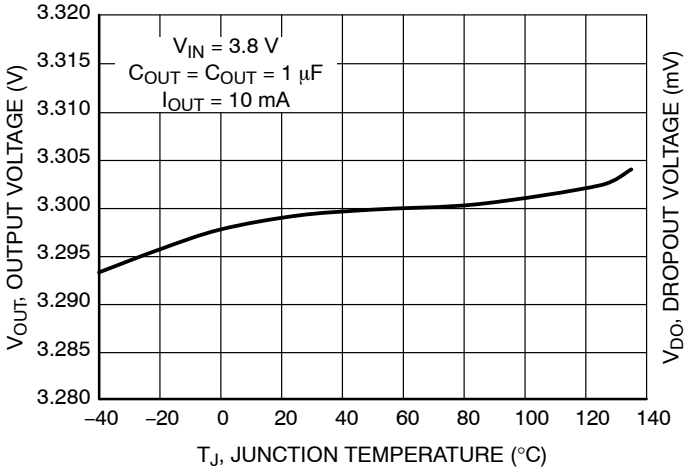


Figure 59. Output Voltage vs. Temperature
V_{OUT} = 3.3 V

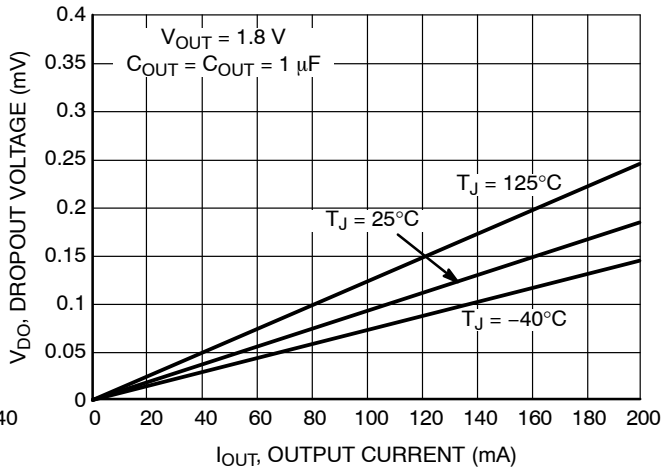


Figure 60. Dropout Voltage vs. Load Current
V_{OUT} = 1.8 V

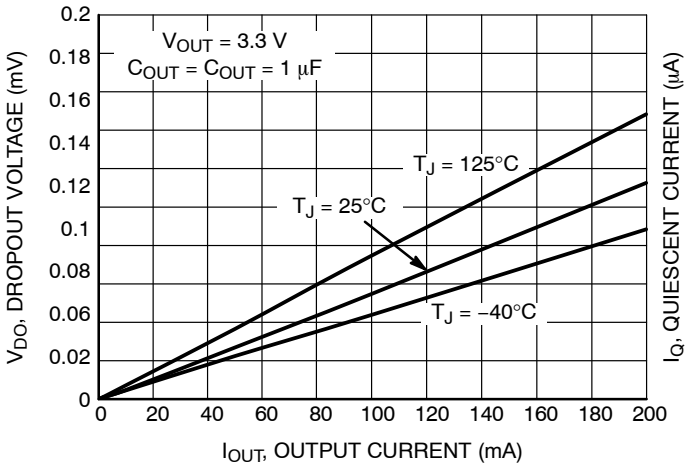


Figure 61. Dropout Voltage vs. Load Current
V_{OUT} = 3.3 V

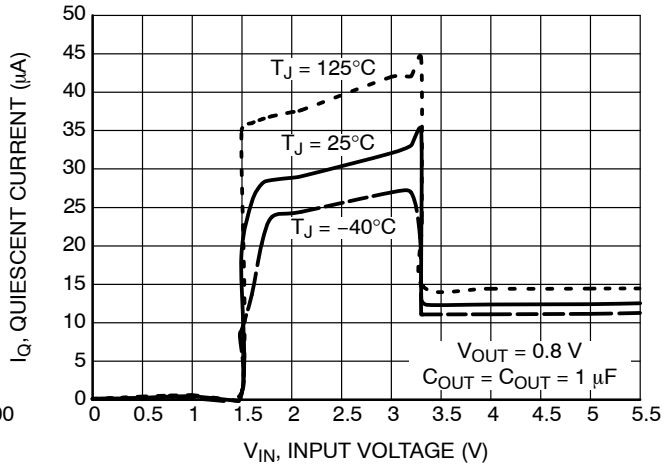


Figure 62. Quiescent Current vs. Input Voltage
V_{OUT} = 0.8 V

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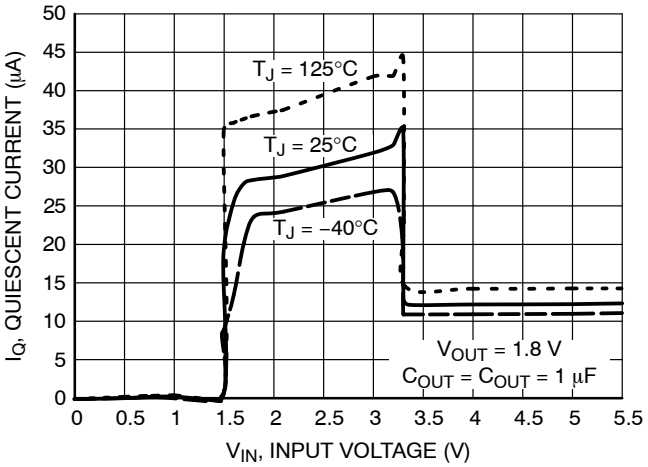


Figure 63. Quiescent Current vs. Input Voltage V_{OUT} = 1.8 V

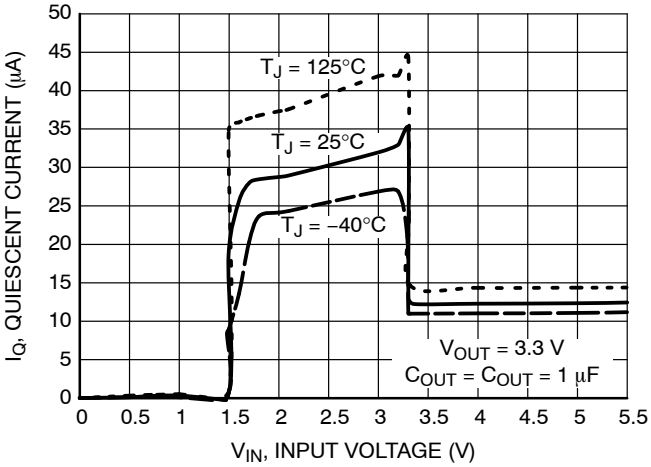


Figure 64. Quiescent Current vs. Input Voltage V_{OUT} = 3.3 V

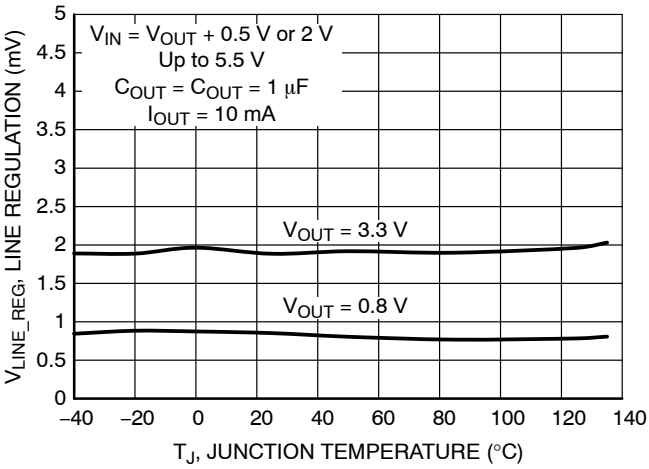


Figure 65. Line Regulation vs. Temperature

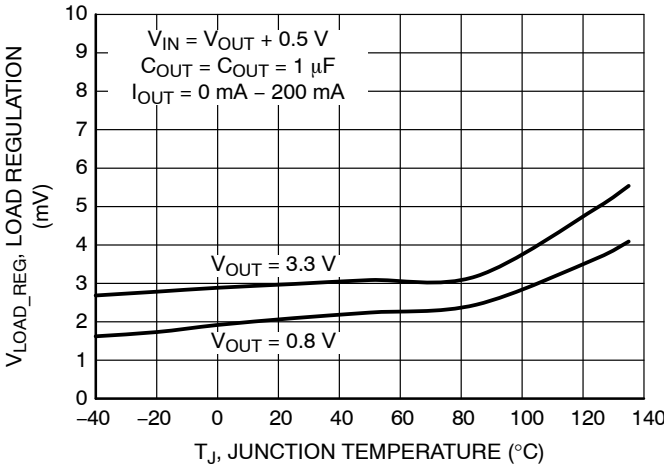


Figure 66. Load Regulation vs. Temperature

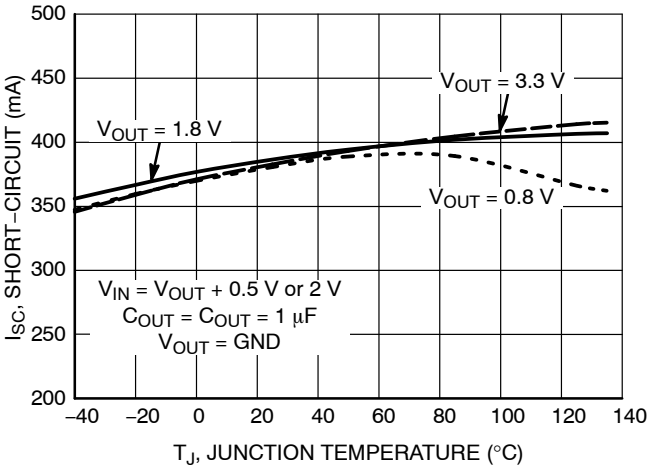


Figure 67. Short−Circuit vs. Temperature

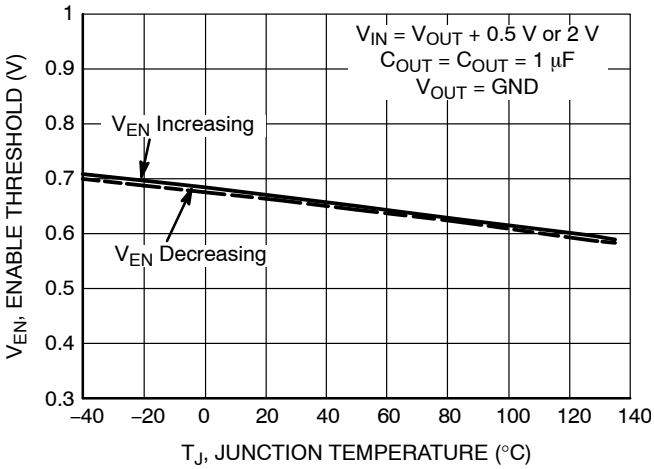


Figure 68. Enable Threshold vs. Temperature

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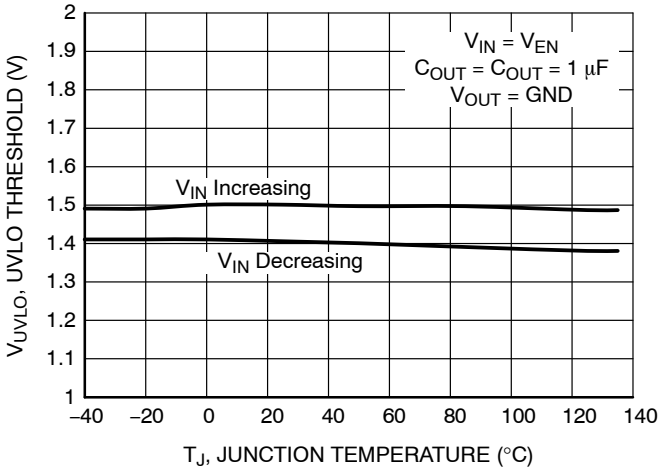


Figure 69. UVLO Threshold vs. Temperature

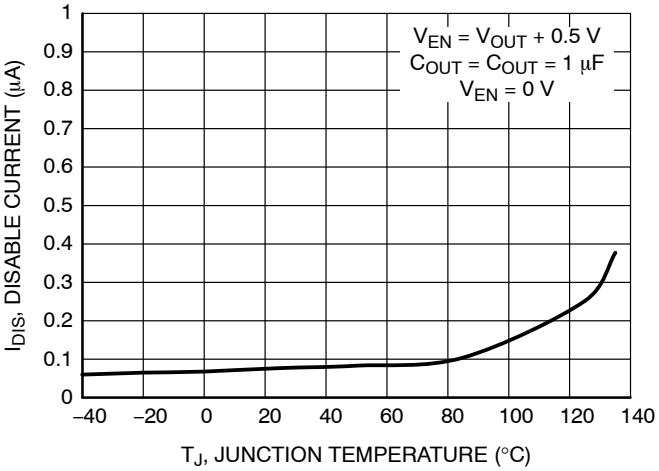


Figure 70. Disable Current vs. Temperature

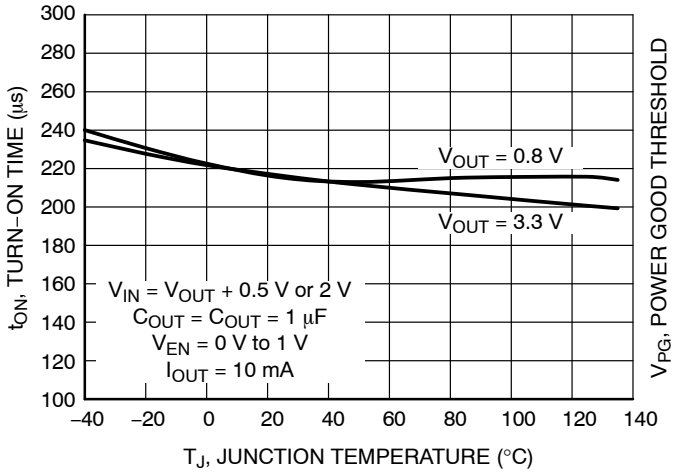


Figure 71. Turn−on Time vs. Temperature

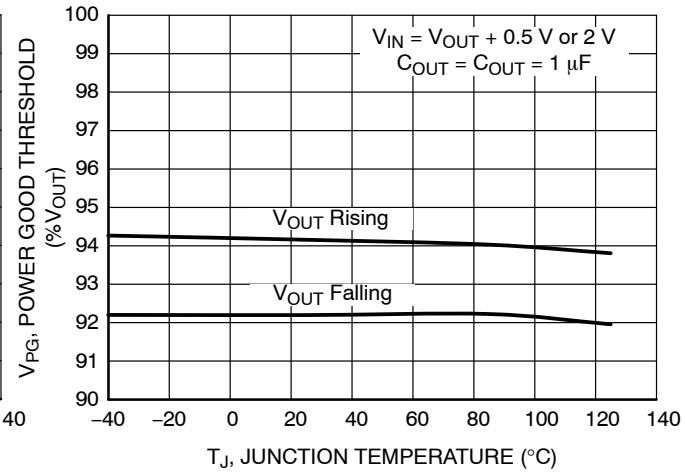


Figure 72. PG Threshold vs. Temperature

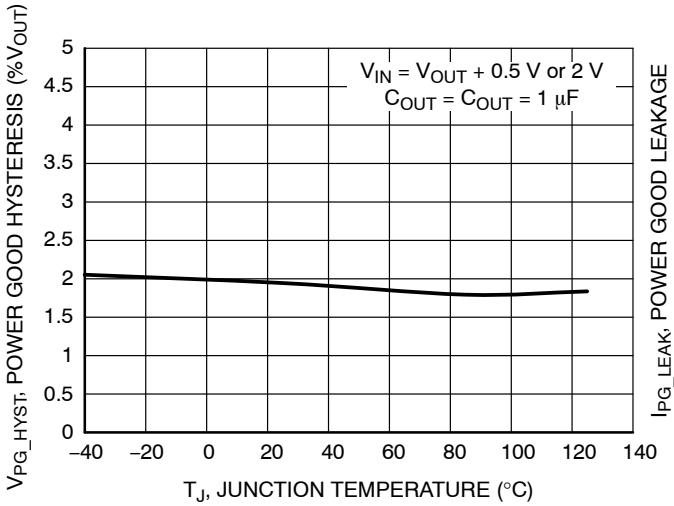


Figure 73. PG Threshold Hysteresis vs. Temperature

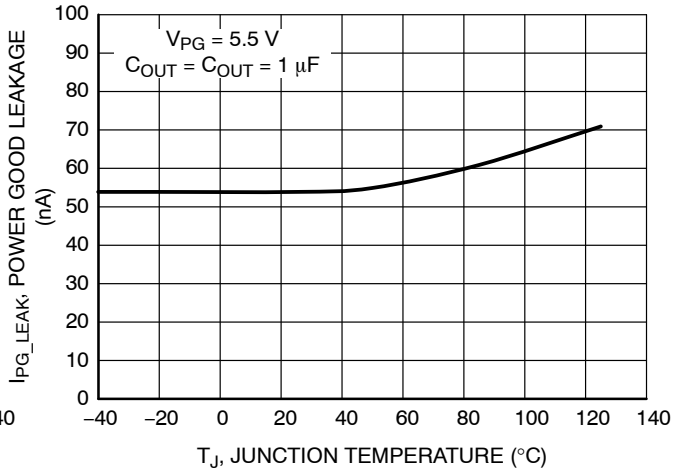


Figure 74. PG Pin Leakage vs. Temperature

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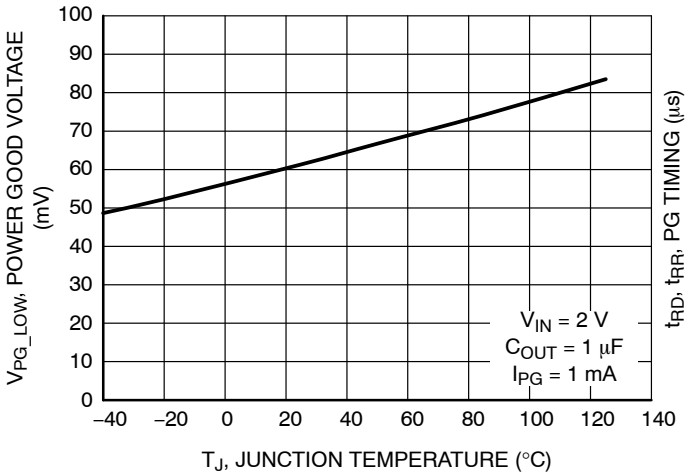


Figure 75. PG Low Voltage vs. Temperature

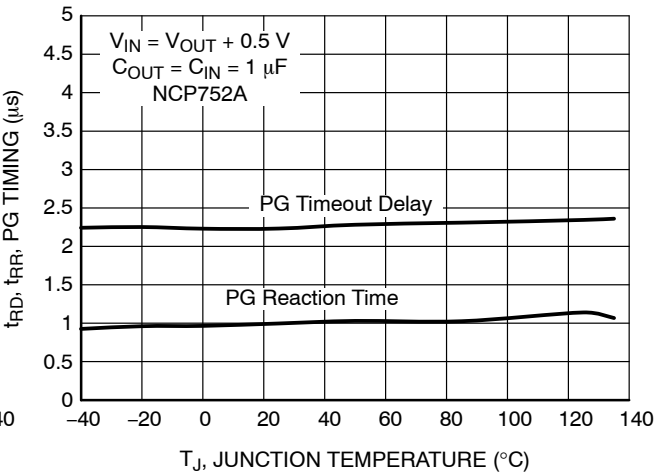


Figure 76. NCP752A PG Reaction Time, Delay Timing

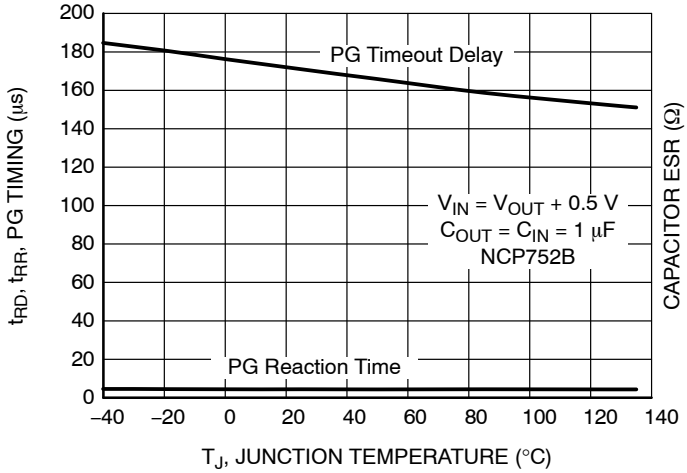


Figure 77. NCP752B PG Reaction Time, Delay Timing

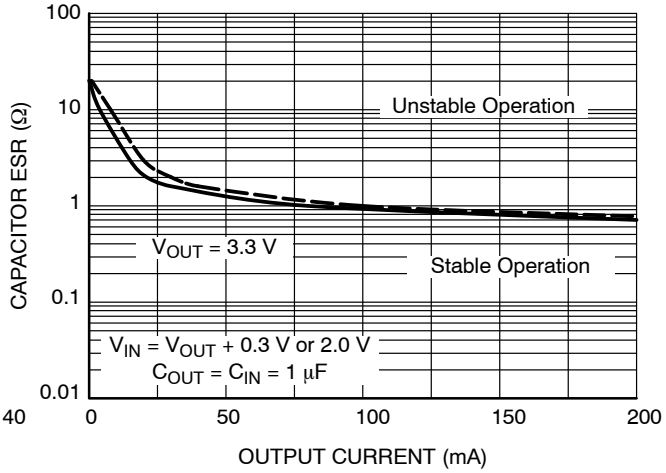


Figure 78. Stability vs. Output Capacitors ESR

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APPLICATION INFORMATION

The NCP752 is a high performance, 200 mA LDO voltage regulator with open−drain PG flag. This device delivers excellent noise and dynamic performance. Thanks to its adaptive ground current feature the device consumes only 12 μA of quiescent current at no−load condition. The regulator features very−low noise of 11.5 μV_{RMS}, PSRR of typ. 68 dB at 1 kHz and very good load/line transient response. The device is an ideal choice for battery powered portable applications.

A logic EN input provides ON/OFF control of the output voltage. When the EN is low the device consumes as low as typ. 120 nA from the IN pin.

The device is fully protected in case of output overload, output short circuit condition and overheating, assuring a very robust design.

Input Capacitor Selection (C_{IN})

It is recommended to connect a minimum of 1 μF Ceramic X5R or X7R capacitor close to the IN pin of the device. Larger input capacitors may be necessary if fast and large load transients are encountered in the application. There is no requirement for the min./max. ESR of the input capacitor but it is recommended to use ceramic capacitors for their low ESR and ESL.

Output Capacitor Selection (C_{OUT})

The NCP752 is designed to be stable with small 1.0 μF and larger ceramic capacitors on the output. The minimum effective output capacitance for which the LDO remains stable is 500 nF. The safety margin is provided to account for capacitance variations due to DC bias voltage, temperature, initial tolerance. There is no requirement for the minimum value of Equivalent Series Resistance (ESR) for the C_{OUT} but the maximum value of ESR should be less than 700 mΩ.

Larger output capacitors could be used to improve the load transient response or high frequency PSRR characteristics. It is not recommended to use tantalum capacitors on the output due to their large ESR. The equivalent series resistance of tantalum capacitors is also strongly dependent on the temperature, increasing at low temperature. The tantalum capacitors are generally more costly than ceramic capacitors.

No−load Operation

The regulator remains stable and regulates the output voltage properly within the ±2% tolerance limits even with no external load applied to the output.

Enable Operation

The NCP752 uses the EN pin to enable/disable its output and to control the active discharge function. If the EN pin voltage is < 0.4 V the device is guaranteed to be disabled. The pass transistor is turned−off so that there is virtually no current flow between the IN and OUT. In case of the option equipped with active discharge − the active discharge transistor is turned−on and the output voltage V_{OUT} is pulled to GND through a 1 kΩ resistor. In the disable state the device consumes as low as typ. 120 nA from the V_{IN}. If the EN pin voltage > 0.9 V the device is guaranteed to be enabled. The NCP752 regulates the output voltage and the active discharge transistor is turned−off. The EN pin has an internal pull − down current source with typ. value of 100 nA which assures that the device is turned−off when the EN pin is not connected. A build in deglitch time in the EN block prevents from periodic on/off oscillations that can occur due to noise on EN line. In the case that the EN function isn't required the EN pin should be tied directly to IN.

Reverse Current

The PMOS pass transistor has an inherent body diode which will be forward biased in the case that $V_{OUT} > V_{IN}$. Due to this fact in cases where the extended reverse current condition is anticipated the device may require additional external protection.

Output Current Limit

Output Current is internally limited within the IC to a typical 400 mA. The NCP752 will source this amount of current measured with the output voltage 100 mV lower than the nominal V_{OUT}. If the Output Voltage is directly shorted to ground (V_{OUT} = 0 V), the short circuit protection will limit the output current to 410 mA (typ). The current limit and short circuit protection will work properly up to V_{IN} = 5.5 V at T_A = 25°C. There is no limitation for the short circuit duration.

Thermal Shutdown

When the die temperature exceeds the Thermal Shutdown threshold (TSD − 160°C typical), Thermal Shutdown event is detected and the device is disabled. The IC will remain in this state until the die temperature decreases below the Thermal Shutdown Reset threshold (TSDU − 140°C typical). Once the IC temperature falls below the 140°C the LDO is enabled again. The thermal shutdown feature provides protection from a catastrophic device failure due to accidental overheating. This protection is not intended to be used as a substitute for proper heat sinking.

Power Dissipation

As power dissipated in the LDO increases, it might become necessary to provide some thermal relief. The maximum power dissipation supported by the device is dependent upon board design and layout. Mounting pad configuration on the PCB, the board material, and the ambient temperature affect the rate of junction temperature rise for the part. The maximum power dissipation the NCP752 can handle is given by:

$$P_{D(MAX)} = \frac{[125 - T_A]}{\theta_{JA}} \quad \text{(eq. 1)}$$

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For reliable operation junction tempertaure should be limited to +125°C.

The power dissipated by the NCP752 for given application conditions can be calculated as follows:

$$P_{D(MAX)} = V_{IN}I_{GND} + I_{OUT}(V_{IN} - V_{OUT}) \quad \text{(eq. 2)}$$

Load Regulation

The NCP752 features very good load regulation of typical 4 mV in the 0 mA to 200 mA range. In order to achieve this very good load regulation a special attention to PCB design is necessary. The trace resistance from the OUT pin to the point of load can easily approach 100 mΩ which will cause a 20 mV voltage drop at full load current, deteriorating the excellent load regulation.

Line Regulation

The IC features very good line regulation of 0.3 mV/V measured from $V_{IN} = V_{OUT} + 0.5$ V to 5.5 V.

Power Supply Rejection Ratio

At low frequencies the PSRR is mainly determined by the feedback open−loop gain. At higher frequencies in the range 100 kHz − 10 MHz it can be tuned by the selection of C_{OUT} capacitor and proper PCB layout.

Output Noise

The IC is designed for very−low output voltage noise. The typical noise performance of 11.5 μV_{RMS} makes the device suitable for noise sensitive applications.

Internal Soft Start

The Internal Soft−Start circuitry will limit the inrush current during the LDO turn−on phase. Please refer to typical characteristics section for typical inrush current values. The soft−start function prevents from any output voltage overshoots and assures monotonic ramp−up of the output voltage.

PCB Layout Recommendations

To obtain good transient performance and good regulation characteristics place C_{IN} and C_{OUT} capacitors close to the device pins and make the PCB traces wide. In order to minimize the solution size use 0402 capacitors. Larger copper area connected to the pins will also improve the device thermal resistance. The actual power dissipation can be calculated by the formula given in Equation 2.

ORDERING INFORMATION

Device	V_{OUT} Option	Marking	Rotation	Description	Package	Shipping†
NCP752AMX28TCG (Note 6)	2.8 V	D	90°	Ver. A PG Time-out Delay: 2 μs (Typ) PG Reaction Time: 2 μs (Typ)	XDFN6 (Pb−Free)	3000 or 5000 / Tape & Reel (Note 6)
NCP752AMX30TCG (Note 6)	3.0 V	E	90°			
NCP752AMX33TCG (Note 6)	3.3 V	F	90°			
NCP752ASN33T1G	3.3 V	EDE			TSOP−5 (Pb−Free)	
NCP752BMX18TCG (Note 6)	1.8 V	A	270°	Ver. B PG Time-out Delay: 200 μs (Typ) PG Reaction Time: 5 μs (Typ)	XDFN6 (Pb−Free)	3000 or 5000 / Tape & Reel (Note 6)
NCP752BMX28TCG (Note 6)	2.8 V	D	270°			
NCP752BMX30TCG (Note 6)	3.0 V	E	270°			
NCP752BMX33TCG (Note 6)	3.3 V	F	270°			
NCP752BSN33T1G	3.3 V	EEE			TSOP−5 (Pb−Free)	

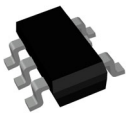
DISCONTINUED (Note 7)

NCP752AMX18TCG	1.8 V	A	90°	Ver. A PG Time-out Delay: 2 μs (Typ) PG Reaction Time: 2 μs (Typ)	XDFN6 (Pb−Free)	3000 or 5000 / Tape & Reel (Note 6)
NCP752ASN18T1G	1.8 V	EDA			TSOP−5 (Pb−Free)	
NCP752ASN28T1G	2.8 V	EDC				
NCP752ASN30T1G	3.0 V	EDD				
NCP752BSN18T1G	1.8 V	EEA		Ver. B PG Time-out Delay: 200 μs (Typ) PG Reaction Time: 5 μs (Typ)	TSOP−5 (Pb−Free)	3000 or 5000 / Tape & Reel (Note 6)
NCP752BSN28T1G	2.8 V	EEC				
NCP752BSN30T1G	3.0 V	EED				

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

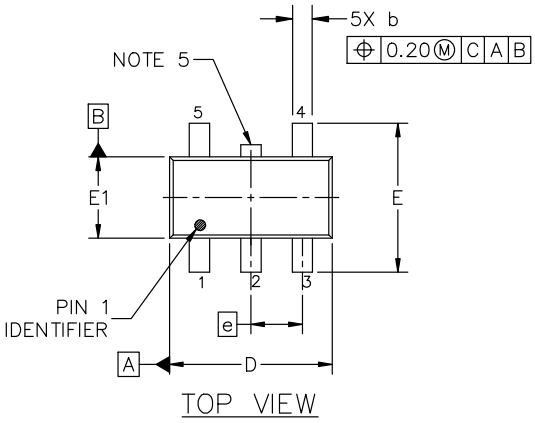
6. Product processed after October 1, 2022 are shipped with quantity 5000 units / tape & reel.
7. **DISCONTINUED:** These devices are not recommended for new design. Please contact your **onsemi** representative for information. The most current information on these devices may be available on www.onsemi.com.

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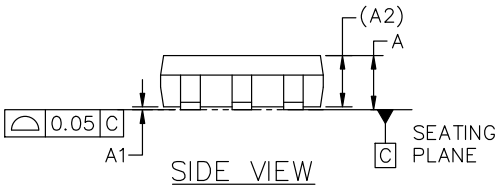


TSOP−5 3.00x1.50x0.95, 0.95P
CASE 483
ISSUE P

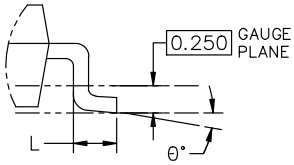
DATE 01 APR 2024



TOP VIEW



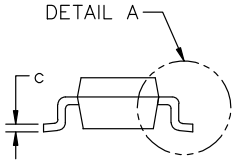
SIDE VIEW



DETAIL "A"
SCALE 2:1

NOTES:

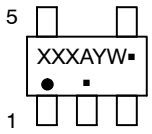
1. DIMENSIONING AND TOLERANCING CONFORM TO ASME Y14.5−2018.
2. ALL DIMENSION ARE IN MILLIMETERS (ANGLES IN DEGREES).
3. MAXIMUM LEAD THICKNESS INCLUDES LEAD FINISH THICKNESS. MINIMUM LEAD THICKNESS IS THE MINIMUM THICKNESS OF BASE MATERIAL.
4. DIMENSIONS D AND E1 DO NOT INCLUDE MOLD FLASH, PROTRUSIONS OF GATE BURRS. MOLD FLASH, PROTRUSIONS, OR GATE BURRS SHALL NOT EXCEED 0.15 PER SIDE. DIMENSION D.
5. OPTIONAL CONSTRUCTION: AN ADDITIONAL TRIMMED LEAD IS ALLOWED IN THIS LOCATION. TRIMMED LEAD NOT TO EXTEND MORE THAN 0.2 FROM BODY.



END VIEW

DIM	MILLIMETERS		
	MIN.	NOM.	MAX.
A	0.900	1.000	1.100
A1	0.010	0.055	0.100
A2		0.950 REF.	
b	0.250	0.375	0.500
c	0.100	0.180	0.260
D	2.850	3.000	3.150
E	2.500	2.750	3.000
E1	1.350	1.500	1.650
e		0.950 BSC	
L	0.200	0.400	0.600
θ	0°	5°	10°

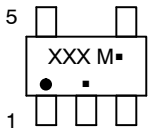
GENERIC
MARKING DIAGRAM*



Analog

XXX = Specific Device Code
A = Assembly Location
Y = Year
W = Work Week
▪ = Pb−Free Package

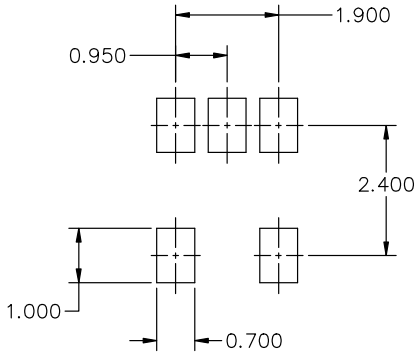
(Note: Microdot may be in either location)



Discrete/Logic

XXX = Specific Device Code
M = Date Code
▪ = Pb−Free Package

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, "G" or microdot "▪", may or may not be present. Some products may not follow the Generic Marking.



RECOMMENDED MOUNTING FOOTPRINT*

* FOR ADDITIONAL INFORMATION ON OUR Pb−FREE STRATEGY AND SOLDERING DETAILS, PLEASE DOWNLOAD THE ON SEMICONDUCTOR SOLDERING AND MOUNTING TECHNIQUES REFERENCE MANUAL, SOLDERRM/D.

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DESCRIPTION:	**TSOP−5 3.00x1.50x0.95, 0.95P**	**PAGE 1 OF 1**

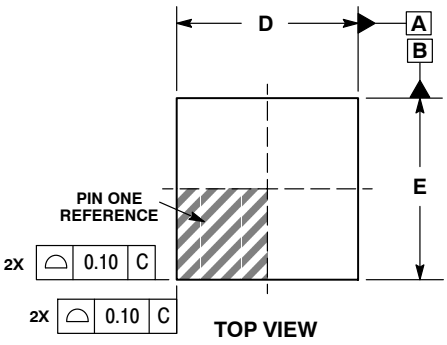
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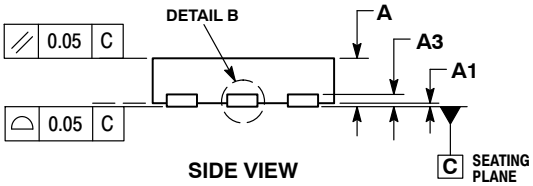
XDFN6 1.5x1.5, 0.5P
CASE 711AE
ISSUE B

DATE 27 AUG 2015

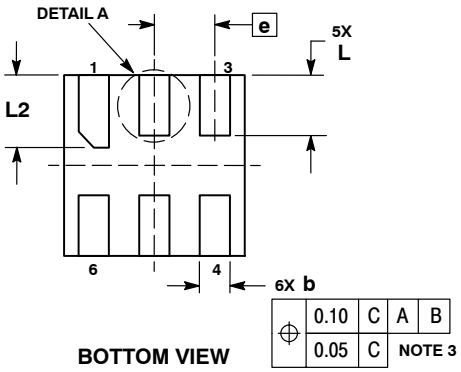
SCALE 4:1



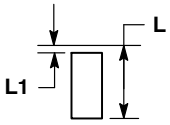
TOP VIEW



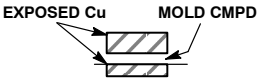
SIDE VIEW



BOTTOM VIEW



DETAIL A
ALTERNATE TERMINAL CONSTRUCTIONS

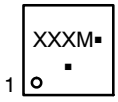


DETAIL B
ALTERNATE CONSTRUCTIONS

NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSION b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.10 AND 0.20mm FROM TERMINAL TIP.

	MILLIMETERS	
DIM	MIN	MAX
A	0.35	0.45
A1	0.00	0.05
A3	0.13 REF	
b	0.20	0.30
D	1.50 BSC	
E	1.50 BSC	
e	0.50 BSC	
L	0.40	0.60
L1	---	0.15
L2	0.50	0.70

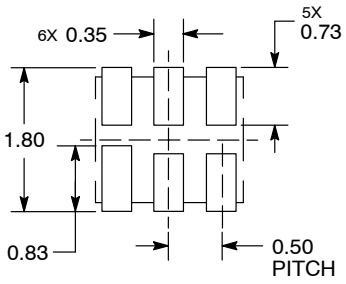
GENERIC MARKING DIAGRAM*



XXX = Specific Device Code
M = Date Code
▪ = Pb−Free Package
(Note: Microdot may be in either location)

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, “G” or microdot “ ▪”, may or may not be present.

RECOMMENDED MOUNTING FOOTPRINT*



DIMENSIONS: MILLIMETERS

*For additional information on our Pb−Free strategy and soldering details, please download the **onsemi** Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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DESCRIPTION:	**XDFN6, 1.5 X 1.5, 0.5 P**		**PAGE 1 OF 1**

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