NCP81391, NCP81391A

Advance Information

Integrated Driver and MOSFET

The NCP81391/A integrates a MOSFET driver, high−side MOSFET and low−side MOSFET into a single package. The driver and MOSFETs have been optimized for high−current DC−DC buck−boost power conversion applications. The NCP81391/A integrated solution greatly reduces package parasitics and board space compared to a discrete component solution.

Features

- Capable of Average Currents up to 25 A
- Capable of Peak Currents up to 65 A
- Over 97% Peak−Efficiency
- Compatible with 3.3 V and 5 V PWM Inputs, with Tri−State
- Zero Current Detection for Improving Light Load Efficiency
- Optional Thermal Shutdown Protection
  - NCP81391: With Thermal Shutdown
  - NCP81391A: No Thermal Shutdown
- Internal Bootstrap Diode
- Undervoltage Lockout
- This is a Pb−Free Device

Applications

- E−Cigarettes
- Unmanned Aerial Vehicles

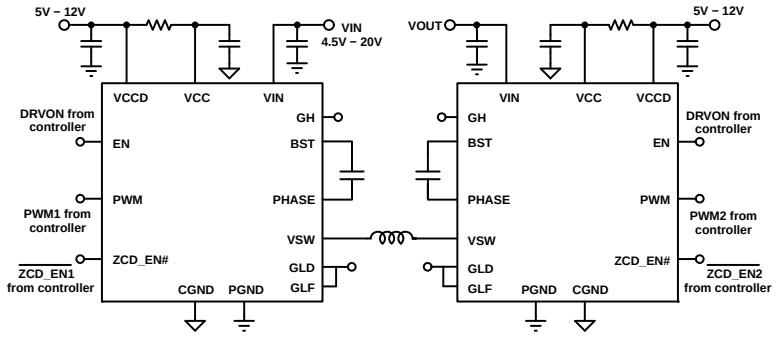
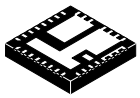


Figure 1. Application Diagram (Buck−Boost)

This document contains information on a new product. Specifications and information herein are subject to change without notice.

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QFN31 5x5
CASE 485FG

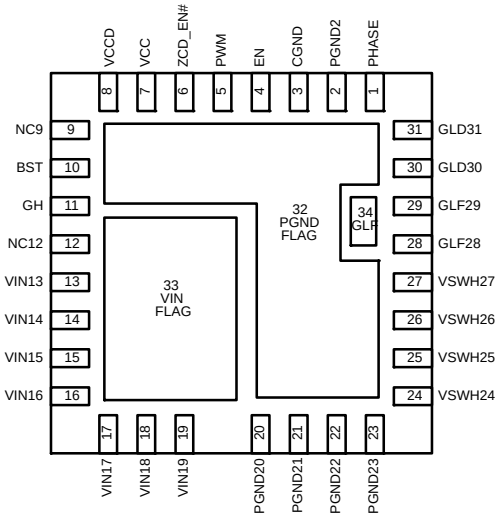
MARKING DIAGRAM



81391 = Specific Device Code
A = Assembly Location
L = Wafer Lot
Y = Year
W = Work Week
▪ = Pb−Free Package

(Note: Microdot may be in either location)

PINOUT DIAGRAM



(Top View)

ORDERING INFORMATION

Device	Package	Shipping†
NCP81391MNTXG	QFN31 (Pb−Free)	2500 / Tape & Reel
NCP81391AMNTXG		

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specification Brochure, BRD8011/D.

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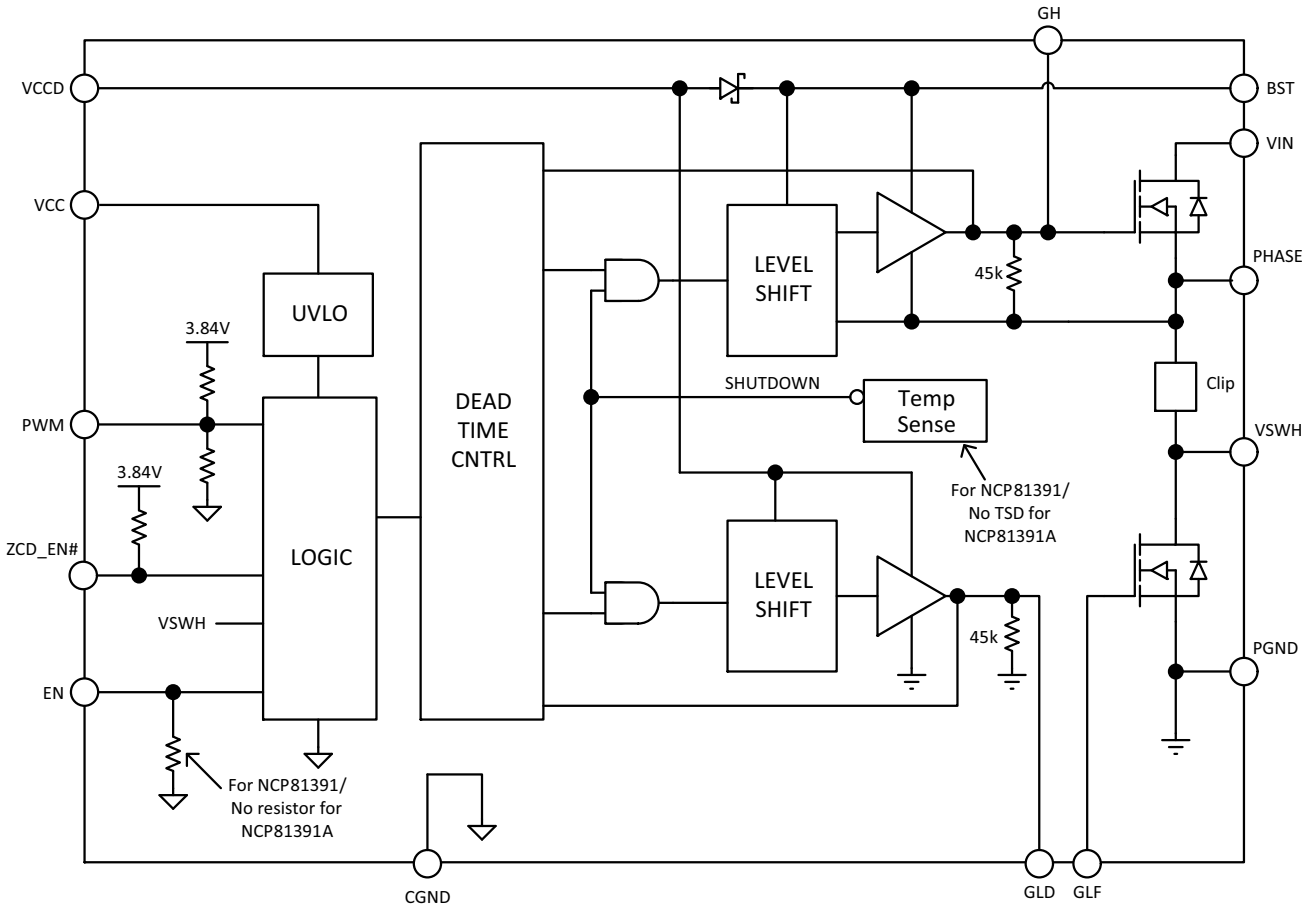


Figure 2. Simplified Block Diagram

Table 1. PIN LIST AND DESCRIPTIONS

Pin No.	Symbol	Description
1	PHASE	Bootstrap Capacitor Return
2	PGND2	Power Ground
3	CGND	Signal Ground
4	EN	Enable. There is a pull−down resistor to CGND for the NCP81391. No pull−down resistor for NCP81391A.
5	PWM	PWM Control Input: PWM = High → HS FET is on, LS FET is off PWM = Mid → HS FET is off, LS FET is off PWM = Low, ZCD_EN# = High → HS FET is off, LS FET is on PWM = Low, ZCD_EN# = Low → HS FET is off, LS FET is off when zero current is detected
6	ZCD_EN#	Zero Current Detect Control. When this pin is at logic low, low−side FET will turn off when zero inductor current is detected (after a minimum blanking/de−bounce time). There is an internal pull−up resistor.
7	VCC	Control Power Supply Input
8	VCCD	Driver Power Supply Input
9	NC9	No Connect
10	BST	Bootstrap Supply Voltage. Connect a MLCC capacitor of at least 0.1 μF from this pin to PHASE.
11	GH	High−Side MOSFET Gate Access. Leave floating.
12	NC12	No Connect
13	VIN13	Conversion Supply Power Input
14	VIN14	Conversion Supply Power Input
15	VIN15	Conversion Supply Power Input

Table 1. PIN LIST AND DESCRIPTIONS

Pin No.	Symbol	Description
16	VIN16	Conversion Supply Power Input
17	VIN17	Conversion Supply Power Input
18	VIN18	Conversion Supply Power Input
19	VIN19	Conversion Supply Power Input
20	PGND20	Power Ground
21	PGND21	Power Ground
22	PGND22	Power Ground
23	PGND23	Power Ground
24	VSWH24	Switch Node Output
25	VSWH25	Switch Node Output
26	VSWH26	Switch Node Output
27	VSWH27	Switch Node Output
28	GLF28	Low−Side MOSFET Gate Access. Pins 28, 29, 30 and 31 must be connected together on the PCB.
29	GLF29	Low−Side MOSFET Gate Access. Pins 28, 29, 30 and 31 must be connected together on the PCB.
30	GLD30	Low−Side Driver Gate Access. Pins 28, 29, 30 and 31 must be connected together on the PCB.
31	GLD31	Low−Side Driver Gate Access. Pins 28, 29, 30 and 31 must be connected together on the PCB.
32	PGND32	Power Ground Flag
33	VIN33	Conversion Supply Power Input Flag
34	GL34	Low Side MOSFET Gate Access. Do not connect to PCB. See Recommended PCB Footprint for details.

Table 2. ABSOLUTE MAXIMUM RATINGS (Electrical Information – all signals referenced to PGND unless noted otherwise)

Pin Name	V_{MIN}	V_{MAX}	Unit
VCC, VCCD (DC)	−0.3	13.2	V
VCC, VCCD (< 100 ns)	−	15	V
VIN	−0.3	30	V
BST (DC)	−0.3	35	V
BST (< 10 ns)	−0.3	40	V
BST to PH (DC)	−0.3	13.2	V
VSWH, PHASE (DC)	−0.3	30	V
VSWH, PHASE (< 10 ns)	−5	35	V
GH (DC)	−	V_{BST} + 0.3	V
GH wrt/ VSWH (DC)	−0.3	13.2	V
GH wrt/ VSWH (< 200 ns)	−2	−	V
GH wrt/ VSWH (< 100 ns)	−	15	V
GL (DC)	−0.3	V_{VCC} + 0.3	V
GL (< 200 ns)	−5	−	V
GL (< 100 ns)	−	15	V
EN, ZCD_EN#, PWM	−0.3	6.5	V

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

Table 3. THERMAL INFORMATION

Rating	Symbol	Value	Unit
Thermal Resistance (Note 1)	θ_{J-A}	23	°C/W
	$R\psi_{J-BT}$	0.3	°C/W
	$R\psi_{J-CT}$	0.5	°C/W
Operating Junction Temperature Range (Note 2)	T_J	−40 to +150	°C
Operating Ambient Temperature Range	T_A	−40 to +125	°C
Maximum Storage Temperature Range	T_{STG}	−40 to +150	°C
Maximum Power Dissipation	P_D	5.4	W
Moisture Sensitivity Level	MSL	3	

1. JESD 51-7 (2S2P Direct-Attach Method) with 0 LFM
2. The maximum package power dissipation must be observed.

Table 4. RECOMMENDED OPERATING CONDITIONS

Parameter	Pin Name	Conditions	Min	Typ	Max	Unit
Supply Voltage Range	VCC, VCCD		4.5	12	13.2	V
Conversion Voltage	VIN		4.5	12	20	V
Continuous Output Current		F_{SW} = 250 kHz			25	A
Peak Output Current		F_{SW} = 250 kHz, V_{VIN} = 12 V, V_{OUT} = 6 V, Duration = 10 ms, Period = 1 s			65	A
Operating Temperature			−40		100	°C

Functional operation above the stresses listed in the Recommended Operating Ranges is not implied. Extended exposure to stresses beyond the Recommended Operating Ranges limits may affect device reliability.

Table 5. ELECTRICAL CHARACTERISTICS

(V_{VCC} = V_{VCCD} = 12 V, V_{VIN} = 12 V, V_{EN} = 5.0 V, C_{VCCD} = C_{VCC} = 0.1 μF unless specified otherwise) Min/Max values are valid for the temperature range −40°C ≤ T_A ≤ 100°C unless noted otherwise, and are guaranteed by test, design or statistical correlation.)

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
VCC						
Operating Current	I_{VCC_PWM}	EN = 5 V, PWM = 250 kHz	−	−	2	mA
Enabled, No switching	I_{VCC_EN}	EN# = 5 V, PWM = 0 V, ZCD_EN# = 5 V	−	−	2	mA
	I_{VCC_ZCD}	EN# = 5 V, PWM = 0 V, ZCD_EN# = 0 V	−	−	2	mA
Disabled Current	I_{VCC_DIS}	EN = 0 V, ZCD_EN# = 5 V	−	960	1500	μA
	$I_{VCC_DIS_ZCD}$	EN = 0 V, ZCD_EN# = 0 V	−	960	1500	μA
UVLO Threshold	V_{UVLO}	VCC rising	3.8	4.35	4.5	V
UVLO Hysteresis	V_{UVLO_HYS}		150	200	−	mV
VCCD SUPPLY CURRENT						
Operating	I_{VCCD_PWM}	EN = 5 V, PWM = 250 kHz	−	47	70	mA
Enabled, No switching	I_{VCCD_EN}	EN = 5 V, PWM = 0 V NCP81391	−	−	100	μA
		EN = 5 V, PWM = 0 V NCP81391A	−	−	100	μA
Disabled	I_{VCCD_DIS}	EN = 0 V	−	60	100	μA
PWM INPUT						
Input High Voltage	V_{PWM_HI}		2.6	−	−	V
Input Mid Voltage	V_{PWM_MID}		1.4	−	1.8	V
Input Low Voltage	V_{PWM_LO}		−	−	0.6	V
PWM Input Resistance	R_{PWM}		−	162	−	kΩ
PWM Input Bias Voltage	V_{PWM_BIAS}	PWM pin is floating	−	1.6	−	V

Table 5. ELECTRICAL CHARACTERISTICS
(V_{VCC} = V_{VCCD} = 12 V, V_{VIN} = 12 V, V_{EN} = 5.0 V, C_{VCCD} = C_{VCC} = 0.1 μF unless specified otherwise) Min/Max values are valid for the temperature range −40°C ≤ T_A ≤ 100°C unless noted otherwise, and are guaranteed by test, design or statistical correlation.)

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
PWM INPUT						
Input Leakage	I_{PWM_LK}		−	−	5	μA
HIGH SIDE DRIVER						
Propagation Delay, PWM Falling	T_{PWM,PD_F}	PWM = Low to GH−VSWH falling @ 90%	−	18	24	
Non−overlap Delay, Leading Edge (Note 3)	T_{NOL_L}	GL falling @ 1 V to GH−VSWH rising @ 1 V	6	13	20	ns
Fall Time, High−Side Gate	t_{fDRVH}	GH falling, 90% to 10%	−	3.5	−	ns
Rise Time, High−Side Gate	t_{rDRVH}	GH rising, 10% to 90%	−	10	−	ns
Entering PWM Mid-state Propagation Delay, High-to−Mid	$T_{PWM_ENTER_H}$	PWM = High−to−Mid to GH−VSWH falling @ 90%	−	20	−	ns
Exiting PWM Mid-state Propagation Delay, Mid-to−High	$T_{PWM_EXIT_H}$	PWM = Mid−to−High to GH−VSWH rising @ 10%	−	13	25	ns
LOW SIDE DRIVER						
Propagation Delay, PWM Rising	T_{PWM,PD_R}	PWM = High to GL falling @ 90%	−	15	22	ns
Non−overlap Delay, Trailing Edge (Note 3)	T_{NOL_T}	GH−VSWH falling @ 1 V to GL rising @ 1 V	5	16	21	ns
Fall Time, Low−Side Gate	t_{fDRVL}	GL falling, 90% to 10%	−	13	−	ns
Rise Time, Low−Side Gate	t_{rDRVL}	GL rising, 10% to 90%	−	2.8	−	ns
Entering PWM Mid-state Propagation Delay, Low-to−Mid	$T_{PWM_ENTER_L}$	PWM = Low−to−Mid to GL falling @ 90%	−	30	−	ns
Exiting PWM Mid-state Propagation Delay, Mid-to−Low	$T_{PWM_EXIT_L}$	PWM = Mid−to−Low to GL rising @ 10%	−	13	25	ns
MOSFET						
N−Channel High−Side MOSFET On Resistance	R_{ON_HS}	From VIN to VSWH pin	−	2.0	−	mΩ
N−Channel Low−Side MOSFET On Resistance	R_{ON_LS}	From VSWH to PGND pin	−	1.7	−	mΩ
EN INPUT						
Input Leakage	I_{EN_LK}	NCP8139	−	20	−	μA
		NCP8139A	−	50	−	nA
Upper Threshold	V_{EN_HI}		2.0	−	−	V
Lower Threshold	V_{EN_LO}		−	−	0.8	V
Hysteresis	V_{EN_HYS}	V_{EN_HI} – V_{EN_LO}	−	470	−	mV
EN Input Resistance (NCP81391 Only)	R_{EN}	Pull−down resistance to CGND	−	300	−	kΩ
Enable Delay Time	T_{EN_ON}	EN rising @ V_{EN_HI} to GH−VSWH rising @ 10%, PWM = High	−	30	−	ns
Disable Delay Time	T_{EN_OFF}	EN falling @ V_{EN_LO} to GL falling @ 90%, PWM = Low	−	15	40	ns
ZERO CURRENT DETECTION ENABLE						
ZCD_EN# High	$V_{ZCD_ENB_HI}$		2.0	−	−	V
ZCD_EN# Low	$V_{ZCD_ENB_LO}$		−	−	0.8	V
Hysteresis	$V_{ZCD_ENB_HYS}$		−	470	−	mV
ZCD_EN# Input Resistance	R_{ZCD_ENB}	Pull−up resistance to internal 3.84 V	−	725	−	kΩ
ZCD Threshold	$V_{ZCD_ENB_TH}$	ZCD_EN# = 0 V, PWM = 0 V	−	−3	−	mV

Table 5. ELECTRICAL CHARACTERISTICS
(V_{VCC} = V_{VCCD} = 12 V, V_{VIN} = 12 V, V_{EN} = 5.0 V, C_{VCCD} = C_{VCC} = 0.1 μF unless specified otherwise) Min/Max values are valid for the temperature range −40°C ≤ T_A ≤ 100°C unless noted otherwise, and are guaranteed by test, design or statistical correlation.)

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
ZERO CURRENT DETECTION ENABLE						
ZCD Blanking + De−Bounce Timer	T_{BLANK}		−	130	−	ns
THERMAL SHUTDOWN (For NCP81391 Only)						
Thermal Shutdown Temperature	T_{THDN}	Temperature at Driver Die	−	170	−	°C
Thermal Shutdown Hysteresis	T_{THDN_HYS}		−	20	−	°C
BOOSTSTRAP DIODE						
Forward Voltage	V_{F_BST}	Forward Bias Current = 2.0 mA	0.1	0.4	0.6	V

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.
3. Guaranteed by design and/or characterization. This parameter is not tested in production.

TYPICAL CHARACTERISTICS

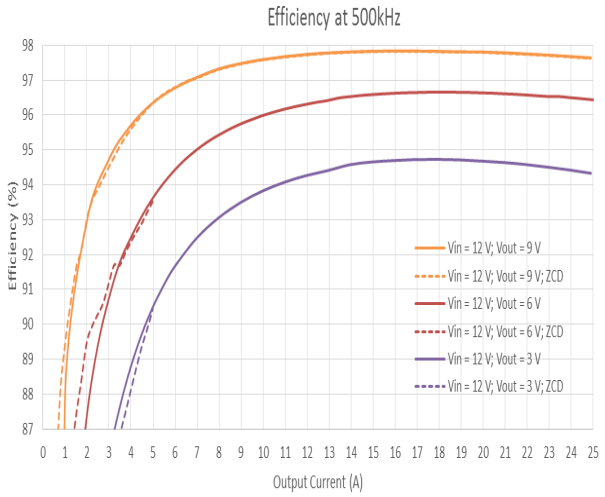


Figure 3. Efficiency − 12 V Input, 500 kHz

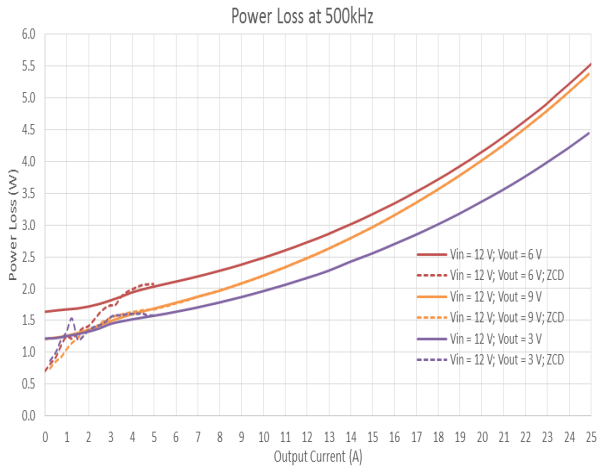


Figure 4. Power Loss − 12 V Input, 500 kHz

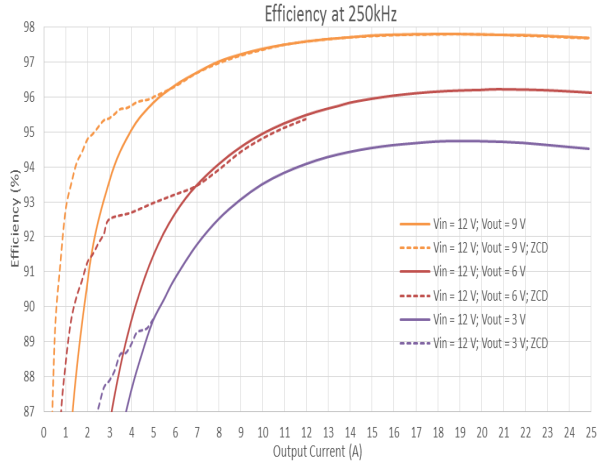


Figure 5. Efficiency − 12 V Input, 250 kHz

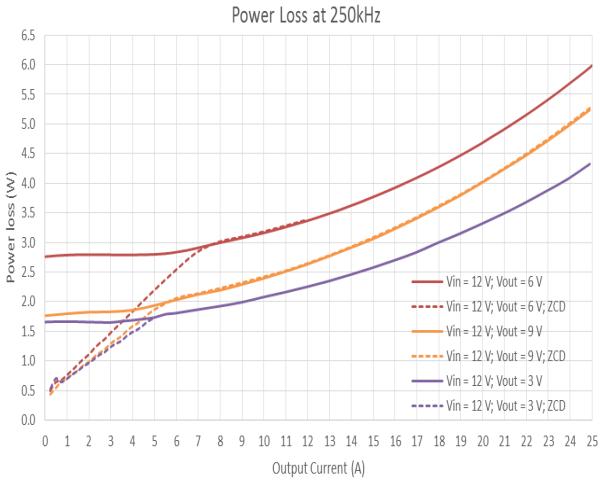


Figure 6. Power Loss − 12 V Input, 250 kHz

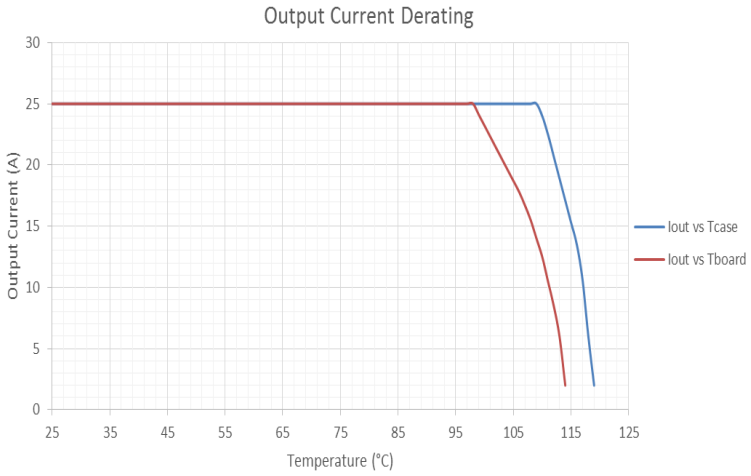


Figure 7. Output Current Derating
f_{SW} = 250 kHz; V_{IN} = 12 V; V_{CC} = V_{CCD} = 12 V; V_{OUT} = 6 V; L = 720 nH

APPLICATIONS INFORMATION

Theory of Operation

Low−Side Driver

The low−side driver drives a ground−referenced low−$R_{DS(on)}$ N−Channel MOSFET. The voltage rail for the low−side driver is internally connected to VCCD and CGND.

The GLD pin connects directly to the output of the low−side driver. The GLF pins connects directly to the gate of the low−side MOSFET. See Figure 2. GLD and GLF are not connected inside the package. For proper operation, these pins must be connected together on the PCB.

High−Side Driver

The high−side driver drives a floating low−$R_{DS(on)}$ N−channel MOSFET. The gate voltage for the high−side driver is developed by a bootstrap circuit referenced to the PHASE pin, which is internally connected to the VSWH pin.

The bootstrap circuit is comprised of an internal diode and an external bootstrap capacitor. When the NCP81391/A is starting up, the VSWH pin is at ground, so the bootstrap capacitor charges up to VCCD through the bootstrap diode (see Figure 1). When the PWM input goes high, the high−side driver will begin to turn on the high−side MOSFET using the stored charge of the bootstrap capacitor. As the high−side MOSFET turns on, the voltage at the VSWH pin rises. When the high−side MOSFET is fully on, the VSWH voltage equals the VIN voltage, with the BST voltage higher than VIN by the amount of voltage on the bootstrap capacitor. The bootstrap capacitor is recharged when the switch node goes low during the next cycle.

Parasitic inductances and capacitances within the packaging and MOSFETs can cause significant ringing of the VSWH signal during turn−on and turn−off of the high−side MOSFET. When operating at high input voltages and high output currents, the peak ringing voltages on VSWH could cause the drain−to−source voltage across the MOSFETs to exceed its maximum rating. Including a resistor in series with the bootstrap capacitor can reduce the peak VSWH ringing voltages. A resistor value of 4 Ω is recommended when operating at VIN voltages greater than 16 V.

Overlap Protection Circuit

As PWM transitions between the logic high and logic low states, the driver circuitry prevents both MOSFETs from being on at the same time. While one MOSFET is turned off, the driver monitors the gate voltage of that MOSFET until it reaches 1 V. At this point, a non−overlap timer is started, and prevents the gate of the other MOSFET from going high until this timer expires. In the electrical characteristics table, this non−overlap timer is specified as the time between 1 V of the falling gate and 10% of the high value of the rising gate.

Three−State PWM Input

Switching PWM between logic−high and logic−low states allows the driver to operate in continuous conduction mode, as long as VCC is greater than the UVLO threshold and EN is high.

The PWM mid−state allows the NCP81391/A to enter a high−impedance mode, where both MOSFETs are off.

Table 6. EN/PWM LOGIC TABLE

EN	PWM	ZCD_EN#	GH	GL
LOW	X	X	LOW	LOW
HIGH	LOW	HIGH	LOW	HIGH
HIGH	MID	HIGH	LOW	LOW
HIGH	HIGH	HIGH	HIGH	LOW
HIGH	LOW	LOW	LOW	ZCD
HIGH	MID	LOW	LOW	LOW
HIGH	HIGH	LOW	HIGH	LOW

Zero Current Detection

At light load conditions, the inductor current can be negative due to the inductor current ripple. The zero current detection (ZCD) function in the NCP81391/A can prevent negative current during these light load conditions. When ZCD is active, the NCP81391/A will monitor the voltage at the VSWH pins when the LS FET is on and conducting. There is a blanking/de−bounce timer that delays when this monitoring starts, from the time GL goes high. As the inductor current falls towards zero, the voltage on VSWH will become less negative. When the VSWH voltage reaches the ZCD threshold, the LS FET is turned off. Positive current can still flow through the body diode of the LS FET, but the body diode will block any current in the negative direction.

ZCD is activated by placing ZCD_EN# in the logic−low state. There is an internal pull−up resistor at the ZCD_EN# pin.

Whenever VCC rises above the UVLO threshold, an auto−calibration is conducted on the ZCD Threshold. During the auto−calibration, the driver outputs will remain low and not respond to the PWM input. The auto−calibration cycle takes 28 μs to complete, typically.

Thermal Shutdown

With the NCP81391, if the driver temperature exceeds T_{THDN}, the part will enter thermal shutdown and turn off both MOSFETs. After the temperature decreases to $T_{THDN} - T_{THDN_HYS}$, the part will resume normal operation.

For applications that prefer not to have this power stage have a thermal shutdown, the NCP81391A removes the thermal shutdown protection feature.

To distinguish between the NCP81391 and NCP81391A, externally, the NCP81391 has an internal pull−down resistor at the EN pin while the NCP81391A does not have an internal pull−down resistor at the EN pin.

Power Supply Decoupling

The NCP81391/A sources relatively large currents into the MOSFET gates. In order to maintain a constant and stable input supply voltage, low−ESR capacitors should be placed between VCC and GND and between VCCD and ground, close to the NCP81391/A. A 1 μF to 4.7 μF multilayer ceramic capacitor (MLCC) is sufficient. To further filter noise from VCCD from entering the VCC pin, placing a 10 Ω resistor between the VCC and VCCD pins is recommended.

Bootstrap Circuit

The bootstrap circuit uses an external charge storage capacitor (C_{BST}) and the internal bootstrap diode. The bootstrap capacitor should have a voltage rating twice the maximum VCCD supply voltage. A bootstrap capacitance of at least 100 nF with a minimum 25 V rating is recommended. For best performances, use a 1 μF ceramic capacitor.

In order to prevent the bootstrap capacitor from discharging during conditions where the high side is turned on for a long time, such as high duty cycle or ZCD, a maximum duty cycle must be respected. The maximum duty cycle depends on the two time constants that appear during the charging time (converter's t_{off}) and discharging time (converter's t_{on}). To keep the bootstrap capacitor charged, the following relation must kept.

$$D \cdot \frac{Rdrv}{(1 - D) \cdot Rbst} > 50$$

Thus, Dmax can be expressed as

$$Dmax = 1 - \frac{Rbst}{\frac{Rdrv}{50} + Rbst}$$

With the converter's duty cycle, R_{drv} the High−Side Driver equivalent resistance from VBST to VSWH (typically 5 kΩ), R_{bst} the bootstrap series resistor. Note that the bootstrap capacitance has no effect on maximum duty cycle since it is common in both time constants.

Example:

f_{sw} = 250 kHz, R_{drv} = 5 kΩ, R_{bst} = 4 Ω, the maximum duty cycle allowed to keep the bootstrap capacitor charged is D_{max} = 96% and $t_{on_max} = D_{max}/f_{sw}$ = 3.84 μs.

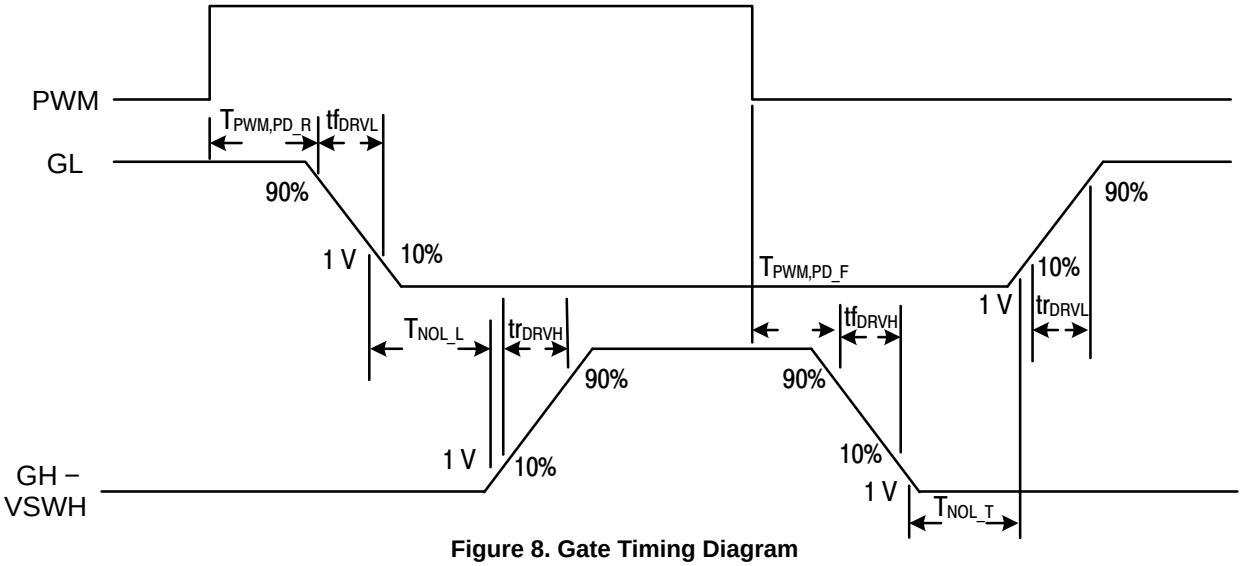


Figure 8. Gate Timing Diagram

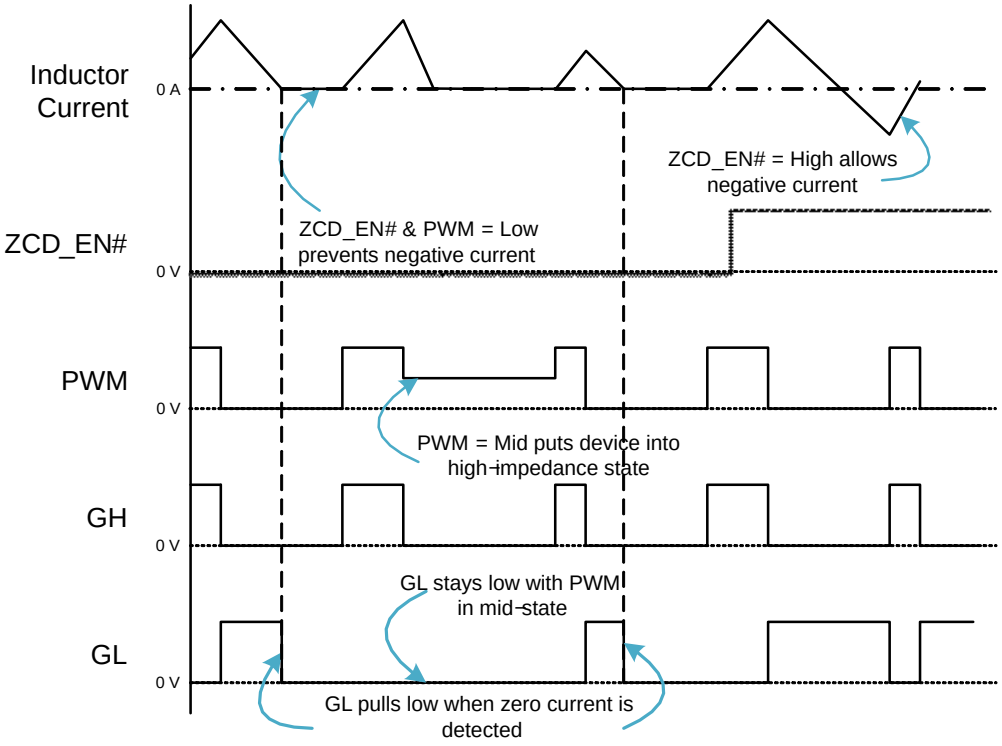


Figure 9. Zero Cross Detect Functionality

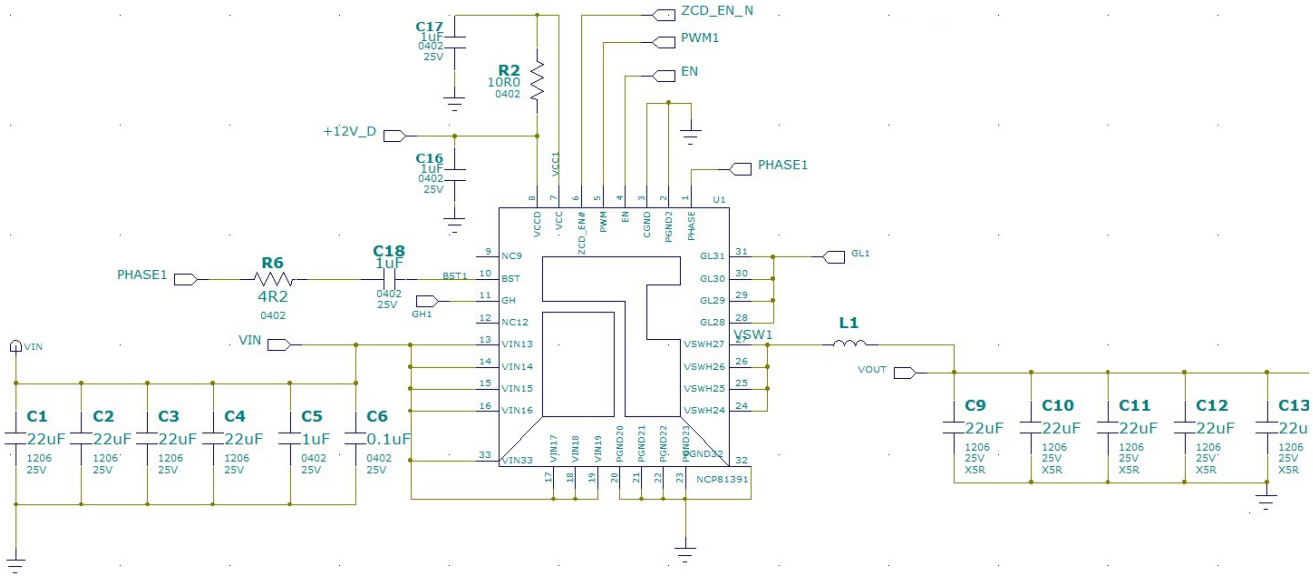


Figure 10. Application Schematic (Buck−Side)

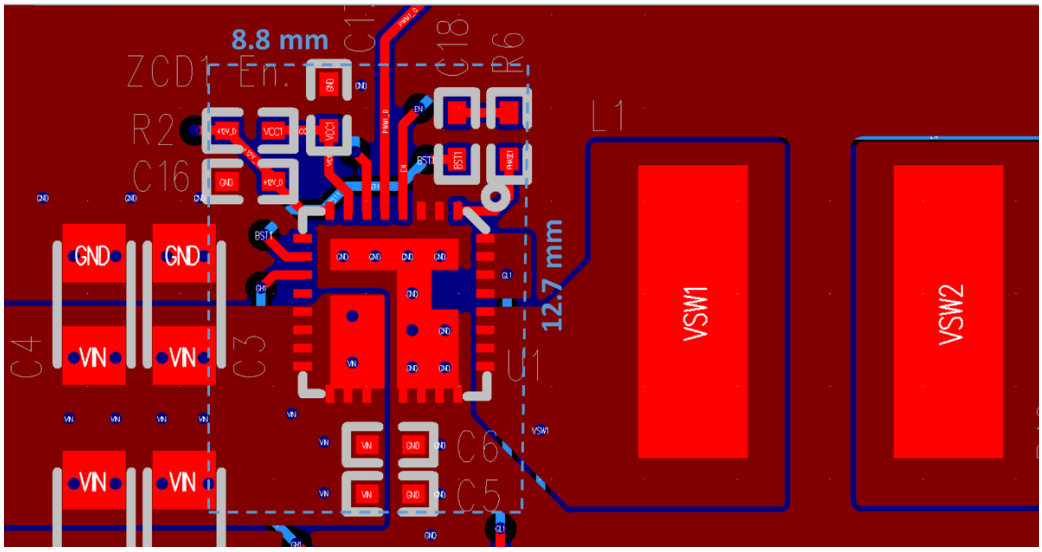
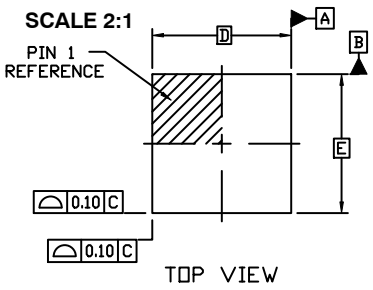


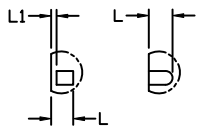
Figure 11. Recommended Layout (Buck−Side)

QFN31 5x5, 0.5P
CASE 485FG
ISSUE A

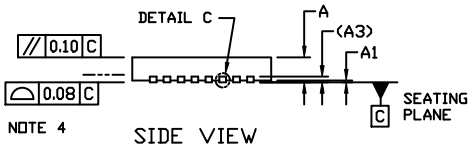
DATE 27 JUL 2017

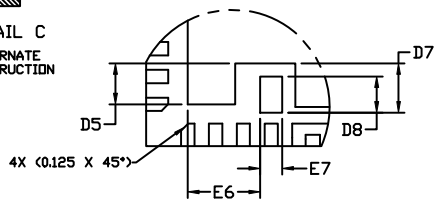
SCALE 2:1

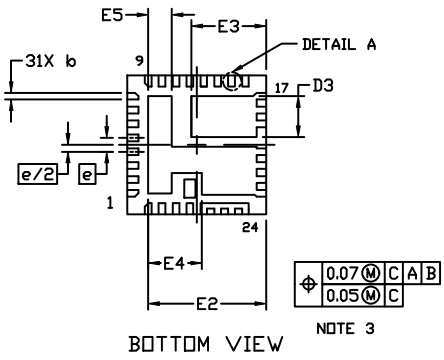


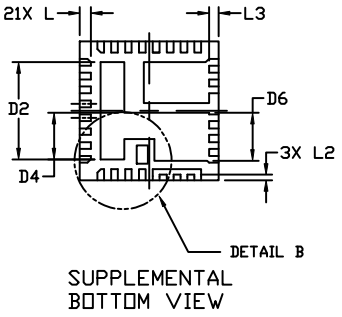








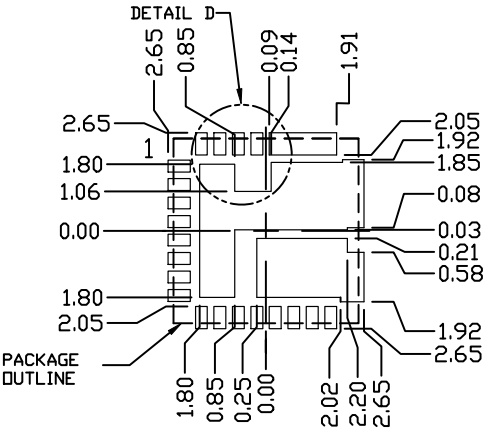




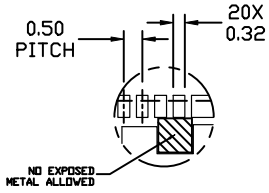
NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS
3. DIMENSION b APPLIES TO THE PLATED TERMINAL AND IS MEASURED BETWEEN 0.15 AND 0.30 MM FROM THE TERMINAL TIP.
4. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.

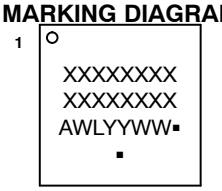
DIM	MILLIMETERS MIN.	MAX.
A	0.80	1.00
A1	---	0.05
A3	0.20 REF	
b	0.18	0.30
D	5.00 BSC	
D2	3.45	3.55
D3	1.43	1.53
D4	1.63	1.83
D5	0.69	0.79
D6	1.68	1.78
D7	0.89 REF	
D8	0.65 REF	
E	5.00 BSC	
E2	4.15	4.35
E3	2.60	2.80
E4	1.89	1.99
E5	0.80	0.90
E6	1.30 REF	
E7	0.40 REF	
e	0.50 BSC	
L	0.30	0.50
L1	---	0.15
L2	0.20 REF	
L3	0.35 REF	



RECOMMENDED
MOUNTING FOOTPRINT



GENERIC
MARKING DIAGRAM*



XXXXX = Specific Device Code
A = Assembly Location
WL = Wafer Lot
YY = Year
WW = Work Week
▪ = Pb−Free Package

(Note: Microdot may be in either location)

*This information is generic. Please refer to device data sheet for actual part marking.
Pb−Free indicator, “G” or microdot “ ▪”, may or may not be present.

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DESCRIPTION:	**QFN31 5x5, 0.5P**	**PAGE 1 OF 1**

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