Voltage Regulator - Dual Low I_Q, Low Dropout, Dual Input

300 mA

NCV8154

The NCV8154 is 300 mA, Dual Output Linear Voltage Regulator that offers two independent input pins and provides a very stable and accurate voltage with ultra low noise and very high Power Supply Rejection Ratio (PSRR) suitable for RF applications. The NCV8154 is suitable for powering RF blocks of automotive infotainment systems and other power sensitive device. Due to low power consumption the NCV8154 offers high efficiency and low thermal dissipation.

Features

- Operating Input Voltage Range: 1.9 V to 5.25 V
- Two Independent Input Voltage Pins
- Two Independent Output Voltage (for detail please refer to Ordering Information)
- Low IQ of typ. 55 μA per Channel
- High PSRR: 75 dB at 1 kHz
- Very Low Dropout: 140 mV Typical at 300 mA
- Thermal Shutdown and Current Limit Protections
- Stable with a 1 μF Ceramic Output Capacitor
- Available in DFN10 3x3mm and WDFN6 1.5x1.5mm Packages
- Active Output Discharge for Fast Output Turn-Off
- NCV Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC-Q100 Qualified and PPAP Capable; Device Temperature Grade 1: −40 °C to +125 °C Ambient Operating Temperature Range
- These are Pb-free Devices

Typical Applications

- Applications Requiring Wettable Flanks for Enhanced Visual Inspection
- Wireless LAN, Bluetooth®, ZigBee® Interfaces
- Automotive Infotainment Systems

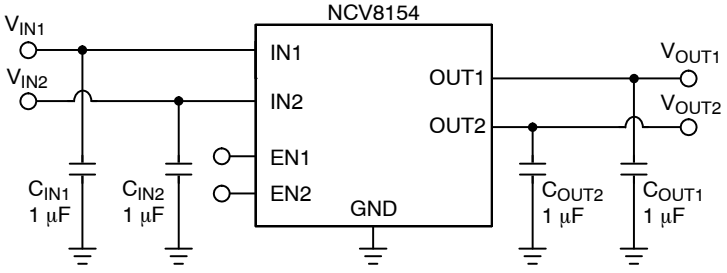


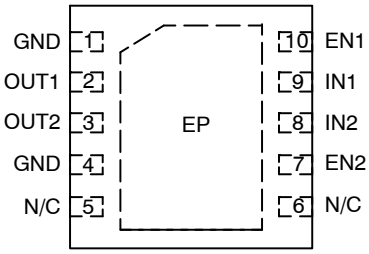
Figure 1. Typical Application Schematic



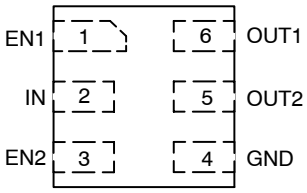
DFN10, 3x3
CASE 485C

WDFN6, 1.5x1.5
CASE 511BJ

PIN CONNECTIONS



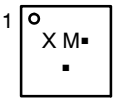
DFN10
(Top View)



WDFN6
(Top View)

MARKING DIAGRAMS





x	= NCV8154N – Non wettable flank
	= NCV8154W – Wettable flank
VVVVV	= Voltage Option
A	= Assembly Location
L	= Wafer Lot
Y	= Year
W	= Work Week
X	= Specific Device Code
M	= Month Code
▪	= Pb-Free Package

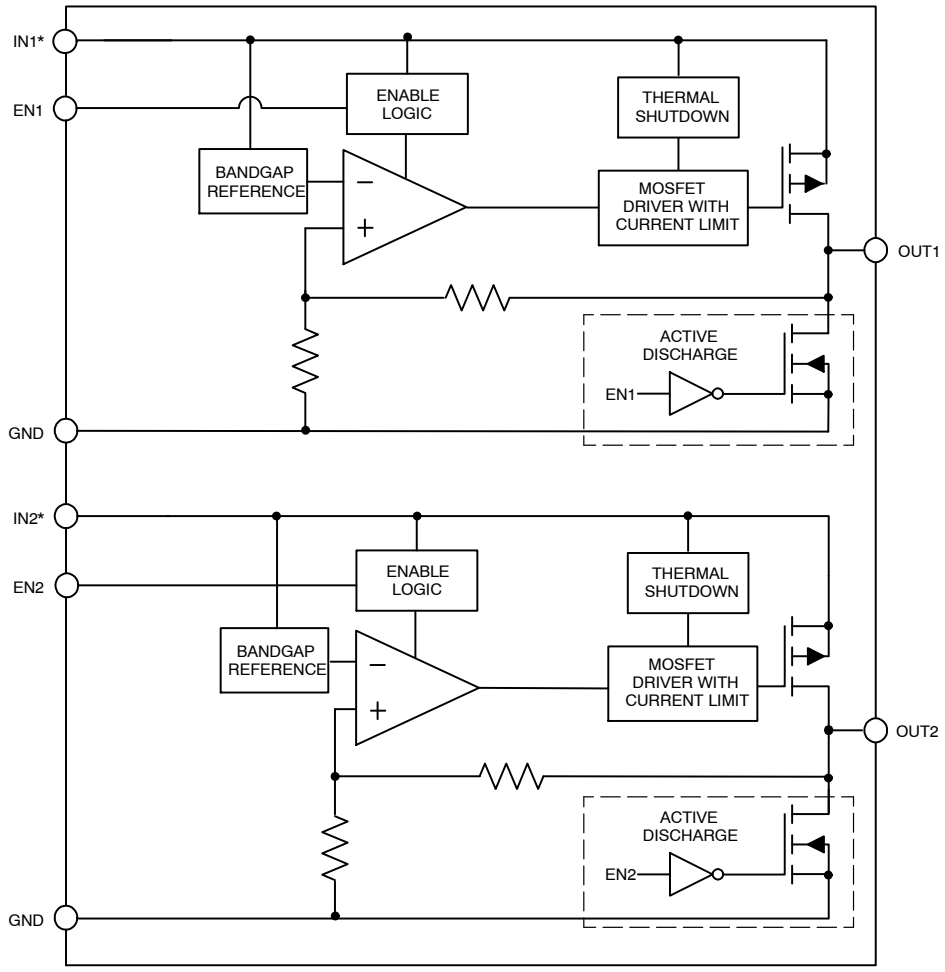
(Note: Microdot may be in either location)

ORDERING INFORMATION

See detailed ordering, marking and shipping information on page 16 of this data sheet.

NOTE: Some of the devices on this data sheet have been **DISCONTINUED**. Please refer to the table on page 16.

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*Dual IN available only for DFN10

Figure 2. Simplified Schematic Block Diagram

Table 1. PIN FUNCTION DESCRIPTION – DFN10

Pin No.	Pin Name	Description
1	GND	Power supply ground. Soldered to the copper plane allows for effective heat dissipation.
2	OUT1	Regulated output voltage of the first channel. A small 1 μF ceramic capacitor is needed from this pin to ground to assure stability.
3	OUT2	Regulated output voltage of the second channel. A small 1 μF ceramic capacitor is needed from this pin to ground to assure stability.
4	GND	Power supply ground. Soldered to the copper plane allows for effective heat dissipation.
5,6	N/C	Not connected, can be tied to ground plane to improve thermal dissipation.
7	EN2	Driving EN2 over 0.9 V turns-on OUT2. Driving EN below 0.4 V turns-off the OUT2 and activates the active discharge.
8	IN2	Inputs pin for second channel. It is recommended to connect 1 μF ceramic capacitor close to the device pin.
9	IN1	Inputs pin for first channel. It is recommended to connect 1 μF ceramic capacitor close to the device pin.
10	EN1	Driving EN1 over 0.9 V turns-on OUT1. Driving EN below 0.4 V turns-off the OUT1 and activates the active discharge.
–	EXP	Exposed pad must be tied to ground. Soldered to the copper plane allows for effective thermal dissipation.

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Table 2. PIN FUNCTION DESCRIPTION – WDFN6

Pin No.	Pin Name	Description
1	EN1	Driving EN1 over 0.9 V turns-on OUT1. Driving EN below 0.4 V turns-off the OUT1.
2	IN	Inputs pin. It is recommended to connect at least 1 μF ceramic capacitor close to the device pin.
3	EN2	Driving EN2 over 0.9 V turns-on OUT2. Driving EN below 0.4 V turns-off the OUT2.
4	GND	Power supply ground. Soldered to the copper plane allows for effective heat dissipation.
5	OUT2	Regulated output voltage of the second channel. A small 1 μF ceramic capacitor is needed from this pin to ground to assure stability.
6	OUT1	Regulated output voltage of the first channel. A small 1 μF ceramic capacitor is needed from this pin to ground to assure stability.

Table 3. ABSOLUTE MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Input Voltage (Note 1)	V_{IN1}, V_{IN2}	−0.3 V to 6 V	V
Output Voltage	V_{OUT1}, V_{OUT2}	−0.3 V to V_{IN} + 0.3 V or 6 V	V
Enable Inputs	V_{EN1}, V_{EN2}	−0.3 V to V_{IN} + 0.3 V or 6 V	V
Output Short Circuit Duration	t_{SC}	Indefinite	s
Operating Ambient Temperature Range	T_A	−40 to +125	°C
Maximum Junction Temperature	$T_{J(MAX)}$	150	°C
Storage Temperature	T_{STG}	−55 to 150	°C
ESD Capability, Human Body Model (Note 2)	ESD_{HBM}	2,000	V
ESD Capability, Machine Model (Note 2)	ESD_{MM}	200	V

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. Refer to ELECTRICAL CHARACTERISTICS and APPLICATION INFORMATION for Safe Operating Area.
2. This device series incorporates ESD protection and is tested by the following methods:
   ESD Human Body Model tested per AEC-Q100-002 (EIA/JESD22-A114)
   ESD Machine Model tested per AEC-Q100-003 (EIA/JESD22-A115)
   Latchup Current Maximum Rating tested per JEDEC standard: JESD78.

Table 4. THERMAL CHARACTERISTICS (Note 3)

Rating	Symbol	Value	Unit
Thermal Characteristics, DFN10 3 × 3 mm, Thermal Resistance, Junction-to-Air	θ_{JA}	109	°C/W
Thermal Characteristics, WDFN6 1.5 × 1.5 mm, Thermal Resistance, Junction-to-Air	θ_{JA}	207	°C/W

3. Single component mounted on 1 oz, FR4 PCB with 645 mm^2 Cu area.

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Min	Max	Unit
Input Voltage	V_{IN}	1.9	5.25	V
Junction Temperature	T_J	−40	125	°C

Functional operation above the stresses listed in the Recommended Operating Ranges is not implied. Extended exposure to stresses beyond the Recommended Operating Ranges limits may affect device reliability.

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Table 5. ELECTRICAL CHARACTERISTICS
(−40 °C ≤ T_J ≤ 125 °C; V_{IN} = $V_{OUT(NOM)}$ + 1 V or 2.5 V, whichever is greater; V_{EN} = 0.9 V, I_{OUT} = 1 mA, C_{IN} = C_{OUT} = 1 μF. Typical values are at T_J = +25 °C. Min/Max values are specified for T_J = −40 °C and T_J = 125 °C respectively.) (Note 4)

Parameter	Test Conditions		Symbol	Min	Typ	Max	Unit
Operating Input Voltage			V_{IN}	1.9		5.25	V
Output Voltage Accuracy	−40 °C ≤ T_J ≤ 125 °C	V_{OUT} > 2 V	V_{OUT}	−3		+3	%
		V_{OUT} ≤ 2 V		−60		+60	mV
Line Regulation	V_{OUT} + 0.5 V ≤ V_{IN} ≤ 5 V		Reg_{LINE}		0.02	0.2	%/V
Load Regulation	I_{OUT} = 1 mA to 300 mA	DFN10	Reg_{LOAD}		15	40	mV
		WDFN6			25	45	
Dropout Voltage (Note 5)	I_{OUT} = 300 mA	$V_{OUT(nom)}$ = 1.8 V	V_{DO}		335	430	mV
		$V_{OUT(nom)}$ = 2.8 V			160	290	
		$V_{OUT(nom)}$ = 3.3 V			140	270	
Output Current Limit	V_{OUT} = 90% $V_{OUT(nom)}$		I_{CL}		400		mA
Quiescent Current	I_{OUT} = 0 mA, EN1 = V_{IN}, EN2 = 0 V or EN2 = V_{IN}, EN1 = 0 V		I_Q		55	100	μA
	I_{OUT1} = I_{OUT2} = 0 mA, V_{EN1} = V_{EN2} = V_{IN}		I_Q		110	200	
Shutdown current (Note 6)	V_{EN} ≤ 0.4 V, V_{IN} = 5.25 V		I_{DIS}		0.1	1	μA
EN Pin Threshold Voltage High Threshold Low Threshold	 V_{EN} Voltage increasing V_{EN} Voltage decreasing		 V_{EN_HI} V_{EN_LO}	 0.9		 0.4	V
EN Pin Input Current	V_{EN} = V_{IN} = 5.25 V		I_{EN}		0.3	1.0	μA
Power Supply Rejection Ratio	V_{IN} = V_{OUT} + 1 V for V_{OUT} > 2 V, V_{IN} = 2.5 V, for V_{OUT} ≤ 2 V, I_{OUT} = 10 mA	f = 1 kHz	PSRR		75		dB
Output Noise Voltage	f = 10 Hz to 100 kHz		V_N		75		$μV_{rms}$
Active Discharge Resistance	V_{IN} = 4 V, V_{EN} < 0.4 V		R_{DIS}		50		Ω
Thermal Shutdown Temperature	Temperature increasing from T_J = +25 °C		T_{SD}		160		°C
Thermal Shutdown Hysteresis	Temperature falling from T_{SD}		T_{SDH}	–	20	–	°C

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

4. Performance guaranteed over the indicated operating temperature range by design and/or characterization. Production tested at T_J = T_A = 25 °C. Low duty cycle pulse techniques are used during testing to maintain the junction temperature as close to ambient as possible.
5. Characterized when V_{OUT} falls 100 mV below the regulated voltage at V_{IN} = $V_{OUT(NOM)}$ + 1 V.
6. Shutdown Current is the current flowing into the IN pin when the device is in the disable state.

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TYPICAL CHARACTERISTICS

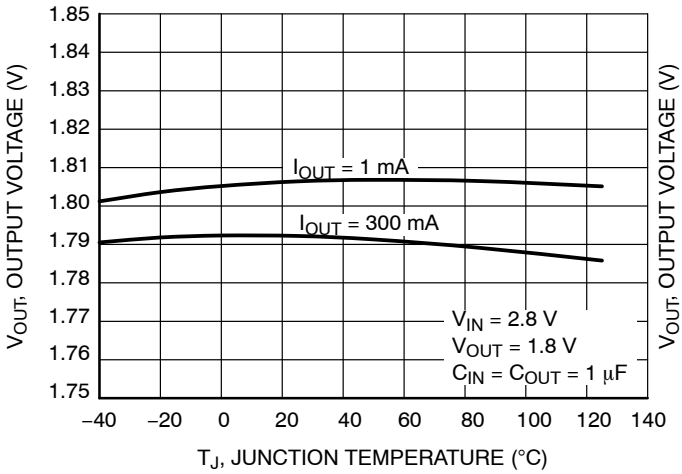


Figure 3. Output Voltage vs. Temperature
V_{OUT} = 1.8 V

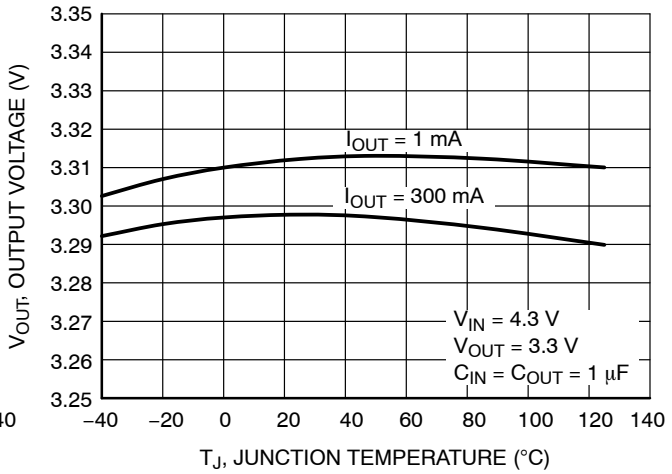


Figure 4. Output Voltage vs. Temperature
V_{OUT} = 3.3 V

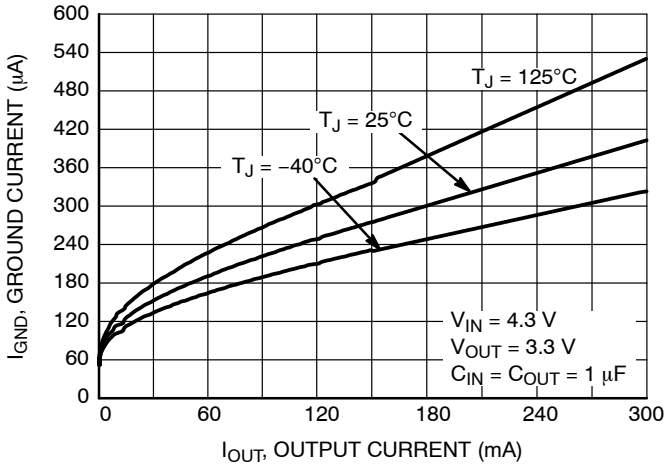


Figure 5. Ground Current vs. Output Current

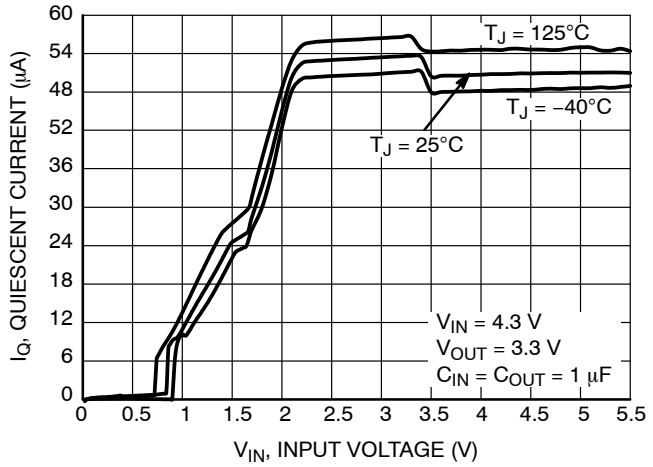


Figure 6. Quiescent Current vs. Input Voltage

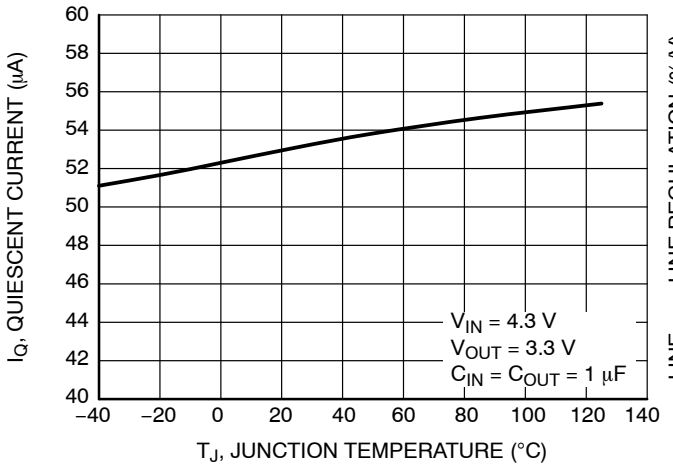


Figure 7. Quiescent Current vs. Temperature

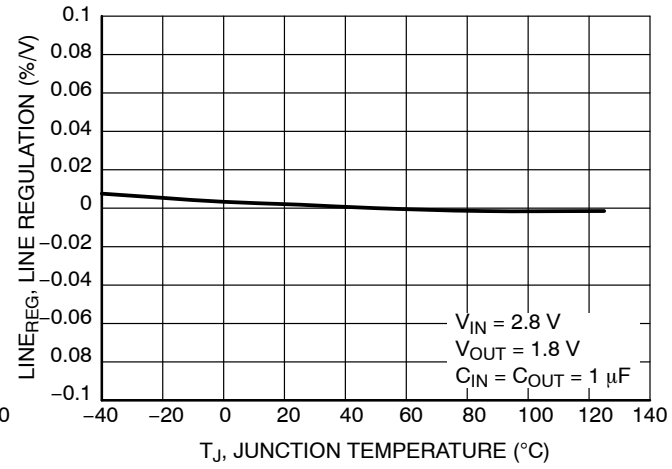


Figure 8. Line Regulation vs. Temperature
V_{OUT} = 1.8 V

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TYPICAL CHARACTERISTICS

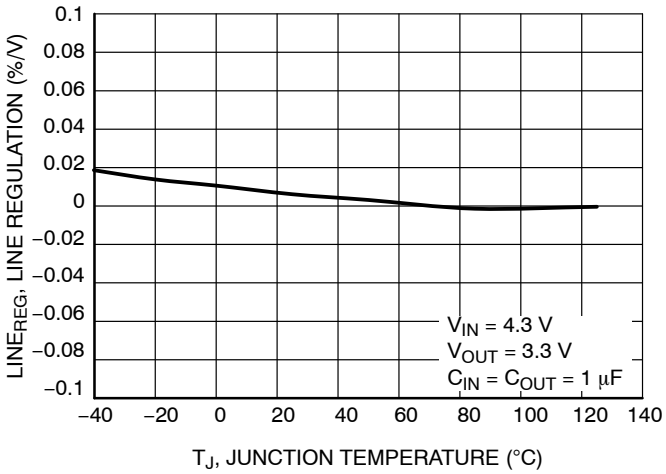


Figure 9. Line Regulation vs. Temperature
V_{OUT} = 3.3 V

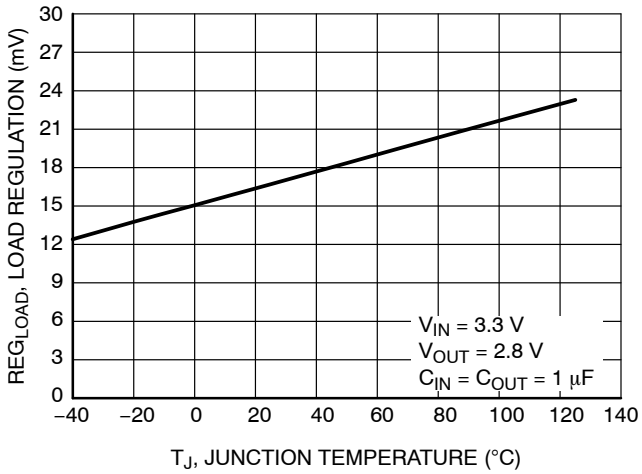


Figure 10. Load Regulation vs. Temperature
V_{OUT} = 2.8 V

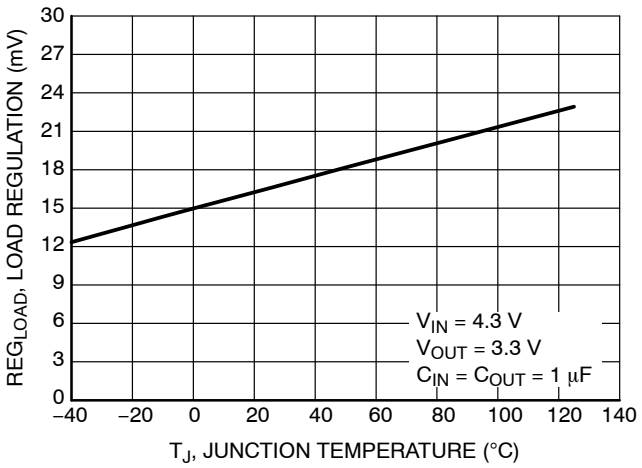


Figure 11. Load Regulation vs. Temperature
V_{OUT} = 3.3 V

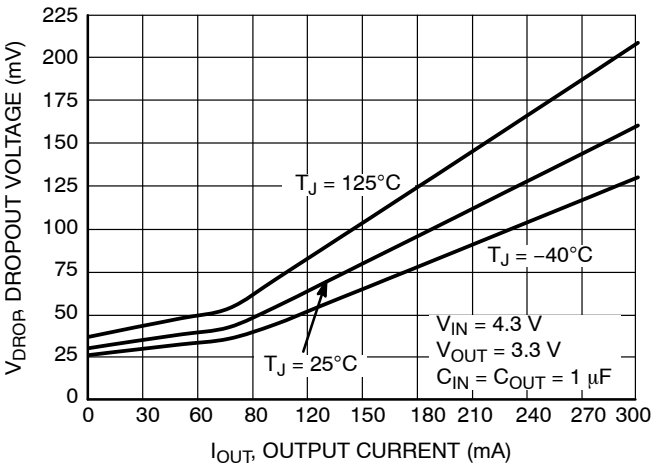


Figure 12. Dropout Voltage vs. Output Current

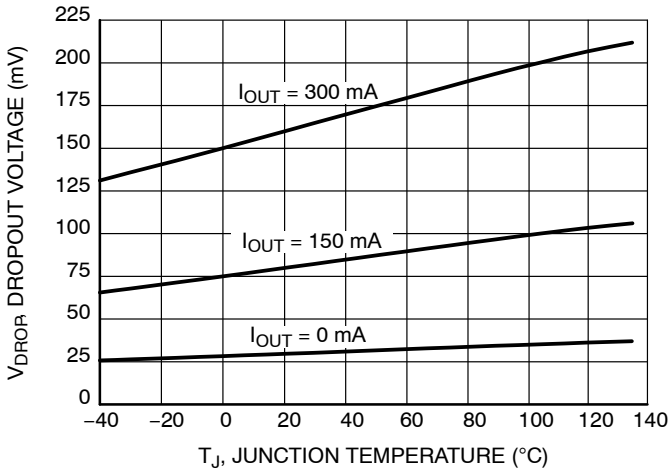


Figure 13. Dropout Voltage vs. Temperature

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TYPICAL CHARACTERISTICS

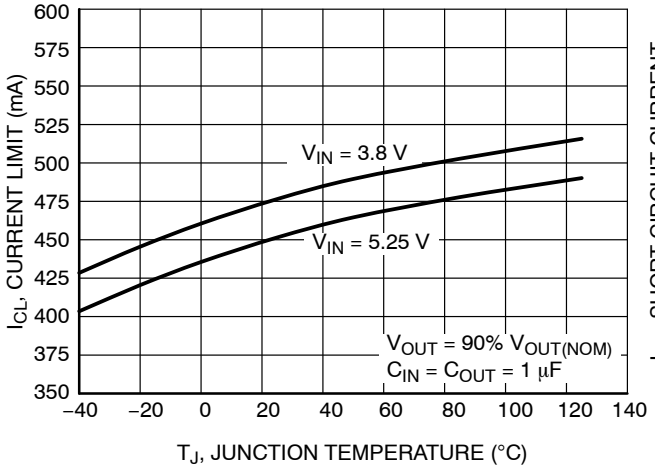


Figure 14. Current Limit vs. Temperature

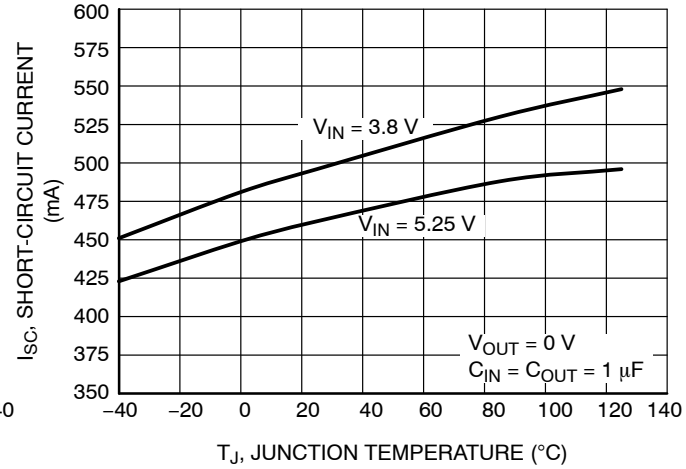


Figure 15. Short-Circuit Current vs. Temperature

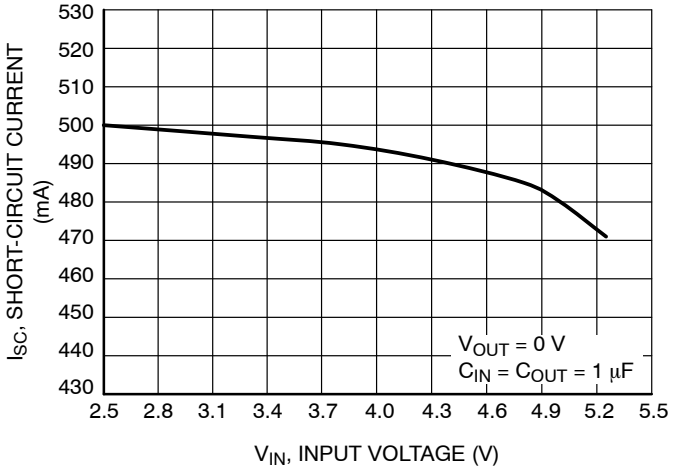


Figure 16. Short-Circuit Current vs. Input Voltage

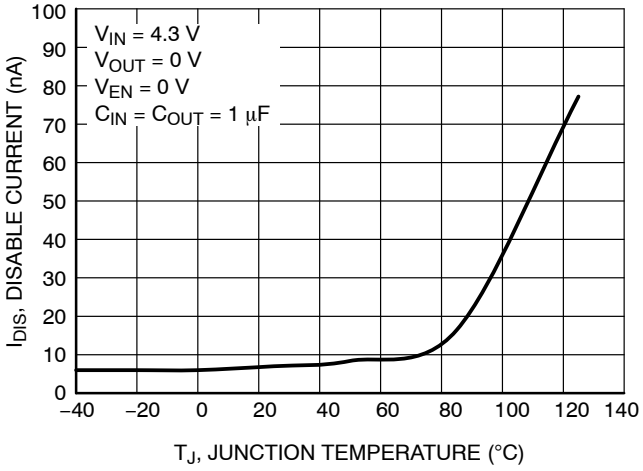


Figure 17. Disable Current vs. Temperature

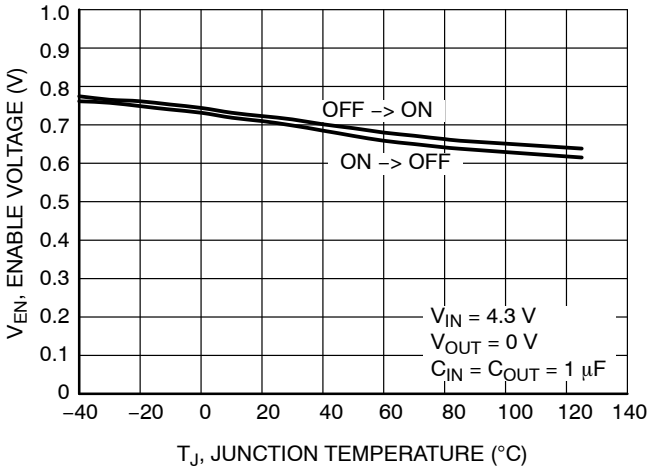


Figure 18. Enable Thresholds vs. Temperature

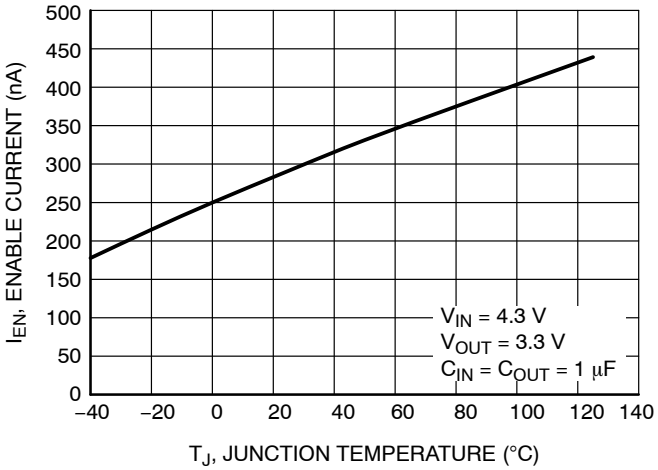


Figure 19. Current to Enable Pin vs. Temperature

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TYPICAL CHARACTERISTICS

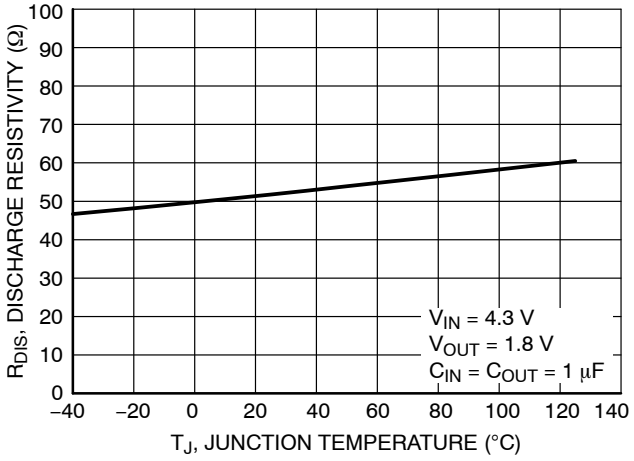


Figure 20. Discharge Resistivity vs. Temperature

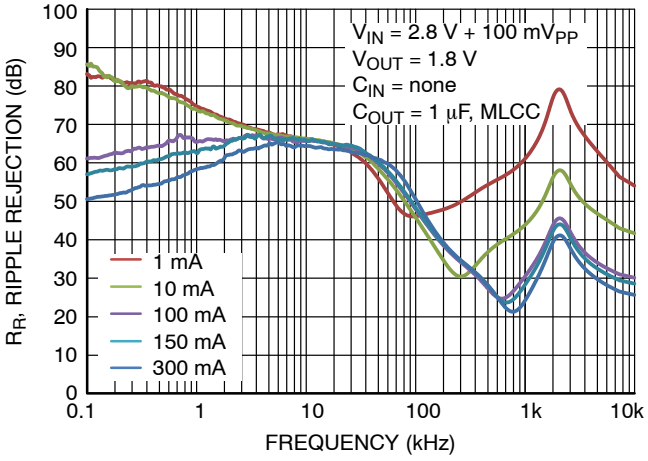


Figure 21. Power Supply Rejection Ratio, V_{OUT} = 1.8 V

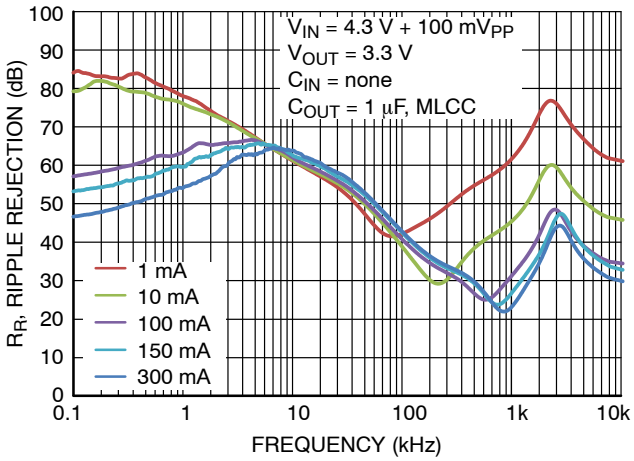


Figure 22. Power Supply Rejection Ratio, V_{OUT} = 3.3 V

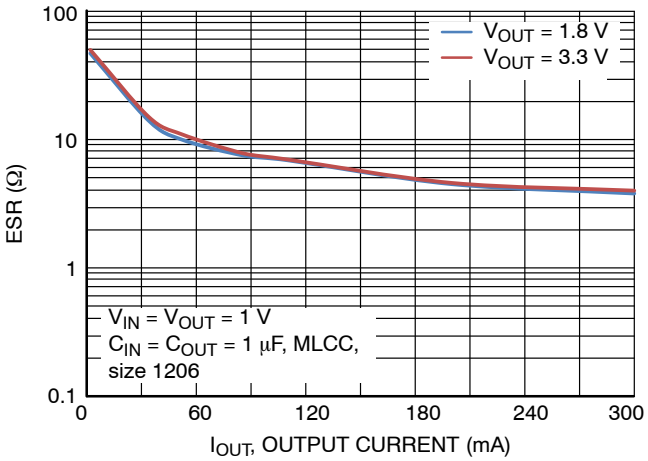
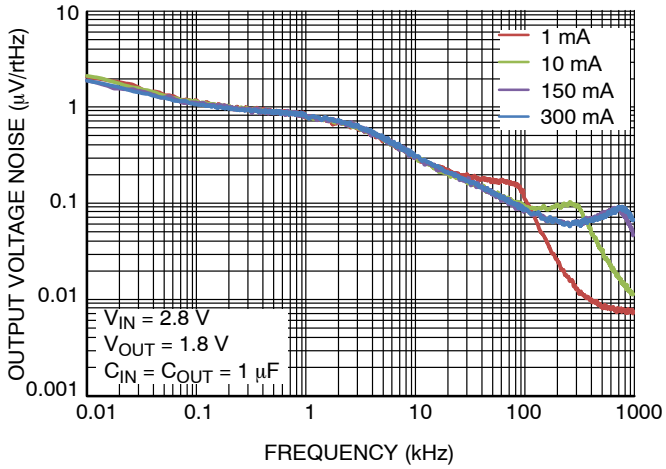


Figure 23. Output Capacitor ESR vs. Output Current

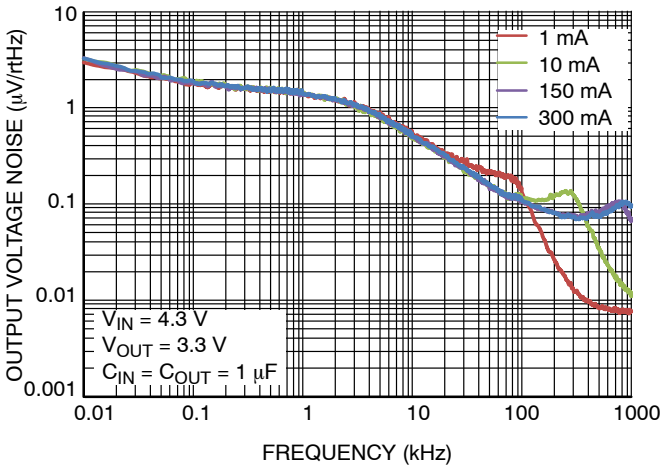


I_{OUT}	RMS Output Noise (μV)	
	10 Hz – 100 kHz	100 Hz – 100 kHz
1 mA	77.84	77.28
10 mA	71.71	70.48
150 mA	71.95	70.88
300 mA	72.71	71.67

Figure 24. Output Voltage Noise Spectral Density for V_{OUT} = 2.8 V, C_{OUT} = 1 μF

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TYPICAL CHARACTERISTICS



I_{OUT}	RMS Output Noise (μV)	
	10 Hz – 100 kHz	100 Hz – 100 kHz
1 mA	119.7	117.87
10 mA	113.47	111.47
150 mA	113.84	112.05
300 mA	115.95	114.03

Figure 25. Output Voltage Noise Spectral Density for V_{OUT} = 3.3 V, C_{OUT} = 1 μF

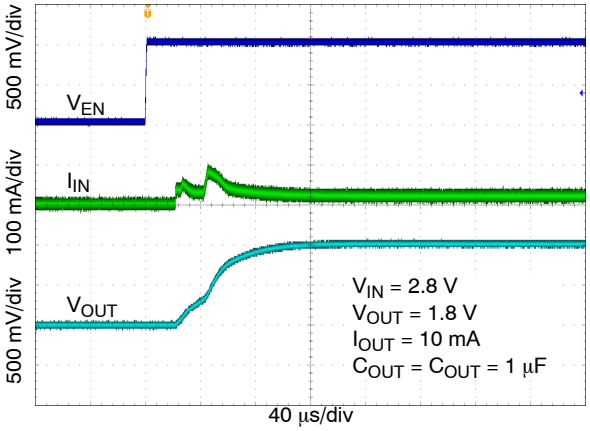


Figure 26. Enable Turn-on Response – V_{OUT} = 1.8 V, C_{OUT} = 1 μF

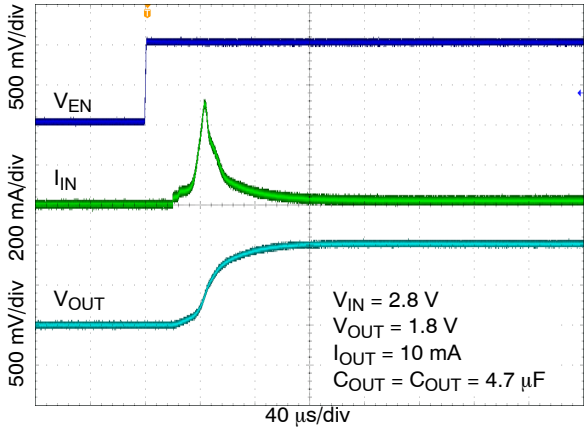


Figure 27. Enable Turn-on Response – V_{OUT} = 1.8 V, C_{OUT} = 4.7 μF

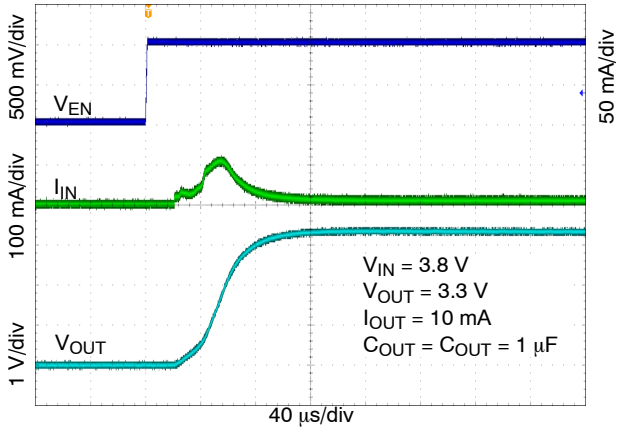


Figure 28. Enable Turn-on Response – V_{OUT} = 3.3 V, C_{OUT} = 1 μF

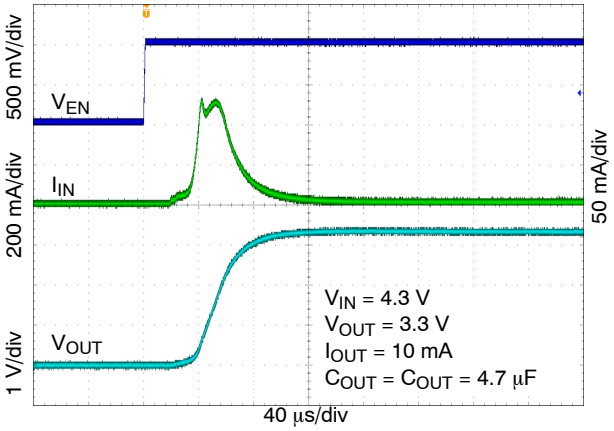


Figure 29. Enable Turn-on Response – V_{OUT} = 3.3 V, C_{OUT} = 4.7 μF

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TYPICAL CHARACTERISTICS

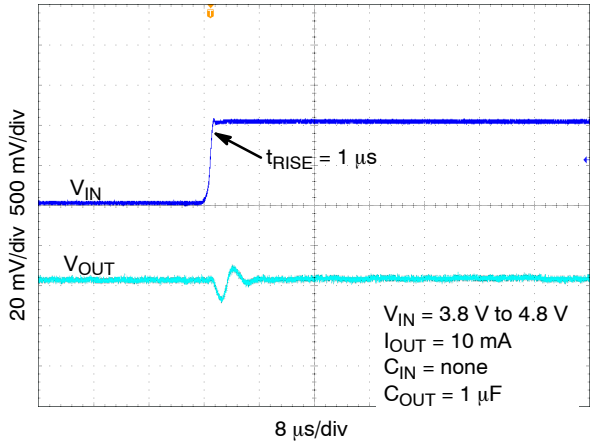


Figure 30. Line Transient Response – Rising Edge, V_{OUT} = 3.3 V, I_{OUT} = 10 mA

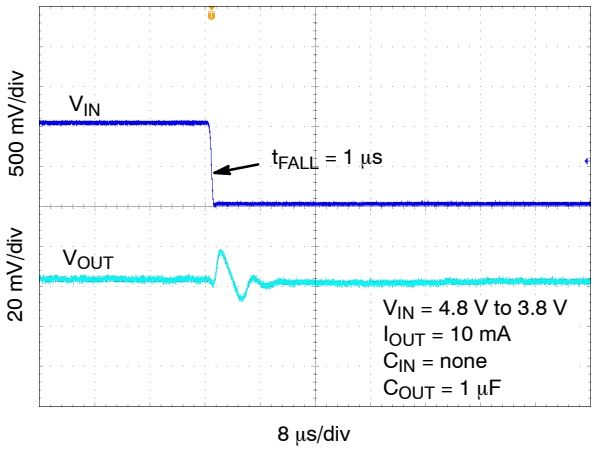


Figure 31. Line Transient Response – Falling Edge, V_{OUT} = 3.3 V, I_{OUT} = 10 mA

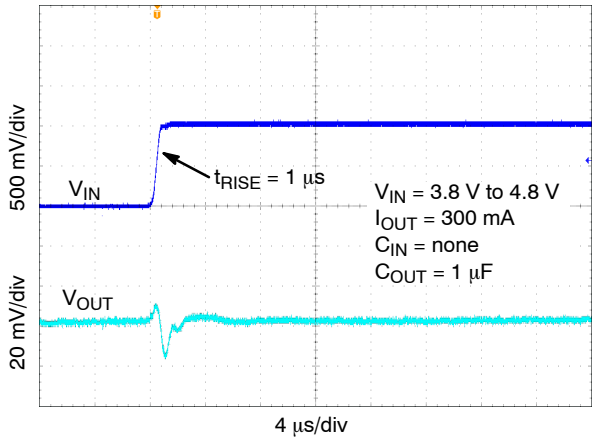


Figure 32. Line Transient Response – Rising Edge, V_{OUT} = 3.3 V, I_{OUT} = 300 mA

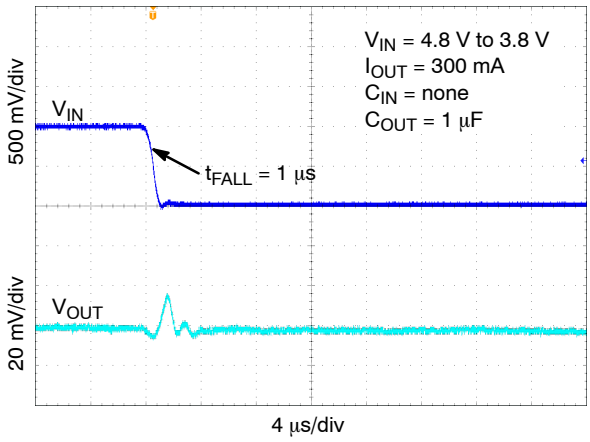


Figure 33. Line Transient Response – Falling Edge, V_{OUT} = 3.3 V, I_{OUT} = 300 mA

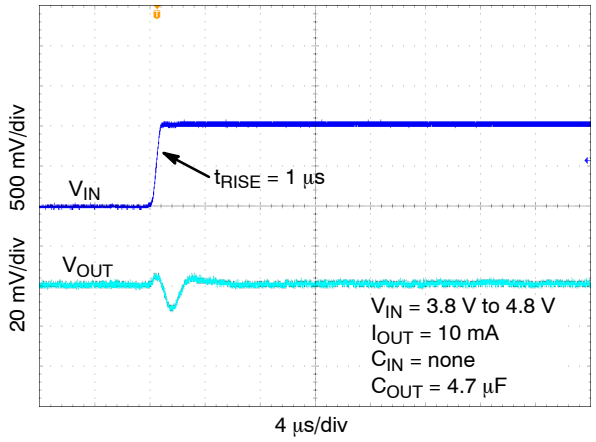


Figure 34. Line Transient Response – Rising Edge, V_{OUT} = 3.3 V, I_{OUT} = 10 mA, C_{OUT} = 4.7 μF

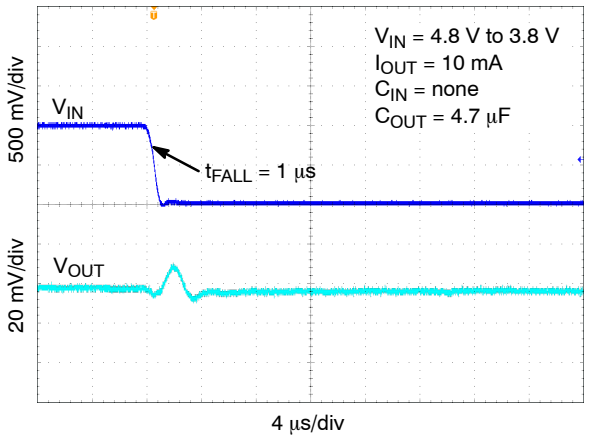


Figure 35. Line Transient Response – Falling Edge, V_{OUT} = 3.3 V, I_{OUT} = 10 mA, C_{OUT} = 4.7 μF

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TYPICAL CHARACTERISTICS

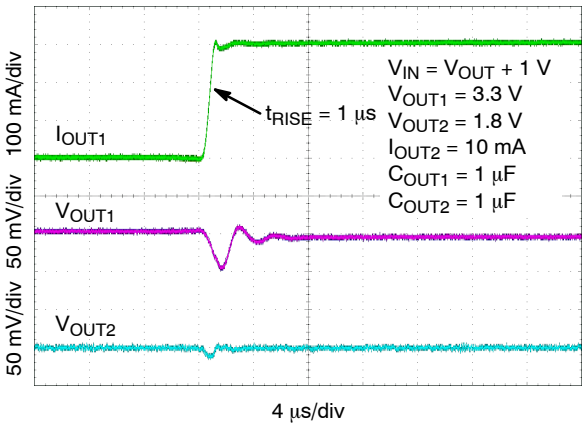


Figure 36. Load Transient Response – 1.8 V – Rising Edge, I_{OUT1} = 100 μA to 300 mA

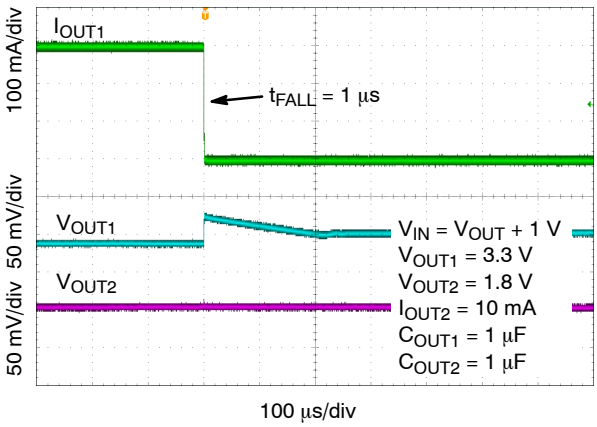


Figure 37. Load Transient Response – 1.8 V – Falling Edge, I_{OUT1} = 300 mA to 100 μA

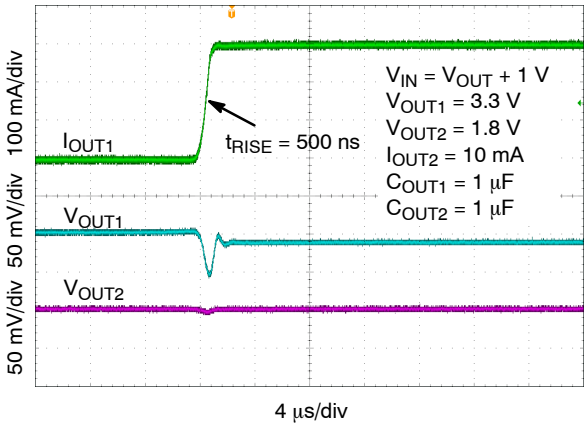


Figure 38. Load Transient Response – 1.8 V – Rising Edge, I_{OUT1} = 1 mA to 300 mA

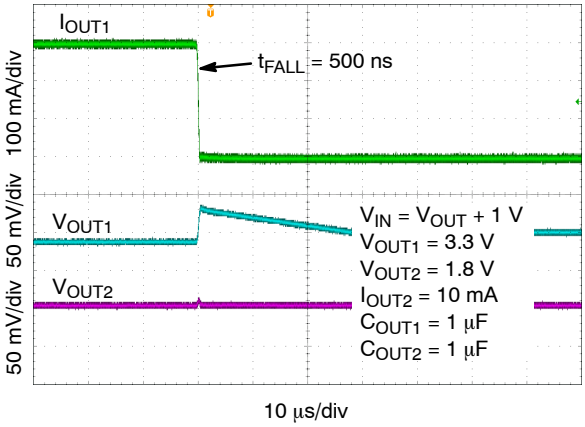


Figure 39. Load Transient Response – 1.8 V – Falling Edge, I_{OUT1} = 300 mA to 1 mA

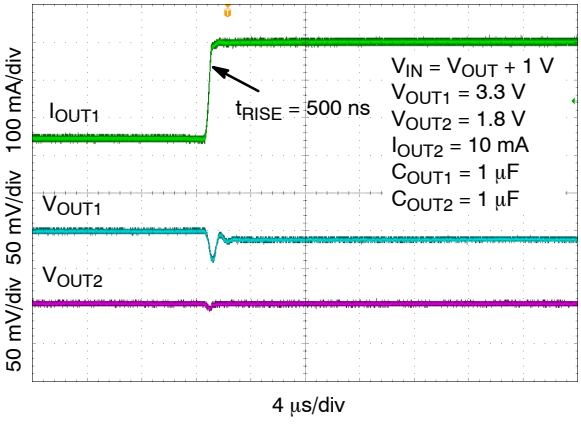


Figure 40. Load Transient Response – 1.8 V – Rising Edge, I_{OUT} = 50 mA to 300 mA

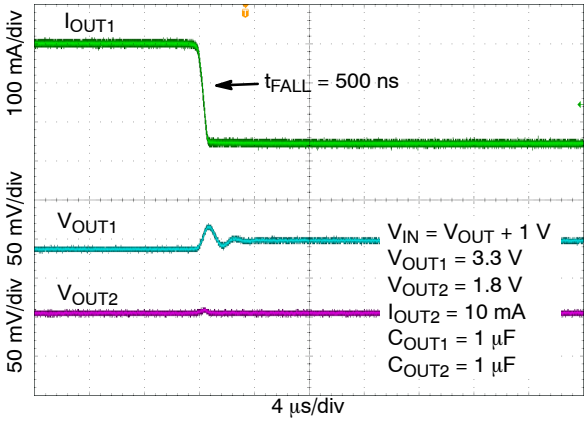


Figure 41. Load Transient Response – Falling Edge, I_{OUT} = 300 mA to 50 mA

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TYPICAL CHARACTERISTICS

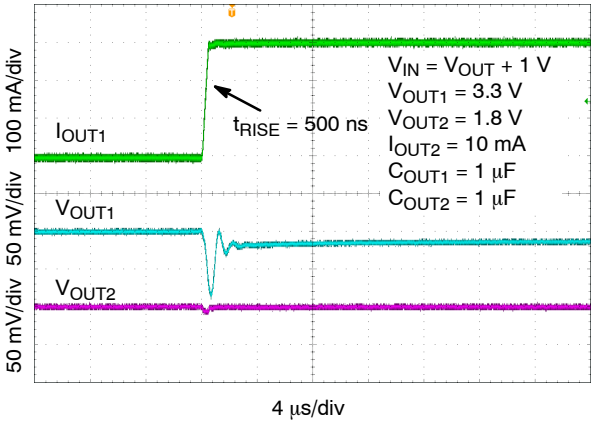


Figure 42. Load Transient Response – 3.3 V – Rising Edge, I_{OUT1} = 100 μA to 300 mA

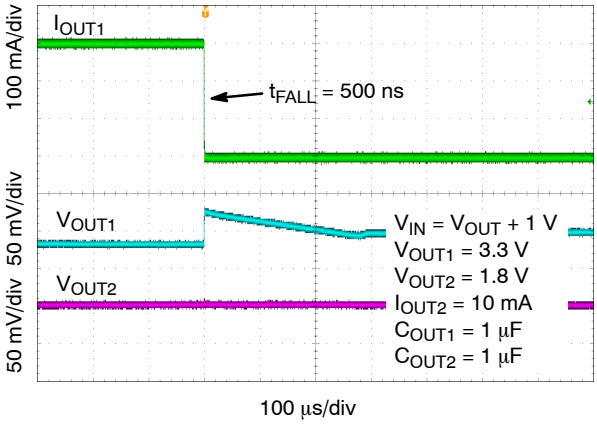


Figure 43. Load Transient Response – 3.3 V – Falling Edge, I_{OUT1} = 300 mA to 100 μA

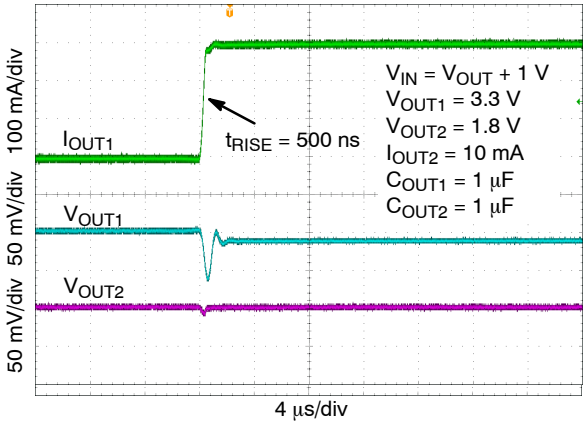


Figure 44. Load Transient Response – 3.3 V – Rising Edge, I_{OUT1} = 1 mA to 300 mA

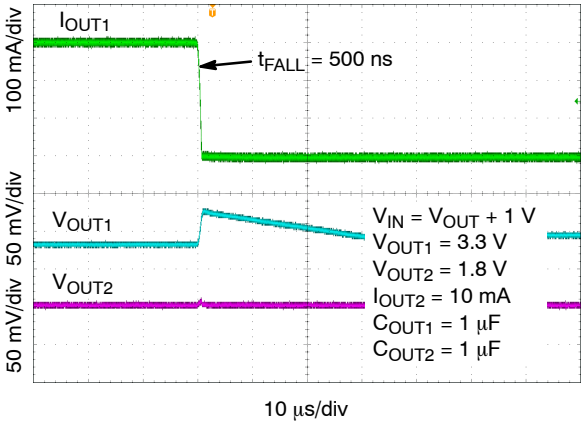


Figure 45. Load Transient Response – 3.3 V – Falling Edge, I_{OUT1} = 300 mA to 1 mA

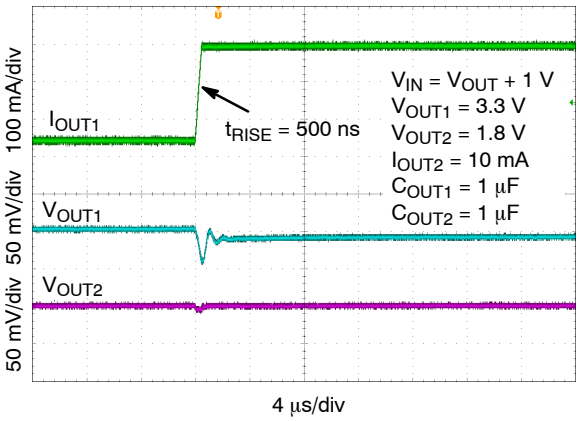


Figure 46. Load Transient Response – 3.3 V – Rising Edge, I_{OUT} = 50 mA to 300 mA

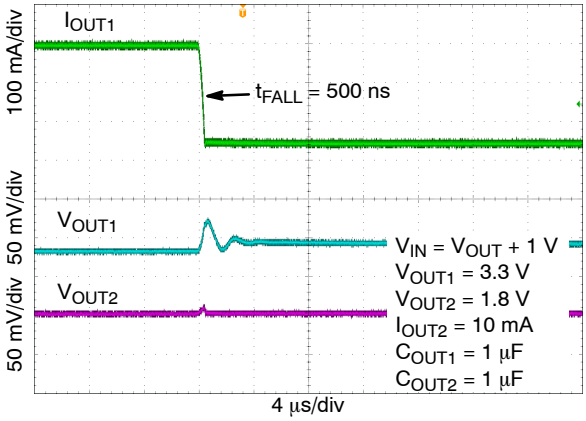


Figure 47. Load Transient Response – Falling Edge, I_{OUT} = 300 mA to 50 mA

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TYPICAL CHARACTERISTICS

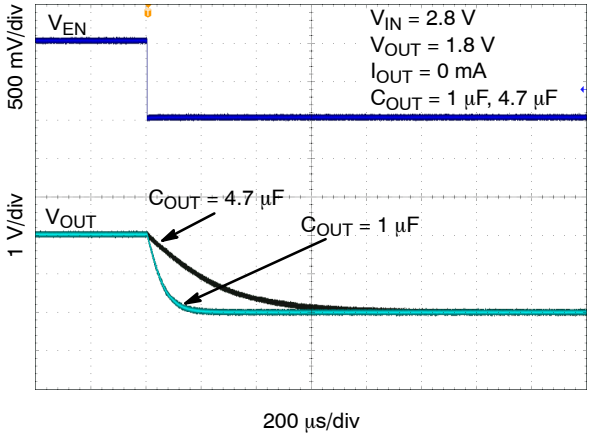


Figure 48. Enable Turn-off, V_{OUT} = 1.8 V

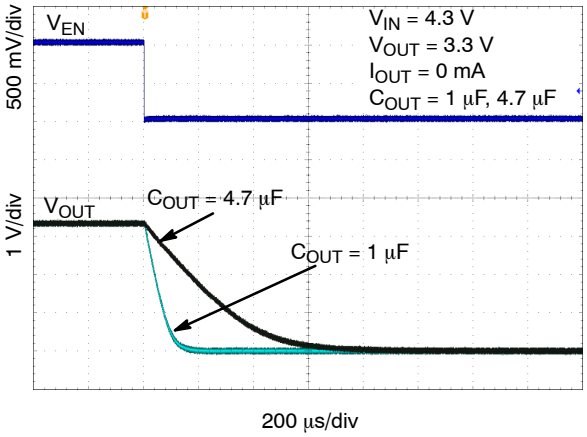


Figure 49. Enable Turn-off, V_{OUT} = 3.3 V

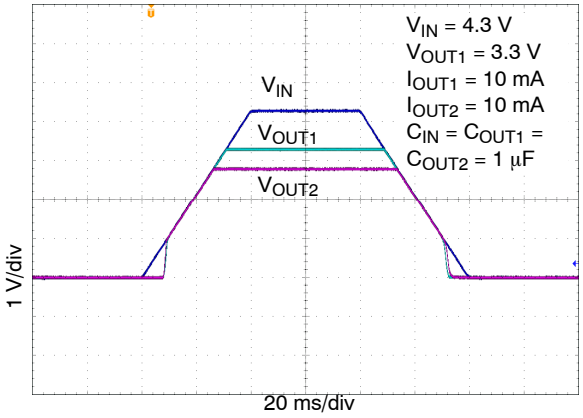


Figure 50. Turn-on/off – Slow Rising V_{IN}

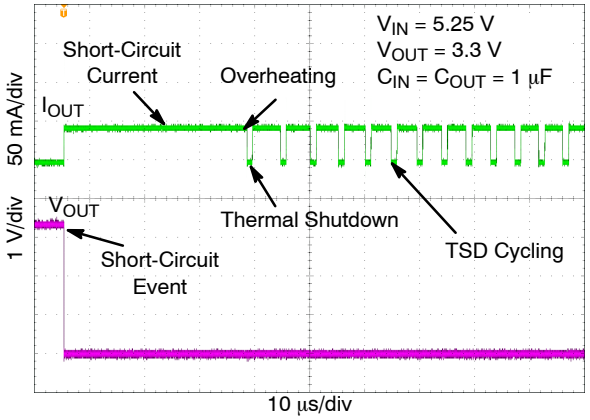


Figure 51. Short-Circuit and Thermal Shutdown

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General

The NCV8154 is a dual output high performance 300 mA Low Dropout Linear Regulator. This device delivers very high PSRR (75 dB at 1 kHz) and excellent dynamic performance as load/line transients. In connection with low quiescent current this device is very suitable for various battery powered applications such as tablets, cellular phones, wireless and many others. Each output is fully protected in case of output overload, output short circuit condition and overheating, assuring a very robust design. The NCV8154 device is housed in DFN10 3 x3 mm package which is useful for space constrains application.

Input Capacitor Selection (C_{IN})

It is recommended to connect at least a 1 μF Ceramic X5R or X7R capacitor as close as possible to the IN pin of the device. This capacitor will provide a low impedance path for unwanted AC signals or noise modulated onto constant input voltage. There is no requirement for the min. or max. ESR of the input capacitor but it is recommended to use ceramic capacitors for their low ESR and ESL. A good input capacitor will limit the influence of input trace inductance and source resistance during sudden load current changes. Larger input capacitor may be necessary if fast and large load transients are encountered in the application.

Output Decoupling (C_{OUT})

The NCV8154 requires an output capacitor for each output connected as close as possible to the output pin of the regulator. The recommended capacitor value is 1 μF and X7R or X5R dielectric due to its low capacitance variations over the specified temperature range. The NCV8154 is designed to remain stable with minimum effective capacitance of 0.33 μF to account for changes with temperature, DC bias and package size. Especially for small package size capacitors such as 0201 the effective capacitance drops rapidly with the applied DC bias.

There is no requirement for the minimum value of Equivalent Series Resistance (ESR) for the C_{OUT} but the maximum value of ESR should be less than 3 Ω. Larger output capacitors and lower ESR could improve the load transient response or high frequency PSRR. It is not recommended to use tantalum capacitors on the output due to their large ESR. The equivalent series resistance of tantalum capacitors is also strongly dependent on the temperature, increasing at low temperature.

Enable Operation

The NCV8154 uses the dedicated EN pin for each output channel. This feature allows driving outputs separately.

If the EN pin voltage is <0.4 V the device is guaranteed to be disabled. The pass transistor is turned-off so that there is virtually no current flow between the IN and OUT. The active discharge transistor is active so that the output voltage V_{OUT} is pulled to GND through a 50 Ω resistor. In the disable state the device consumes as low as typ. 10 nA from the V_{IN}.

If the EN pin voltage >0.9 V the device is guaranteed to be enabled. The NCV8154 regulates the output voltage and the active discharge transistor is turned-off.

The both EN pin has internal pull-down current source with typ. value of 300 nA which assures that the device is turned-off when the EN pin is not connected. In the case where the EN function isn't required the EN should be tied directly to IN.

Output Current Limit

Output Current is internally limited within the IC to a typical 400 mA. The NCV8154 will source this amount of current measured with a voltage drops on the 90% of the nominal V_{OUT}. If the Output Voltage is directly shorted to ground (V_{OUT} = 0 V), the short circuit protection will limit the output current to 520 mA (typ). The current limit and short circuit protection will work properly over whole temperature range and also input voltage range. There is no limitation for the short circuit duration. This protection works separately for each channel. Short circuit on the one channel do not influence second channel which will work according to specification.

Thermal Shutdown

When the die temperature exceeds the Thermal Shutdown threshold (T_{SD} − 160 °C typical), Thermal Shutdown event is detected and the affected channel is turn-off. Second channel still working. The channel which is overheated will remain in this state until the die temperature decreases below the Thermal Shutdown Reset threshold (T_{SDU} − 140 °C typical). Once the device temperature falls below the 140 °C the appropriate channel is enabled again. The thermal shutdown feature provides the protection from a catastrophic device failure due to accidental overheating. This protection is not intended to be used as a substitute for proper heat sinking. The long duration of the short circuit condition to some output channel could cause turn-off other output when heat sinking is not enough and temperature of the other output reach T_{SD} temperature.

Power Dissipation

As power dissipated in the NCV8154 increases, it might become necessary to provide some thermal relief. The maximum power dissipation supported by the device is dependent upon board design and layout. Mounting pad configuration on the PCB, the board material, and the ambient temperature affect the rate of junction temperature rise for the part. For reliable operation, junction temperature should be limited to +125 °C.

The maximum power dissipation the NCV8154 can handle is given by:

$$P_{D(MAX)} = \frac{\left[T_{J(MAX)} - T_A\right]}{\theta_{JA}} \qquad \text{(eq. 1)}$$

The power dissipated by the NCV8154 for given application conditions can be calculated from the following equations:

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$$P_D \approx (V_{IN1} \cdot I_{GND1}) + (V_{IN2} \cdot I_{GND2}) + \\ + I_{OUT1}(V_{IN1} - V_{OUT1}) + I_{OUT2}(V_{IN2} - V_{OUT2}) \quad \text{(eq. 2)}$$

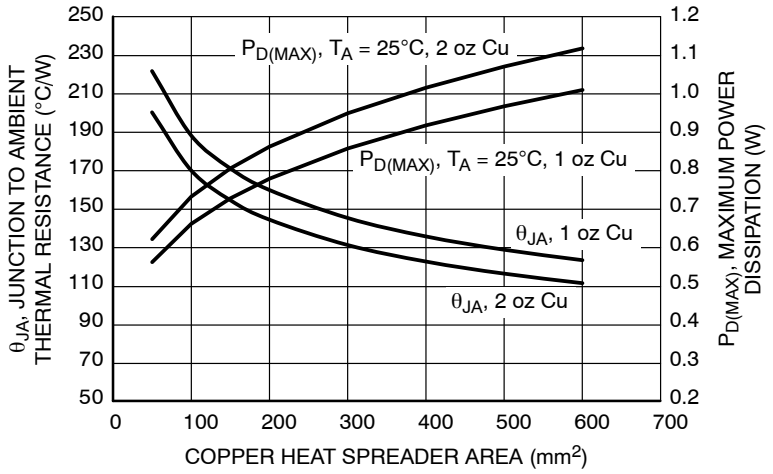


Figure 52. θ_{JA} and $P_{D(MAX)}$ vs. Copper Area – DFN10

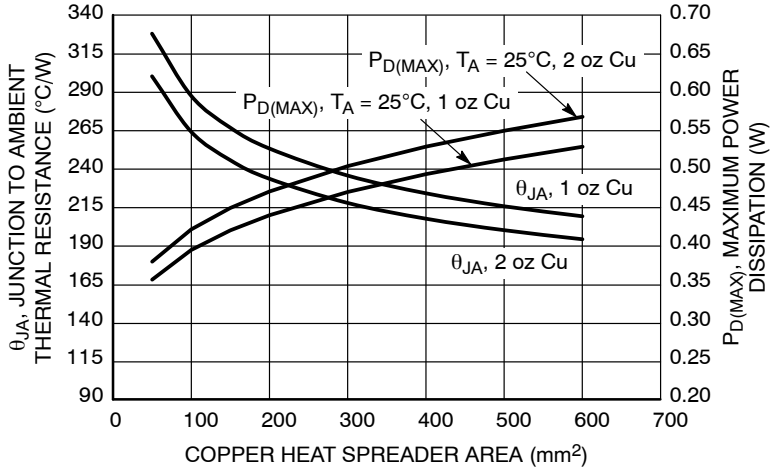


Figure 53. θ_{JA} and $P_{D(MAX)}$ vs. Copper Area – WDFN6

Reverse Current

The PMOS pass transistor has an inherent body diode which will be forward biased in the case that $V_{OUT} > V_{IN}$. Due to this fact in cases, where the extended reverse current condition can be anticipated the device may require additional external protection.

Power Supply Rejection Ratio

The NCV8154 features very good Power Supply Rejection ratio. If desired the PSRR at higher frequencies in the range 100 kHz – 10 MHz can be tuned by the selection of C_{OUT} capacitor and proper PCB layout.

Turn-On Time

The turn-on time is defined as the time period from EN assertion to the point in which V_{OUT} will reach 98% of its nominal value. This time is dependent on various application conditions such as $V_{OUT(NOM)}$, C_{OUT}, T_A.

PCB Layout Recommendations

To obtain good transient performance and good regulation characteristics place input and output capacitors close to the device pins and make the PCB traces wide. In order to minimize the solution size, use 0402 capacitors. Larger copper area connected to the pins will also improve the device thermal resistance. The actual power dissipation can be calculated from the equation above (Equation 2). Expose pad should be tied the shortest path to the GND pin.

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Table 6. ORDERING INFORMATION

Device	Marking	Voltage Option (OUT1/OUT2)	Active Discharge	Features	Package	Shipping†
NCV8154MW120180TBG	8154W 1218	1.2 V / 1.8 V	Yes	Wettable Flank	DFN10 (Pb-Free)	3000 / Tape & Reel
NCV8154MW120280TBG	8154W 1228	1.2 V / 2.8 V	Yes			
NCV8154MW150180TBG	8154W 1518	1.5 V / 1.8 V	Yes			
NCV8154MW150330TBG	8154W 1533	1.5 V / 3.3 V	Yes			
NCV8154MW180250TBG	8154W 1825	1.8 V / 2.5 V	Yes			
NCV8154MW180280TBG	8154W 1828	1.8 V / 2.8 V	Yes			
NCV8154MW280120TBG	8154W 2812	2.8 V / 1.2 V	Yes			
NCV8154MN300300TBG	8154N 3030	3.0 V / 3.0 V	Yes	Non-wettable Flank		
NCV8154MW300300TBG	8154W 3030		Yes	Wettable Flank		
NCV8154MW330180TBG	8154W 3318	3.3 V / 1.8 V	Yes	Wettable Flank		
NCV8154MW330280TBG	8154W 3328	3.3 V / 2.8 V	Yes	Wettable Flank		
NCV8154MW330330TBG	8154W 3333	3.3 V / 3.3 V	Yes			
NCV8154MTW180280TCG	DA	1.8 V / 2.8 V	No	Wettable Flank	WDFN6 (Pb-Free)	3000 / Tape & Reel

DISCONTINUED (Note 7)

NCV8154MN330180TBG	8154N 3318	3.3 V / 1.8 V	Yes	Non-wettable Flank	DFN10 (Pb-Free)	3000 / Tape & Reel

† For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

7. **DISCONTINUED:** This device is not available. Please contact your **onsemi** representative for information. The most current information on this device may be available on www.onsemi.com.

Bluetooth is a registered trademark of Bluetooth SIG.
ZigBee is a registered trademark of ZigBee Alliance.

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REVISION HISTORY

Revision	Description of Changes	Date
12	Rebranded the Data Sheet to **onsemi** format. NCV8154MN330180TBG OPN Marked as Discontinued.	2/23/2026

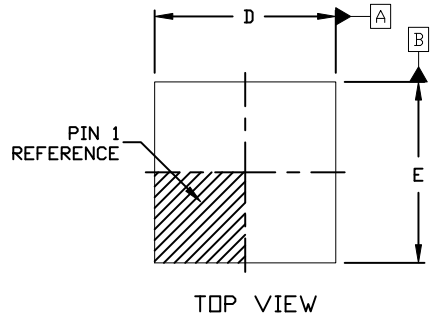
This document has undergone updates prior to the inclusion of this revision history table. The changes tracked here only reflect updates made on the noted approval dates.

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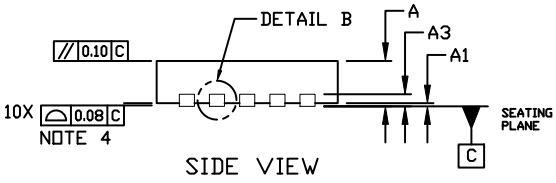
DFN10, 3x3, 0.5P
CASE 485C
ISSUE F

DATE 16 DEC 2021

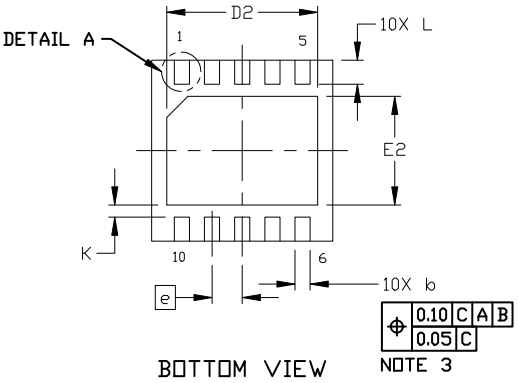
SCALE 2:1



TOP VIEW

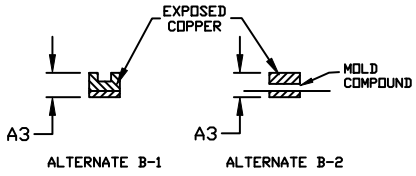


SIDE VIEW

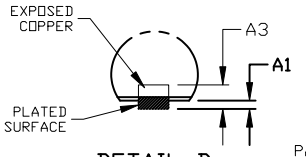


BOTTOM VIEW

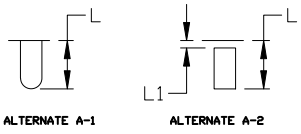
NOTES:
1. DIMENSION AND TOLERANCING PER ASME Y14.5, 2009.
2. CONTROLLING DIMENSION: MILLIMETERS
3. DIMENSION b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.15 AND 0.30 MM FROM THE TERMINAL TIP.
4. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.
5. TERMINAL b MAY HAVE MOLD COMPOUND MATERIAL ALONG SIDE EDGE. MOLD FLASH MAY NOT EXCEED 30 MICRONS ONTO BOTTOM SURFACE OF TERMINAL.
6. FOR DEVICE OPN CONTAINING W OPTION, DETAIL A AND DETAIL B ALTERNATE CONSTRUCTIONS ARE NOT APPLICABLE. WETTABLE FLANK CONSTRUCTION IS DETAIL B AS SHOWN ON SIDE VIEW OF PACKAGE.



DETAIL B
ALTERNATE CONSTRUCTION

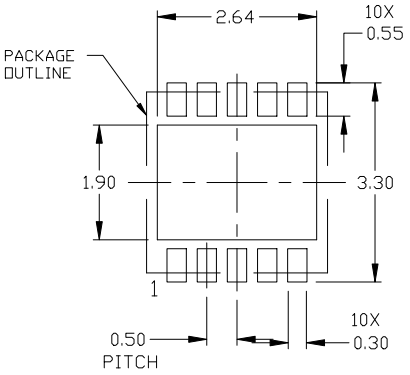


DETAIL B
WETTABLE FLANK
CONSTRUCTION



DETAIL A
ALTERNATE CONSTRUCTION

DIM	MILLIMETERS		
	MIN.	NOM.	MAX.
A	0.80	0.90	1.00
A1	0.00	---	0.05
A3		0.20 REF	
b	0.18	0.23	0.30
D	2.90	3.00	3.10
D2	2.40	2.50	2.60
E	2.90	3.00	3.10
E2	1.70	1.80	1.90
e		0.50 BSC	
K		0.20 REF	
L	0.30	0.40	0.50
L1	---	---	0.03



RECOMMENDED
MOUNTING FOOTPRINT

For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

GENERIC
MARKING DIAGRAM*



XXXXX = Specific Device Code
A = Assembly Location
L = Wafer Lot
Y = Year
W = Work Week
▪ = Pb−Free Package

(Note: Microdot may be in either location)

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, “G” or microdot “▪”, may or may not be present. Some products may not follow the Generic Marking.

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DESCRIPTION:	**DFN10, 3X3 MM, 0.5 MM PITCH**		**PAGE 1 OF 1**

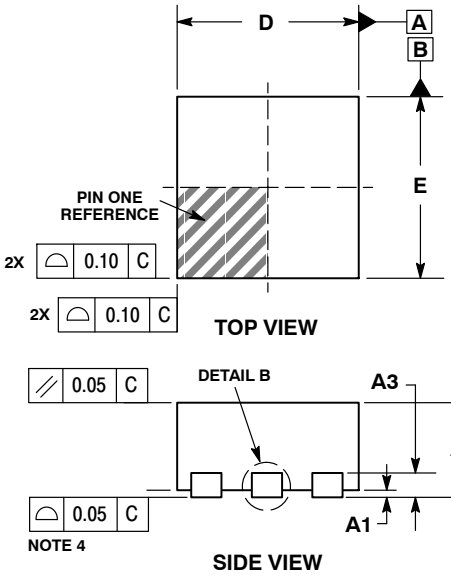
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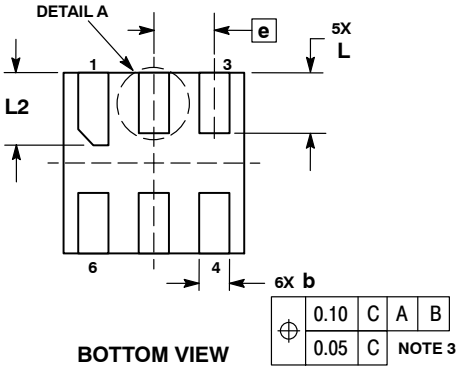
WDFN6 1.5x1.5, 0.5P
CASE 511BJ
ISSUE C

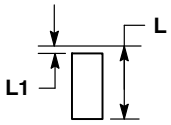
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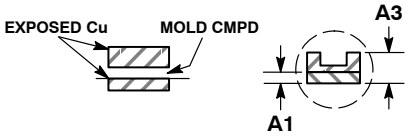
SCALE 4:1







DETAIL A
ALTERNATE TERMINAL CONSTRUCTIONS

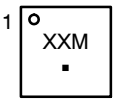


DETAIL B
ALTERNATE CONSTRUCTIONS

NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSION b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.15 AND 0.30mm FROM TERMINAL TIP.
4. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.

	MILLIMETERS	
DIM	MIN	MAX
A	0.70	0.80
A1	0.00	0.05
A3	0.20 REF	
b	0.20	0.30
D	1.50 BSC	
E	1.50 BSC	
e	0.50 BSC	
L	0.40	0.60
L1	---	0.15
L2	0.50	0.70

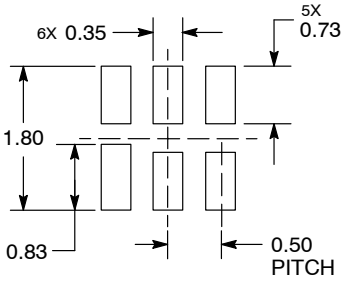
GENERIC MARKING DIAGRAM*



XX = Specific Device Code
M = Date Code
▪ = Pb−Free Package

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, “G” or microdot “ ▪”, may or may not be present.

RECOMMENDED MOUNTING FOOTPRINT*



DIMENSIONS: MILLIMETERS

*For additional information on our Pb−Free strategy and soldering details, please download the **onsemi** Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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DESCRIPTION:	**WDFN6, 1.5 X 1.5, 0.5 P**		**PAGE 1 OF 1**

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