LDO Regulator, 300 mA, Low Dropout Voltage, Ultra Low Noise, High PSRR with Power Good
NCV8164

The NCV8164 is a 300 mA LDO, next generation of high PSRR, ultra−low noise and low dropout regulators with Power Good open collector output. Designed to meet the requirements of RF and sensitive analog circuits, the NCV8164 device provides ultra−low noise, high PSRR and low quiescent current. The device also offer excellent load/line transients. The NCV8164 is designed to work with a 1 μF input and a 1 μF output ceramic capacitor. It is available in industry standard TSOP−5, WDFNW6 0.65P, 2 mm x 2 mm and DFNW8 0.65P, 3 mm x 3 mm.

Features

- Operating Input Voltage Range: 1.6 V to 5.5 V
- Available in Fixed Voltage Option: 1.2 V to 5.0 V
- Adjustable Version Reference Voltage: 1.2 V
- ±2% Accuracy Over Load and Temperature
- Ultra Low Quiescent Current Typ. 30 μA
- Standby Current: Typ. 0.1 μA
- Very Low Dropout: 110 mV at 300 mA for 3.3 V Variant
- Ultra High PSRR: Typ. 85 dB at 10 mA, f = 1 kHz
- Ultra Low Noise: 9 μV_{RMS} (Fixed Version)
- Stable with a 1 μF Small Case Size Ceramic Capacitors
- Available in – TSOP−5 3 mm x 1.5 mm x 1 mm CASE 483
  - WDFNW6 2 mm x 2 mm x 0.75 mm CASE 511DW
  - DFNW8 3 mm x 3 mm x 0.9 mm CASE 507AD
- NCV Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements
- AEC−Q100 Qualified and PPAP Capable
- These Devices are Pb−Free, Halogen Free/BFR Free and are RoHS Compliant

Typical Applications

- Communication Systems
- In−Vehicle Networking
- Telematics, Infotainment and Clusters
- General Purpose Automotive

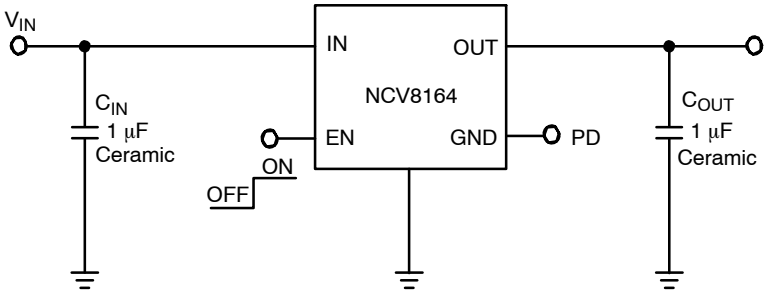
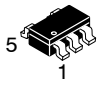
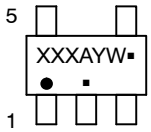


Figure 1. Typical Application Schematics

MARKING DIAGRAMS

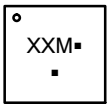


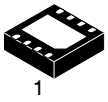
TSOP−5
CASE 483



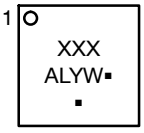


WDFNW6 2x2, 0.65P
CASE 511DW





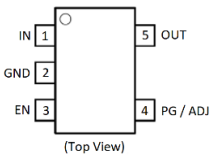
DFNW8 3x3, 0.65P
CASE 507AD

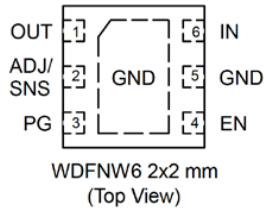


XXX = Specific Device Code
A = Assembly Location
L = Wafer Lot
M = Month Code
Y = Year
W = Work Week
▪ = Pb−Free Package

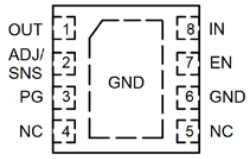
(Note: Microdot may be in either location)

PIN CONNECTONS





WDFNW6 2x2 mm
(Top View)



DFNW8 3x3 mm
(Top View)

ORDERING INFORMATION

See detailed ordering, marking and shipping information on page 10 of this data sheet.

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PIN FUNCTION DESCRIPTION

Pin No. TSOP−5	Pin No. WDFNW6	Pin No. DFNW8	Pin Name	Description
1	6	8	IN	Input voltage supply pin
5	1	1	OUT	Regulated output voltage. The output should be bypassed with small 1 μF ceramic capacitor
3	4	7	EN	Chip enable: Applying V_{EN} < 0.25 V disables the regulator, Pulling V_{EN} > 0.7 V enables the LDO
4 / –	3	3	PG	Power Good, open collector. Use 10 kΩ to 100 kΩ pull−up resistor connected to output or input voltage
2	5	6	GND	Common ground connection
– / 4	2	2	ADJ	Adjustable output feedback pin (for adjustable version only)
–	2	2	SNS	Sense feedback pin. Must be connected to OUT pin on PCB (for fixed versions only)
–	–	4, 5	N/C	Not connected, pin can be tied to ground plane for better power dissipation
–	EPAD	EPAD	EPAD	Expose pad should be tied to ground plane for better power dissipation

ABSOLUTE MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Input Voltage (Note 1)	V_{IN}	−0.3 to 6	V
Output Voltage	V_{OUT}	−0.3 to V_{IN}+0.3, max. 6	V
Chip Enable Input	V_{CE}	−0.3 to 6	V
Power Good Voltage	V_{PG}	−0.3 to 6	V
Power Good Current	I_{PG}	30	mA
Output Short Circuit Duration	t_{SC}	unlimited	s
Maximum Junction Temperature	T_J	150	°C
Storage Temperature	T_{STG}	−55 to 150	°C
ESD Capability, Human Body Model (Note 2)	ESD_{HBM}	2000	V
ESD Capability, Charged Device Model (Note 2)	ESD_{CDM}	1000	V

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. Refer to ELECTRICAL CHARACTERISTIS and APPLICATION INFORMATION for Safe Operating Area.
2. This device series incorporates ESD protection and is tested by the following methods:
   ESD Human Body Model tested per AEC−Q100−002 (EIA/JESD22−A114)
   ESD Charged Device Model tested per EIA/JESD22−C101, Field Induced Charge Model

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THERMAL CHARACTERISTICS

Rating	Symbol	Value	Unit
THERMAL CHARACTERISTICS, TSOP−5 PACKAGE			
Thermal Resistance, Junction−to−Ambient (Note 3)	$R_{\theta JA}$	158	°C/W
Thermal Resistance, Junction−to−Case (top)	$R_{\theta JC(top)}$	155	°C/W
Thermal Resistance, Junction−to−Case (bottom) (Note 4)	$R_{\theta JC(bot)}$	102	°C/W
Thermal Resistance, Junction−to−Board	$R_{\theta JB}$	197	°C/W
Characterization Parameter, Junction−to−Top	Ψ_{JT}	40	°C/W
Characterization Parameter, Junction−to−Board	Ψ_{JB}	82	°C/W
THERMAL CHARACTERISTICS, WDFNW6−2X2, 0.65 PITCH PACKAGE			
Thermal Resistance, Junction−to−Ambient (Note 3)	$R_{\theta JA}$	51	°C/W
Thermal Resistance, Junction−to−Case (top)	$R_{\theta JC(top)}$	142	°C/W
Thermal Resistance, Junction−to−Case (bottom) (Note 4)	$R_{\theta JC(bot)}$	2.0	°C/W
Thermal Resistance, Junction−to−Board	$R_{\theta JB}$	117	°C/W
Characterization Parameter, Junction−to−Top	Ψ_{JT}	1.9	°C/W
Characterization Parameter, Junction−to−Board	Ψ_{JB}	7.7	°C/W
THERMAL CHARACTERISTICS, DFNW8−3X3, 0.65 PITCH PACKAGE			
Thermal Resistance, Junction−to−Ambient (Note 3)	$R_{\theta JA}$	50	°C/W
Thermal Resistance, Junction−to−Case (top)	$R_{\theta JC(top)}$	142	°C/W
Thermal Resistance, Junction−to−Case (bottom) (Note 4)	$R_{\theta JC(bot)}$	7.9	°C/W
Thermal Resistance, Junction−to−Board	$R_{\theta JB}$	125	°C/W
Characterization Parameter, Junction−to−Top	Ψ_{JT}	2.0	°C/W
Characterization Parameter, Junction−to−Board	Ψ_{JB}	7.5	°C/W

3. The junction−to−ambient thermal resistance under natural convection is obtained in a simulation on a high−K board, following the JEDEC51.7 guidelines with assumptions as above, in an environment described in JESD51−2a.
4. The junction−to−case (bottom) thermal resistance is obtained by simulating a cold plate test on the IC exposed pad. Test description can be found in the ANSI SEMI standard G30−88.

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ELECTRICAL CHARACTERISTICS

($-40°C \le T_J \le 150°C$; $V_{IN} = V_{OUT(NOM)} + 0.5$ V; $I_{OUT} = 1$ mA, $C_{IN} = C_{OUT} = 1$ μF, $V_{EN} = V_{IN}$, unless otherwise noted. Typical values are at $T_J = +25°C$ (Note 5))

Parameter	Test Conditions		Symbol	Min	Typ	Max	Unit
Operating Input Voltage			V_{IN}	1.6		5.5	V
Output Voltage Accuracy	$V_{IN} = V_{OUT(NOM)} + 0.5$ V to 5.5 V, $0.1 \text{ mA} \le I_{OUT} \le 300$ mA		V_{OUT}	−2		+2	%
Reference Voltage (Adjustable Ver. ADJ pin connected to OUT)	$V_{IN} = 1.6$ V to 5.5 V, $0.1 \text{ mA} \le I_{OUT} \le 300$ mA		V_{ADJ}	1.176	1.2	1.224	V
Line Regulation	$V_{OUT(NOM)} + 0.5 \text{ V} \le V_{IN} \le 5.5$ V		$Line_{Reg}$		0.5		mV/V
Load Regulation	$I_{OUT} = 1$ mA to 300 mA		$Load_{Reg}$		2		mV
Dropout Voltage (Note 6) TSOP−5, WDFNW6	$I_{OUT} = 300$ mA	$V_{OUT(NOM)} = 1.5$ V	V_{DO}		170	295	mV
		$V_{OUT(NOM)} = 1.8$ V			155	255	
		$V_{OUT(NOM)} = 2.5$ V			125	200	
		$V_{OUT(NOM)} = 2.8$ V			115	185	
		$V_{OUT(NOM)} = 3.0$ V			113	177	
		$V_{OUT(NOM)} = 3.3$ V			110	170	
		$V_{OUT(NOM)} = 5.0$ V			95	135	
Dropout Voltage (Note 6) DFNW8	$I_{OUT} = 300$ mA	$V_{OUT(NOM)} = 1.5$ V	V_{DO}		180	315	mV
		$V_{OUT(NOM)} = 1.8$ V			165	275	
		$V_{OUT(NOM)} = 2.5$ V			140	220	
		$V_{OUT(NOM)} = 2.8$ V			130	205	
		$V_{OUT(NOM)} = 3.0$ V			127	197	
		$V_{OUT(NOM)} = 3.3$ V			125	190	
		$V_{OUT(NOM)} = 5.0$ V			112	170	
Output Current Limit	$V_{OUT} = 90\% V_{OUT(NOM)}$		I_{CL}	350	560		mA
Short Circuit Current	$V_{OUT} = 0$ V		I_{SC}		580		
Quiescent Current	$I_{OUT} = 0$ mA		I_Q		30	40	μA
Shutdown Current	$V_{EN} \le 0.25$ V		I_{DIS}		0.01	1.5	μA
EN Pin Threshold Voltage	EN Input Voltage “H”		V_{ENH}	0.7			V
	EN Input Voltage “L”		V_{ENL}			0.25	
EN Pull Down Current	$V_{EN} = 5.5$ V		I_{EN}		0.2	0.6	μA
Power Good Threshold Voltage	Output Voltage Raising		V_{PGUP}		95		%
	Output Voltage Falling		V_{PGDW}		90		
Power Good Output Voltage Low	IPG = 5 mA, Open drain		V_{PGLO}			0.3	V
Turn−On Time (Note 7)	$C_{OUT} = 1$ μF, From assertion of V_{EN} to $V_{OUT} = 95\% V_{OUT(NOM)}$				120		μs

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ELECTRICAL CHARACTERISTICS (continued)
($-40°C \le T_J \le 150°C$; $V_{IN} = V_{OUT(NOM)} + 0.5$ V; $I_{OUT} = 1$ mA, $C_{IN} = C_{OUT} = 1$ μF, $V_{EN} = V_{IN}$, unless otherwise noted. Typical values are at $T_J = +25°C$ (Note 5))

Parameter	Test Conditions		Symbol	Min	Typ	Max	Unit
Power Supply Rejection Ratio (Note 7)	$V_{OUT(NOM)}$ = 3.3 V, I_{OUT} = 10 mA	f = 100 Hz	P_{SRR}		83		dB
		f = 1 kHz			85		
		f = 10 kHz			80		
		f = 100 kHz			61		
Output Voltage Noise (Fixed Ver.)	f = 10 Hz to 100 kHz	I_{OUT} = 10 mA	V_N		9		μV_{RMS}
Thermal Shutdown Threshold (Note 7)	Temperature rising		T_{SDH}		165		°C
	Temperature hysteresis		T_{HYST}		15		°C
Active output discharge resistance	V_{EN} < 0.25 V, Version A only		R_{DIS}		260		Ω

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

5. Performance guaranteed over the indicated operating temperature range by design and/or characterization. Production tested at $T_J = T_A = 25°C$.
6. Low duty cycle pulse techniques are used during the testing to maintain the junction temperature as close to ambient as possible. Dropout voltage is characterized when V_{OUT} falls 3% below $V_{OUT(NOM)}$.
7. Guaranteed by design and characterization.

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TYPICAL CHARACTERISTICS

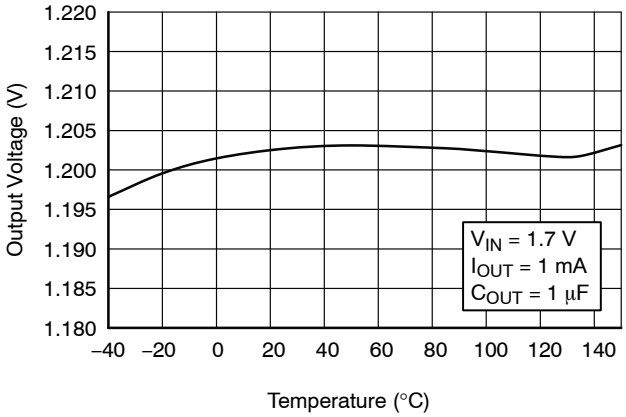

Figure 2. Output Voltage vs. Temperature – V_{OUT} = 1.2 V

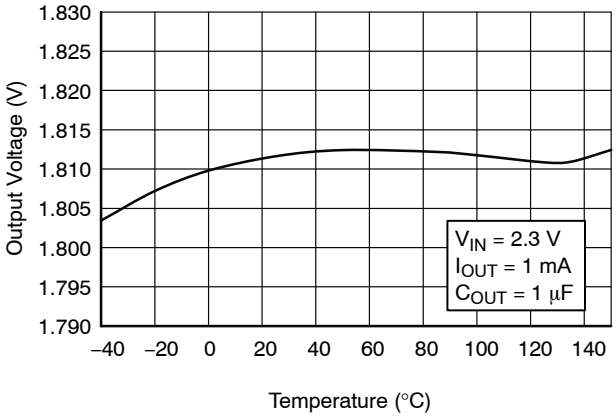

Figure 3. Output Voltage vs. Temperature – V_{OUT} = 1.8 V

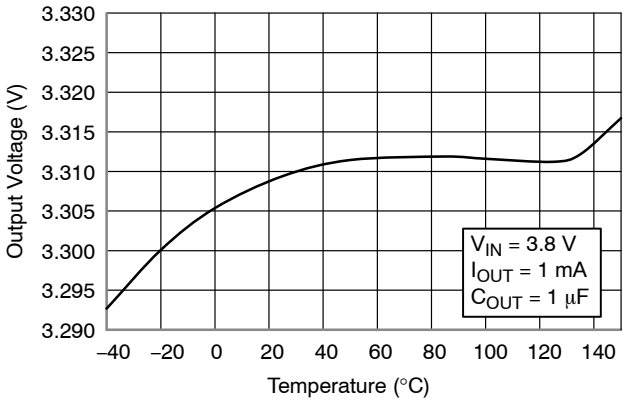

Figure 4. Output Voltage vs. Temperature – V_{OUT} = 3.3 V

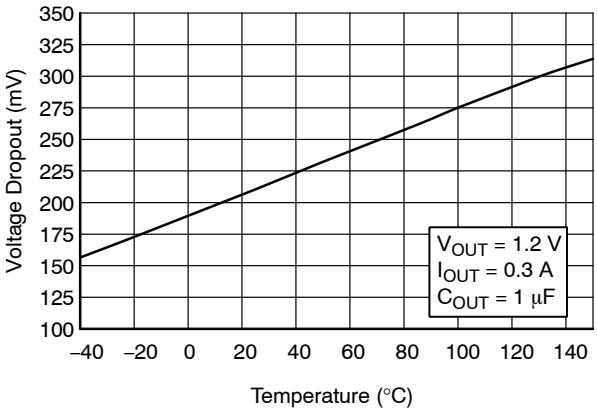

Figure 5. Dropout Voltage vs. Temperature – V_{OUT} = 1.2 V

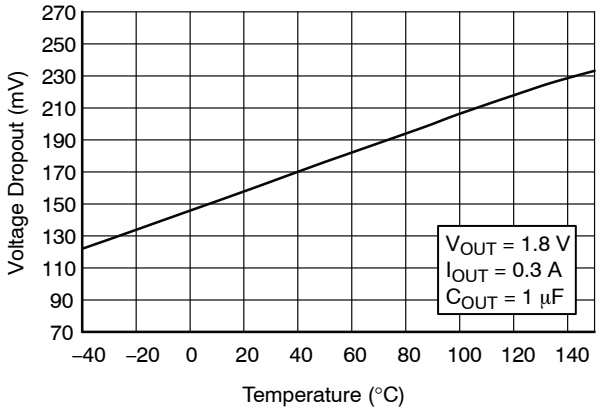

Figure 6. Dropout Voltage vs. Temperature – V_{OUT} = 1.8 V

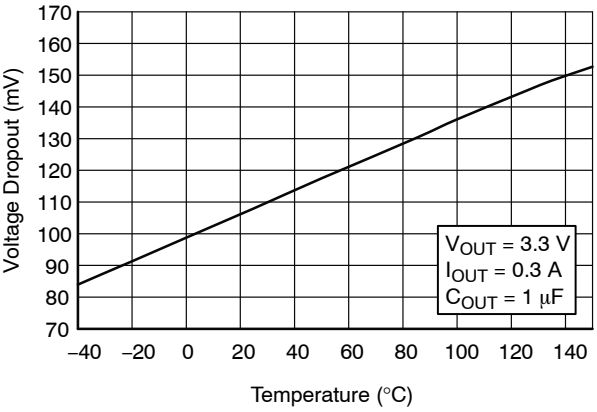

Figure 7. Dropout Voltage vs. Temperature – V_{OUT} = 3.3 V

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TYPICAL CHARACTERISTICS (continued)

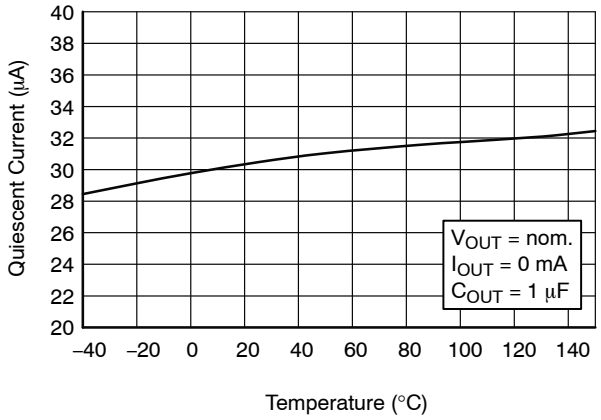

Figure 8. Quiescent Current va Temperature

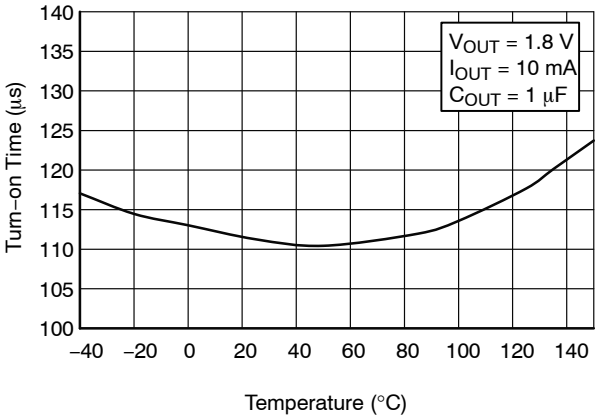

Figure 9. Turn−on Time vs. Temperature

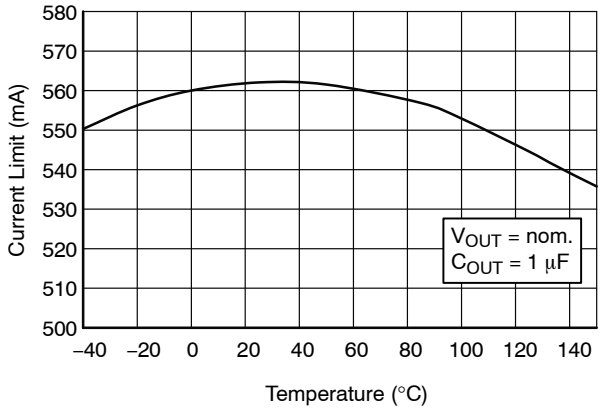

Figure 10. Current Limit vs. Temperature

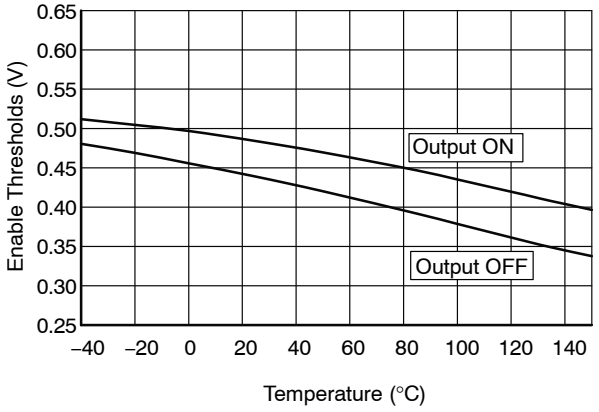

Figure 11. Enable Thresholds vs Temperature

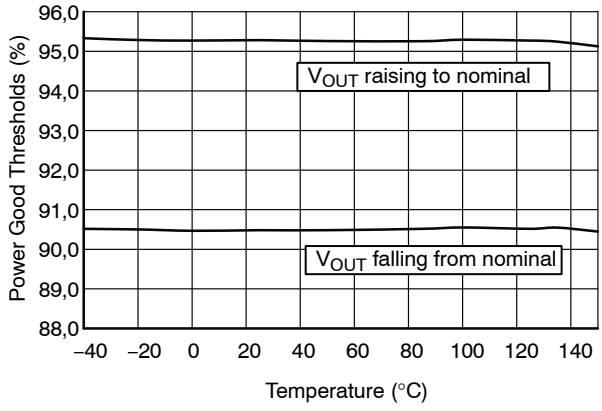

Figure 12. Power Good Threshold vs. Temperature

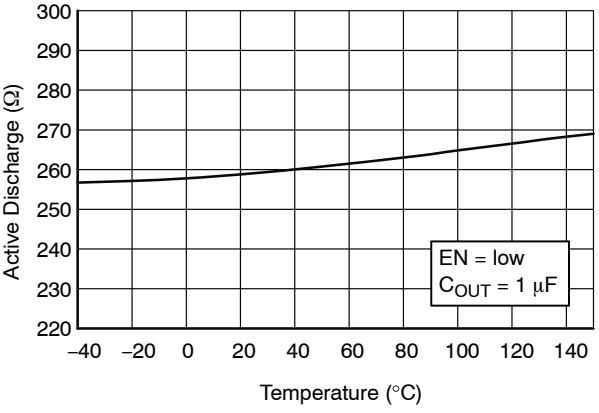

Figure 13. Active Discharge Resistance vs. Temperature

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TYPICAL CHARACTERISTICS (continued)

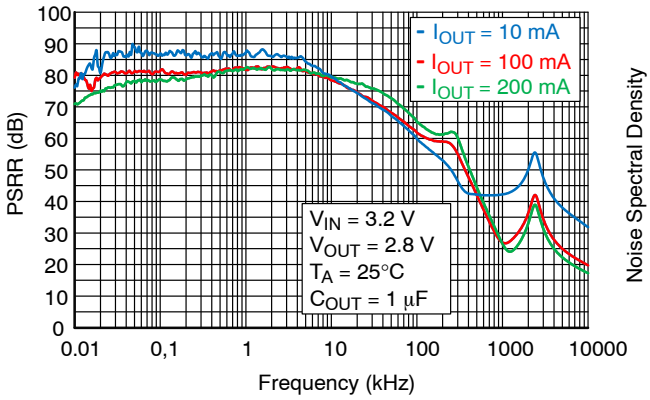

Figure 14. Power Supply Rejection Ration for V_{OUT} = 2.8 V, C_{OUT} = 1 μF

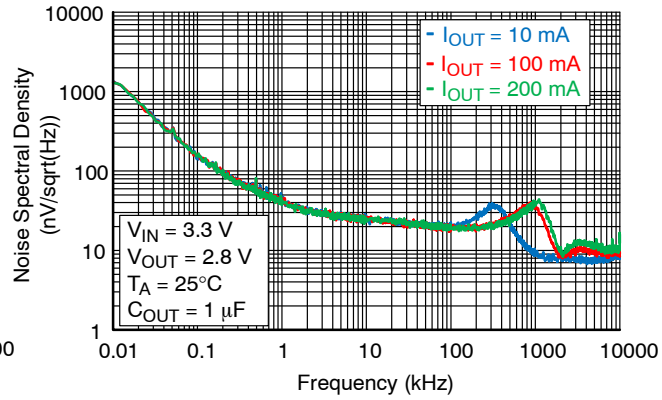

Figure 15. Output Voltage Noise Spectral Density for V_{OUT} = 2.8 V, C_{OUT} = 1 μF

APPLICATIONS INFORMATION

The NCV8164 is the member of new family of high output current and low dropout regulators which delivers low quiescent and ground current consumption, good noise and power supply ripple rejection ratio performance. The NCV8164 incorporates EN pin and power good output for simple controlling by MCU or logic. Standard features include current limiting, soft−start feature and thermal protection.

Input Decoupling (C_{IN})

It is recommended to connect at least 1 μF ceramic X5R or X7R capacitor between IN and GND pin of the device. This capacitor will provide a low impedance path for any unwanted AC signals or noise superimposed onto constant input voltage. The good input capacitor will limit the influence of input trace inductances and source resistance during sudden load current changes. Higher capacitance and lower ESR capacitors will improve the overall line transient response.

Output Decoupling (C_{OUT})

The NCV8164 does not require a minimum Equivalent Series Resistance (ESR) for the output capacitor. The device is designed to be stable with standard ceramics capacitors with values of 1 μF or greater. The X5R and X7R types have the lowest capacitance variations over temperature thus they are recommended.

Power Good Output Connection

The NCV8164 include Power Good functionality for better interfacing to MCU system. Power Good output is open collector type, capable to sink up to 10 mA. Recommended operating current is between 10 mA and 1 mA to obtain low saturation voltage. External pull−up resistor can be connected to any voltage up to 5.5 V (please see Absolute Maximum Ratings table above). Please note that Power Good internal circuitry is non−functional (disabled) to achieve the lowest possible internal current consumption in case of disabled LDO through Enable input (EN = Low). In this case internal Power Good transistor is open and output logic level is defined by voltage used for pull−up resistor. When Power Good is intended to be used as part of power sequencing functionality, then please connect external pull−up resistor to output voltage of NCV8164. This will allow you to get correct low PG signal when LDO is disabled. Active discharge option is recommended to discharge output capacitors connected to LDO.

Power Dissipation and Heat Sinking

The maximum power dissipation supported by the device is dependent upon board design and layout. Mounting pad configuration on the PCB, the board material, and the ambient temperature affect the rate of junction temperature rise for the part. For reliable operation junction temperature should be limited to +125°C, however device is capable to work up to junction temperature +150°C. The maximum power dissipation the NCV8164 can handle is given by:

$$P_{D(MAX)} = \frac{\left[T_{J(MAX)} - T_A\right]}{R_{\theta JA}} \quad \text{(eq. 1)}$$

The power dissipated by the NCV8164 for given application conditions can be calculated from the following equations:

$$P_D \approx V_{IN}(I_{GND}(I_{OUT})) + I_{OUT}\,(V_{IN} - V_{OUT}) \quad \text{(eq. 2)}$$

or

$$V_{IN(MAX)} \approx \frac{P_{D(MAX)} + \left(V_{OUT} \times I_{OUT}\right)}{I_{OUT} + I_{GND}} \quad \text{(eq. 3)}$$

Hints

VIN and GND printed circuit board traces should be as wide as possible. When the impedance of these traces is high, there is a chance to pick up noise or cause the regulator to malfunction. Place external components, especially the output capacitor, as close as possible to the NCV8164, and make traces as short as possible.

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Adjustable Version

Not only adjustable version, but also any fixed version can be used to create adjustable voltage, where original fixed voltage becomes reference voltage for resistor divider and feedback loop. Output voltage can be equal or higher than original fixed option, while possible range is from 1.2 V up to 5.0 V. Figure 16 shows how to add external resistors to increase output voltage above fixed value.

Output voltage is then given by equation

$$V_{OUT} = V_{FIX} \times (1 + R1/R2) \quad \text{(eq. 4)}$$

where V_{FIX} is voltage of original fixed version (from 1.2 V up to 5.0 V) or adjustable version (1.2 V). Do not operate the device at output voltage about 5.2 V, as device can be damaged.

In order to avoid influence of current flowing into SNS pin to output voltage accuracy (SNS current varies with voltage option and temperature, typical value is 300 nA) it is recommended to use values of R1 and R2 below 500 kΩ.

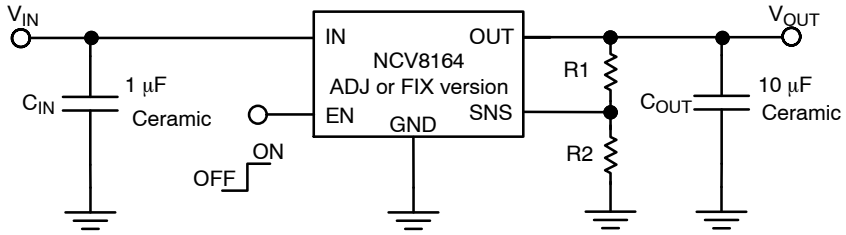

Figure 16. Adjustable Variant Application

Please note that output noise is amplified by V_{OUT} / V_{FIX} ratio. For example, if original 1.2 V fixed variant is used to create 3.6 V output voltage, output noise is increased 3.6 / 1.2 = 3 times and real value will be 3 × 9 μVrms = 27 μVrms. For noise sensitive applications it is recommended to use as high fixed variant as possible – for example in case above it is better to use 3.3 V fixed variant to create 3.6 V output voltage, as output noise will be amplified only 3.6 / 3.3 = 1.09 × (9.8 μVrms).

Share Feedback
Your Opinion Matters

ORDERING INFORMATION

Device part no.	Voltage Option	Marking	Option	Package	Shipping †
NCV8164ASNADJT1G	ADJ	M2	With Active Output Discharge	TSOP−5 (Pb−Free)	3000 / Tape & Reel
NCV8164ASN120T1G	1.2 V	MA	With Active Output Discharge		
NCV8164ASN150T1G	1.5 V	MN	With Active Output Discharge		
NCV8164ASN180T1G	1.8 V	MJ	With Active Output Discharge		
NCV8164ASN250T1G	2.5 V	MP	With Active Output Discharge		
NCV8164ASN280T1G	2.8 V	MK	With Active Output Discharge		
NCV8164ASN300T1G	3.0 V	MQ	With Active Output Discharge		
NCV8164ASN330T1G	3.3 V	ML	With Active Output Discharge		
NCV8164AMTWADJTAG	ADJ	L3	With Active Output Discharge	WDFNW6 (WF, Pb−Free)	3000 / Tape & Reel
NCV8164AMTW110TAG	1.1 V	LC	With Active Output Discharge		
NCV8164AMTW120TAG	1.2 V	LA	With Active Output Discharge		
NCV8164AMTW180TAG	1.8 V	LJ	With Active Output Discharge		
NCV8164AMTW280TAG	2.8 V	LK	With Active Output Discharge		
NCV8164AMTW290TAG	2.9 V	LH	With Active Output Discharge		
NCV8164AMLADJTCG	ADJ	K2	With Active Output Discharge	DFNW8 (WF, Pb−Free)	3000 / Tape & Reel
NCV8164AML120TCG	1.2 V	KA	With Active Output Discharge		
NCV8164AML150TCG	1.5 V	KN	With Active Output Discharge		
NCV8164AML180TBG	1.8 V	KJ	With Active Output Discharge		
NCV8164AML180TCG	1.8 V	KJ	With Active Output Discharge		
NCV8164AML250TCG	2.5 V	KP	With Active Output Discharge		
NCV8164AML280TCG	2.8 V	KK	With Active Output Discharge		
NCV8164AML300TCG	3.0 V	KQ	With Active Output Discharge		
NCV8164AML330TCG	3.3 V	KL	With Active Output Discharge		

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

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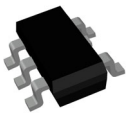
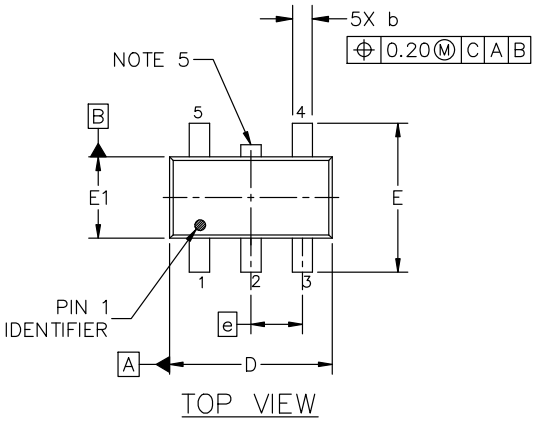
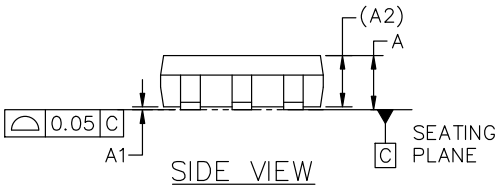


TSOP−5 3.00x1.50x0.95, 0.95P
CASE 483
ISSUE P

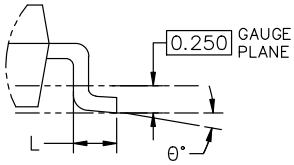
DATE 01 APR 2024



TOP VIEW



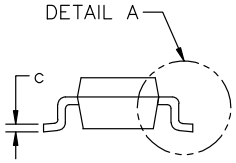
SIDE VIEW



DETAIL "A"
SCALE 2:1

NOTES:

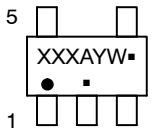
1. DIMENSIONING AND TOLERANCING CONFORM TO ASME Y14.5−2018.
2. ALL DIMENSION ARE IN MILLIMETERS (ANGLES IN DEGREES).
3. MAXIMUM LEAD THICKNESS INCLUDES LEAD FINISH THICKNESS. MINIMUM LEAD THICKNESS IS THE MINIMUM THICKNESS OF BASE MATERIAL.
4. DIMENSIONS D AND E1 DO NOT INCLUDE MOLD FLASH, PROTRUSIONS OF GATE BURRS. MOLD FLASH, PROTRUSIONS, OR GATE BURRS SHALL NOT EXCEED 0.15 PER SIDE. DIMENSION D.
5. OPTIONAL CONSTRUCTION: AN ADDITIONAL TRIMMED LEAD IS ALLOWED IN THIS LOCATION. TRIMMED LEAD NOT TO EXTEND MORE THAN 0.2 FROM BODY.



END VIEW

DIM	MILLIMETERS		
	MIN.	NOM.	MAX.
A	0.900	1.000	1.100
A1	0.010	0.055	0.100
A2		0.950 REF.	
b	0.250	0.375	0.500
c	0.100	0.180	0.260
D	2.850	3.000	3.150
E	2.500	2.750	3.000
E1	1.350	1.500	1.650
e		0.950 BSC	
L	0.200	0.400	0.600
θ	0°	5°	10°

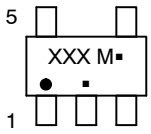
GENERIC
MARKING DIAGRAM*



Analog

XXX = Specific Device Code
A = Assembly Location
Y = Year
W = Work Week
▪ = Pb−Free Package

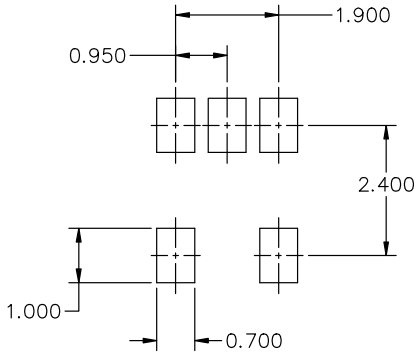
(Note: Microdot may be in either location)



Discrete/Logic

XXX = Specific Device Code
M = Date Code
▪ = Pb−Free Package

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, "G" or microdot "▪", may or may not be present. Some products may not follow the Generic Marking.



RECOMMENDED MOUNTING FOOTPRINT*

* FOR ADDITIONAL INFORMATION ON OUR Pb−FREE STRATEGY AND SOLDERING DETAILS, PLEASE DOWNLOAD THE ON SEMICONDUCTOR SOLDERING AND MOUNTING TECHNIQUES REFERENCE MANUAL, SOLDERRM/D.

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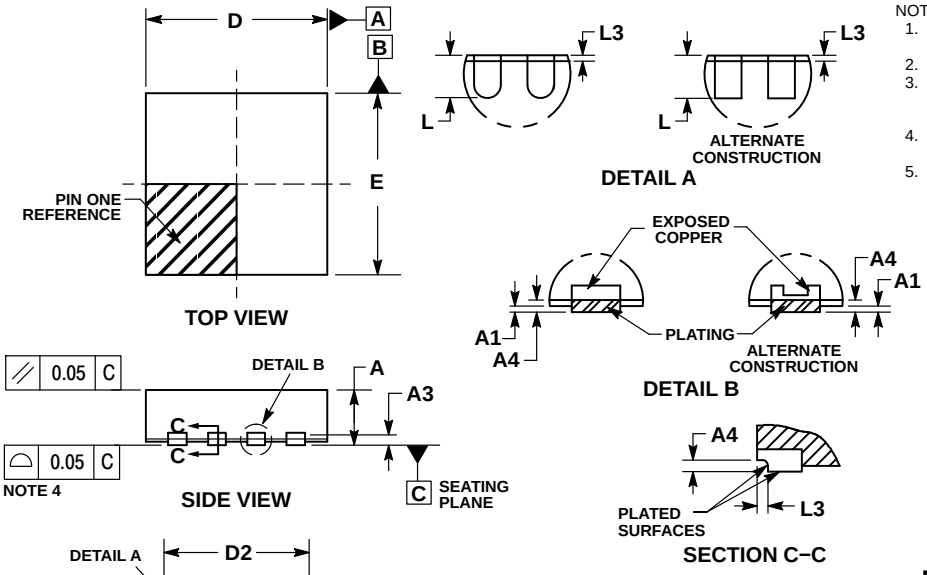
SCALE 2:1

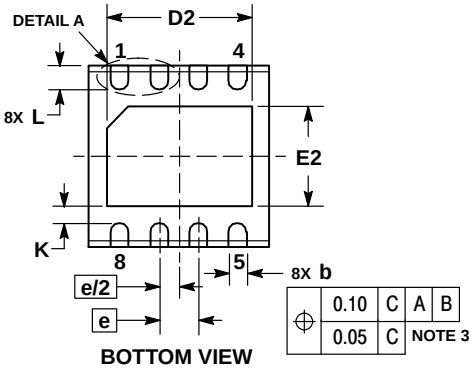
DFNW8 3x3, 0.65P
CASE 507AD
ISSUE A

DATE 15 JUN 2018

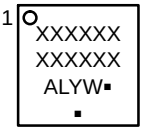


NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSION b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.15 AND 0.30mm FROM THE TERMINAL TIP.
4. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.
5. THIS DEVICE CONTAINS WETTABLE FLANK DESIGN FEATURE TO AID IN FILLET FORMATION ON THE LEADS DURING MOUNTING.

	MILLIMETERS		
DIM	MIN	NOM	MAX
A	0.80	0.90	1.00
A1	−−−	−−−	0.05
A3		0.20 REF	
A4	0.10	−−−	−−−
b	0.25	0.30	0.35
D	2.90	3.00	3.10
D2	2.30	2.40	2.50
E	2.90	3.00	3.10
E2	1.55	1.65	1.75
e		0.65 BSC	
K		0.28 REF	
L	0.30	0.40	0.50
L3		0.05 REF	



GENERIC MARKING DIAGRAM*

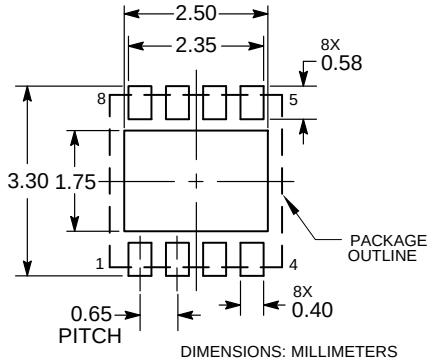


XXXXXX = Specific Device Code
A = Assembly Location
L = Wafer Lot
Y = Year
W = Work Week
▪ = Pb−Free Package

(Note: Microdot may be in either location)

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, “G” or microdot “ ▪”, may or may not be present. Some products may not follow the Generic Marking.

RECOMMENDED SOLDERING FOOTPRINT*



DIMENSIONS: MILLIMETERS

*For additional information on our Pb−Free strategy and soldering details, please download the **onsemi** Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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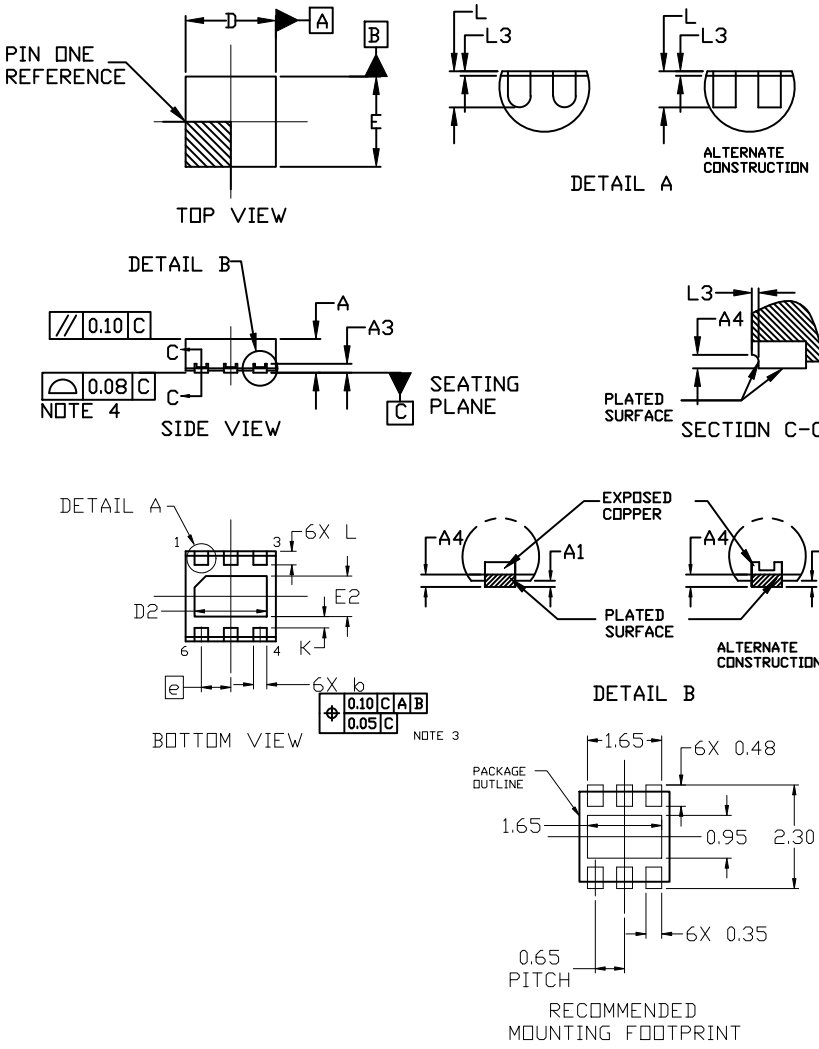
WDFNW6 2x2, 0.65P
CASE 511DW
ISSUE B

DATE 15 JUN 2018



SCALE 4:1

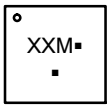


NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS
3. DIMENSION b APPLIES TO PLATED TERMINALS AND IS MEASURED BETWEEN 0.15 AND 0.30MM FROM THE TERMINAL TIP.
4. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.
5. THIS DEVICE CONTAINS WETTABLE FLANK DESIGN FEATURES TO AID IN FILLET FORMATION ON THE LEADS DURING MOUNTING.

DIM	MILLIMETERS		
	MIN.	NOM.	MAX.
A	0.70	0.75	0.80
A1	---	---	0.05
A3	0.20 REF		
A4	0.10	---	---
b	0.25	0.30	0.35
D	1.90	2.00	2.10
D2	1.50	1.60	1.70
E	1.90	2.00	2.10
E2	0.80	0.90	1.00
e	0.65 BSC		
K	0.25 REF		
L	0.25	0.30	0.35
L3	0.05 REF		

GENERIC MARKING DIAGRAM*



M = Month Code
▪ = Pb−Free Package

(Note: Microdot may be in either location)

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, “G” or microdot “ ▪”, may or may not be present. Some products may not follow the Generic Marking.

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