Voltage Regulator - Low Iq, Low Dropout, Power Good Output
1.2 A

NCV8187

The NCV8187 is 1.2 A LDO Linear Voltage Regulator. It is a very stable and accurate device with low quiescent current consumption (typ. 30 μA over the full temperature range), low dropout, low output noise and very good PSRR. The regulator incorporates several protection features such as Thermal Shutdown, Soft Start, Current Limiting and also Power Good Output signal for easy MCU interfacing.

Features

- Operating Input Voltage Range: 1.5 V to 5.5 V
- Adjustable and Fixed Voltage Options Available: 0.8 V to 5.2 V
- Low Quiescent Current: typ. 30 μA over Temperature
- ±2% Accuracy Over Full Load, Line and Temperature variations
- PSRR: 75 dB at 1 kHz
- Low Noise: typ. 15 μV_{RMS} from 10 Hz to 100 kHz
- Stable With Small 10 μF Ceramic Capacitor
- Soft−start to Reduce Inrush Current and Overshoots
- Thermal Shutdown and Current Limit Protection
- Power Good Signal Extends Application Range
- Available in WDFN6 and WDFNW6 2x2, DFN6 3x3, DFNW6 3x3, DFNW8 3x3 and DPAK−5 with Wettable Flank (pin edge plating)
- NCV Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC−Q100 Qualified and PPAP Capable
- These Devices are Pb−Free, Halogen Free/BFR Free and are RoHS Compliant

Typical Applications

- Wireless Chargers and Portable Equipment
- Smart Camera and Robotic Vision Systems
- Telecommunication and Networking Systems
- Infotainment and Cluster
- Modular Platforms for Dashboard Display
- Internet Connection Sharing (ICS) Gateway Server Applications
- General Purpose Automotive

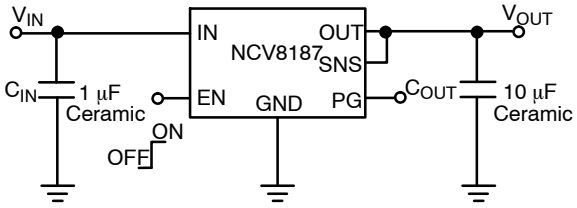
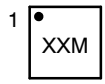


Figure 1. Typical Application Schematic

GENERIC MARKING DIAGRAMS

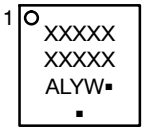


WDFN6/WDFNW6 2x2
CASE 511BR & 511DW



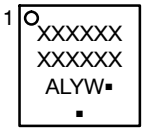


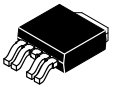
DFN6/DFNW6 3x3
CASE 506DK & 507AW



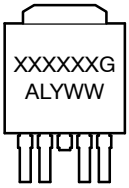


DFNW8 3x3
CASE 507AD





DPAK−5
CASE 175AA



XXXXXX = Specific Device Code
A = Assembly Location
L = Wafer Lot
Y = Year
W/WW = Work Week
D = Date Code
▪/G = Pb−Free Package

(Note: Microdot may be in either location)

ORDERING INFORMATION

See detailed ordering and shipping information on page 12 of this data sheet.

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PIN FUNCTION CONNECTION

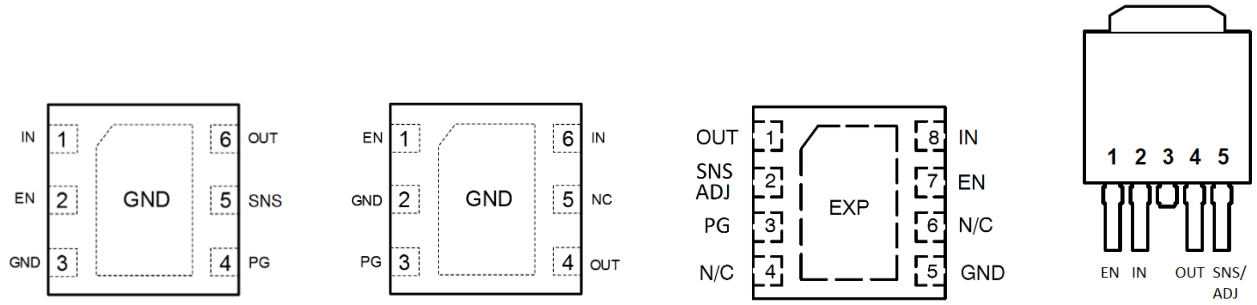

Figure 2. Pin Function Connection

PIN FUNCTION DESCRIPTION

Pin No. WDFN6 & WDFNW6 2x2	Pin No. DFN6 & DFNW6 3x3	Pin No. DFNW8 3x3	Pin No. DPAK−5	Pin Name	Description
1	6	8	2	IN	Input pin. A small capacitor is needed from this pin to ground to assure stability
6	4	1	4	OUT	Regulated output voltage pin. A small 10 μF ceramic capacitor is needed from this pin to ground to assure stability
3, EXP	2, EXP	5, EXP	TAB	GND	Power supply ground
2	1	7	1	EN	Enable pin. Driving this pin high turns on the regulator. Driving EN pin low puts the regulator into shutdown mode
5	–	2 / –	5 / –	SNS	Sense pin. Connect this pin to regulated output voltage
–	–	– / 2	– / 5	ADJ	Adjustable feedback voltage input. Connect this pin to external resistor divider for desired voltage output
4	3	3	–	PG	Power Good, open collector. Use 10 kΩ to 100 kΩ pull−up resistor connected to output or input voltage
–	5	4, 6	–	NC	No connection. This pin can be tied to ground to improve thermal dissipation or left disconnected

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ABSOLUTE MAXIMUM RATINGS

Ratings	Symbol	Value	Unit
Input Voltage (Note 1)	V_{IN}	−0.3 to 6	V
Enable Voltage	V_{EN}	−0.3 to 6	V
Power Good Current	I_{PG}	30	mA
Power Good Voltage	V_{PG}	−0.3 to 6	V
Output Voltage	V_{OUT}	−0.3 to V_{IN} + 0.3 (max. 5.5)	V
Output Short Circuit Duration	t_{SC}	Indefinite	s
Maximum Junction Temperature	$T_{J(MAX)}$	150	°C
Storage Temperature	T_{STG}	−55 to 150	°C
ESD Capability, Human Body Model (Note 2)	ESD_{HBM}	2000	V
ESD Capability, Machine Model (Note 2)	ESD_{MM}	200	V

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. Refer to ELECTRICAL CHARACTERISTICS and APPLICATION INFORMATION for Safe Operating Area.
2. This device series incorporates ESD protection and is tested by the following methods:
   ESD Human Body Model tested per AEC−Q100−002 (EIA/JESD22−A114)
   ESD Machine Model tested per AEC−Q100−003 (EIA/JESD22−A115)

THERMAL CHARACTERISTICS

Rating	Symbol	Value	Unit
THERMAL CHARACTERISTICS, WDFN6, 2x2, 0.65 PITCH PACKAGE			
Thermal Resistance, Junction−to−Ambient (Note 3)	$R_{\theta JA}$	51	°C/W
Thermal Resistance, Junction−to−Case (top)	$R_{\theta JC(top)}$	142	°C/W
Thermal Resistance, Junction−to−Case (bottom) (Note 4)	$R_{\theta JC(bot)}$	7.8	°C/W
Thermal Resistance, Junction−to−Board	$R_{\theta JB}$	125	°C/W
Characterization Parameter, Junction−to−Top	Ψ_{JT}	2.0	°C/W
Characterization Parameter, Junction−to−Board	Ψ_{JB}	7.7	°C/W
THERMAL CHARACTERISTICS, DFN6 / DFNW6, 3x3, 0.95 PITCH PACKAGES			
Thermal Resistance, Junction−to−Ambient (Note 3)	$R_{\theta JA}$	50	°C/W
Thermal Resistance, Junction−to−Case (top)	$R_{\theta JC(top)}$	142	°C/W
Thermal Resistance, Junction−to−Case (bottom) (Note 4)	$R_{\theta JC(bot)}$	7.9	°C/W
Thermal Resistance, Junction−to−Board	$R_{\theta JB}$	125	°C/W
Characterization Parameter, Junction−to−Top	Ψ_{JT}	2.0	°C/W
Characterization Parameter, Junction−to−Board	Ψ_{JB}	7.5	°C/W

3. The junction−to−ambient thermal resistance under natural convection is obtained in a simulation on a high−K board, following the JEDEC51.7 guidelines with assumptions as above, in an environment described in JESD51−2a.
4. The junction−to−case (bottom) thermal resistance is obtained by simulating a cold plate test on the IC exposed pad. Test description can be found in the ANSI SEMI standard G30−88.

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ELECTRICAL CHARACTERISTICS – WDFN6 2x2, WDFNW6 2x2, DFN6 3x3 AND DFNW6 3x3 ($-40°C \le T_J \le 150°C$; $V_{IN} = V_{OUT} + 1.0$ V; I_{OUT} = 10 mA, C_{IN} = 1 μF, C_{OUT} = 10 μF, unless otherwise noted. Typical values are at T_J = +25°C. (Note 6))

Parameter	Test Conditions		Symbol	Min	Typ	Max	Unit
Operating Input Voltage			V_{IN}	1.5	–	5.5	V
Output Voltage Accuracy	$-40°C \le T_J \le 150°C$, V_{OUT} +1 V < V_{IN} < 5.5 V, 0 mA < I_{OUT} < 1.2 A	V_{OUT} < 1.7 V	V_{OUT}	–35 mV	–	+35 mV	V
		$V_{OUT} \ge$ 1.7 V		–2%	–	+2%	
Reference Voltage			V_{REF}	–	0.8	–	V
Line Regulation	V_{OUT} + 1 V ≤ V_{IN} ≤ 5.5 V, I_{OUT} = 1 mA		Reg_{LINE}	–	40	–	μV/V
Load Regulation	I_{OUT} = 0 mA to 1.2 A		Reg_{LOAD}	–	2	–	μV/mA
Dropout Voltage	$V_{DO} = V_{IN} - (V_{OUT(NOM)} - 3\%)$, I_{OUT} = 1.2 A	1.2 V – 1.4 V	V_{DO}	–	325	495	mV
		1.5 V – 1.7 V		–	240	400	
		1.8 V – 2.7 V		–	200	335	
		2.8 V – 3.2 V		–	165	250	
		3.3 V – 4.9 V		–	150	220	
		5 V		–	120	180	
Maximum Output Current	(Note 7)		I_{OUT}	1300	1750	–	mA
Short Circuit Current	(Note 7)		I_{SC}	–	1850	–	mA
Disable Current	V_{EN} = 0 V		I_{DIS}	–	0.1	5.0	μA
Quiescent Current	I_{OUT} = 0 mA		I_Q	–	30	45	μA
Ground Current	I_{OUT} = 1.2 A		I_{GND}	–	2	–	mA
Power Supply Rejection Ratio	V_{IN} = 3.5 V + 100 mVpp, V_{OUT} = 2.5 V, I_{OUT} = 10 mA, C_{OUT} = 1 μF	f = 1 kHz	PSRR	–	75	–	dB
Output Noise Voltage	V_{OUT} = 1.8 V, I_{OUT} = 10 mA, f = 10 Hz to 100 kHz		V_N	–	15	–	μV_{rms}
Enable Input Threshold Voltage	Voltage increasing		V_{EN_HI}	0.9	–	–	V
	Voltage decreasing		V_{EN_LO}	–	–	0.3	
EN Pin Current	V_{EN} = 5.5 V			–	100	–	nA
Active Output Discharge Resistance	V_{IN} = 5.5 V, V_{EN} = 0 V		R_{DIS}	–	120	–	Ω
Power Good, Output Voltage Raising			V_{PGup}	–	92	–	%
Power Good, Output Voltage Falling			V_{PGdw}	–	80	–	%
Power Good Output Voltage Low	I_{PG} = 6 mA, Open drain		V_{PGlo}	–	0.14	0.4	V
Thermal Shutdown Temperature (Note 5)	Temperature increasing from T_J = +25°C		T_{SD}	–	170	–	°C
Thermal Shutdown Hysteresis (Note 5)	Temperature falling from TSD		T_{SDH}	–	15	–	°C

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

5. Guaranteed by design and characterization.
6. Performance guaranteed over the indicated operating temperature range by design and/or characterization production tested at T_J = T_A = 25°C. Low duty cycle pulse techniques are used during testing to maintain the junction temperature as close to ambient as possible.
7. Respect SOA.

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ELECTRICAL CHARACTERISTICS – DFNW8 3x3 AND DPAK–5 ($-40°C \le T_J \le 150°C$; $V_{IN} = V_{OUT} + 1.0$ V; $I_{OUT} = 10$ mA, $C_{IN} = 1$ μF, $C_{OUT} = 10$ μF, unless otherwise noted. Typical values are at $T_J = +25°C$. (Note 9))

Parameter	Test Conditions		Symbol	Min	Typ	Max	Unit
Operating Input Voltage			V_{IN}	1.5	–	5.5	V
Output Voltage Accuracy	$-40°C \le T_J \le 150°C$, $V_{OUT} + 1$ V < V_{IN} < 5.5 V, 0 mA < I_{OUT} < 1 A	V_{OUT} < 1.7 V	V_{OUT}	–35 mV	–	+35 mV	V
		$V_{OUT} \ge 1.7$ V		–2%	–	+2%	
Reference Voltage			V_{REF}	–	1.2	–	V
Line Regulation	$V_{OUT} + 1$ V ≤ V_{IN} ≤ 5.5 V, I_{OUT} = 1 mA		Reg_{LINE}	–	40	–	μV/V
Load Regulation	I_{OUT} = 0 mA to 1 A		Reg_{LOAD}	–	2	–	μV/mA
Dropout Voltage	$V_{DO} = V_{IN} - (V_{OUT(NOM)} - 3\%)$, I_{OUT} = 1 A	1.2 V – 1.4 V	V_{DO}	–	295	450	mV
		1.5 V – 1.7 V		–	220	360	
		1.8 V – 2.7 V		–	180	305	
		2.8 V – 3.2 V		–	150	225	
		3.3 V – 4.9 V		–	135	200	
		5 V		–	110	165	
Maximum Output Current	(Note 10), $T_J = 25°C$		I_{OUT}	1025	1500	1750	mA
Maximum Output Current	(Note 10)		I_{OUT}	1025	1500	1950	mA
Short Circuit Current	(Note 10)		I_{SC}	–	1550	–	mA
Disable Current	V_{EN} = 0 V		I_{DIS}	–	0.1	5.0	μA
Quiescent Current	I_{OUT} = 0 mA		I_Q	–	30	45	μA
Ground Current	I_{OUT} = 1 A		I_{GND}	–	2	–	mA
Power Supply Rejection Ratio	V_{IN} = 3.5 V + 100 mVpp, V_{OUT} = 2.5 V, I_{OUT} = 10 mA, C_{OUT} = 1 μF	f = 1 kHz	PSRR	–	75	–	dB
Output Noise Voltage	V_{OUT} = 1.8 V, I_{OUT} = 10 mA, f = 10 Hz to 100 kHz		V_N	–	15	–	μV_{rms}
Enable Input Threshold Voltage	Voltage increasing		V_{EN_HI}	0.9	–	–	V
	Voltage decreasing		V_{EN_LO}	–	–	0.3	
EN Pin Current	V_{EN} = 5.5 V			–	100	–	nA
Active Output Discharge Resistance	V_{IN} = 5.5 V, V_{EN} = 0 V		R_{DIS}	–	120	–	Ω
Power Good, Output Voltage Raising			V_{PGup}	–	92	–	%
Power Good, Output Voltage Falling			V_{PGdw}	–	80	–	%
Power Good Output Voltage Low	I_{PG} = 6 mA, Open drain		V_{PGlo}	–	0.14	0.4	V
Thermal Shutdown Temperature (Note 8)	Temperature increasing from $T_J = +25°C$		T_{SD}	–	170	–	°C
Thermal Shutdown Hysteresis (Note 8)	Temperature falling from TSD		T_{SDH}	–	15	–	°C

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

8. Guaranteed by design and characterization.
9. Performance guaranteed over the indicated operating temperature range by design and/or characterization production tested at $T_J = T_A = 25°C$. Low duty cycle pulse techniques are used during testing to maintain the junction temperature as close to ambient as possible.
10. Respect SOA.

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TYPICAL CHARACTERISTICS

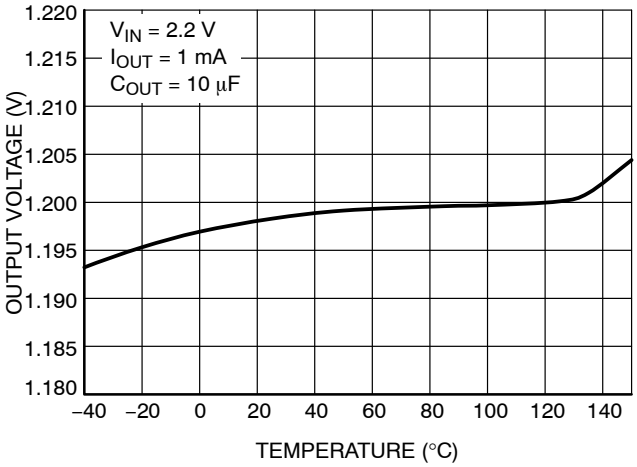

Figure 3. Output Voltage vs. Temperature – V_{OUT} = 1.2 V

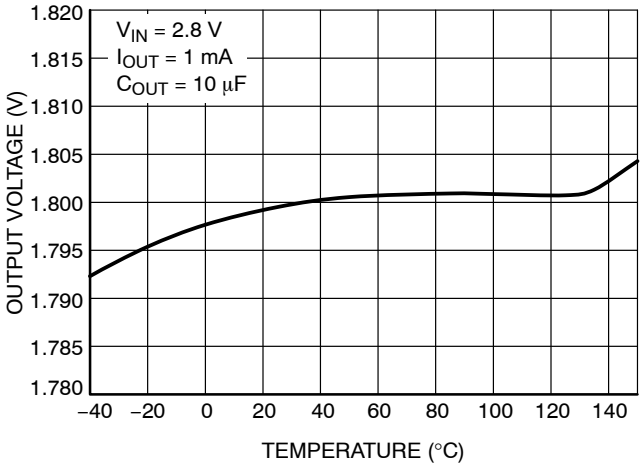

Figure 4. Output Voltage vs. Temperature – V_{OUT} = 1.8 V

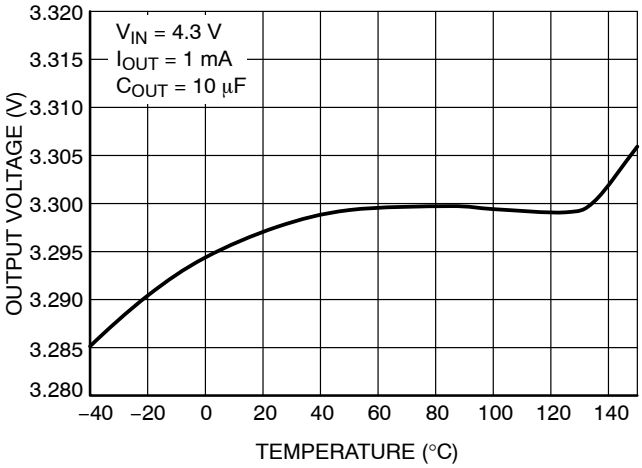

Figure 5. Output Voltage vs. Temperature – V_{OUT} = 3.3 V

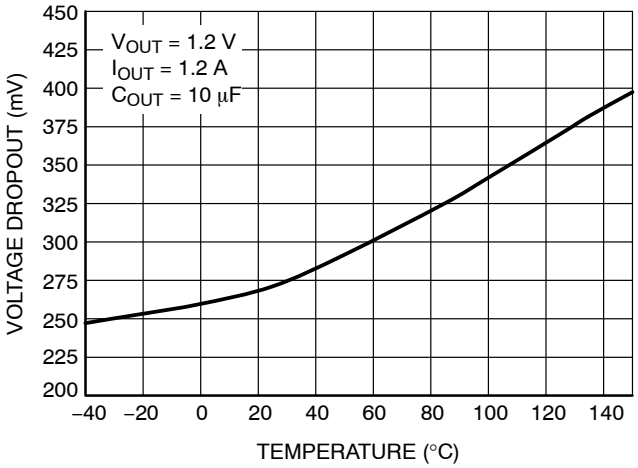

Figure 6. Dropout Voltage vs. Temperature – V_{OUT} = 1.2 V

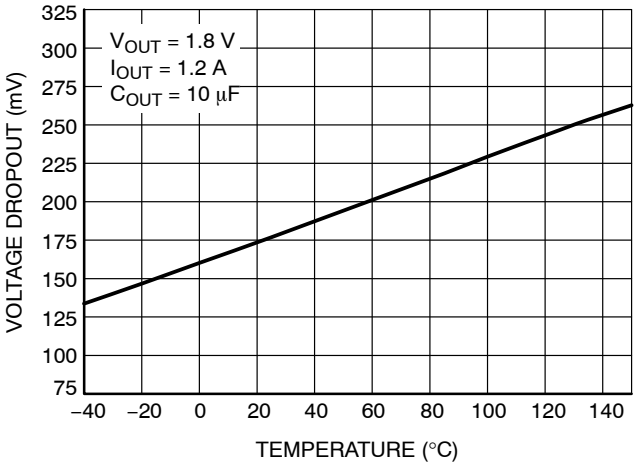

Figure 7. Dropout Voltage vs. Temperature – V_{OUT} = 1.8 V

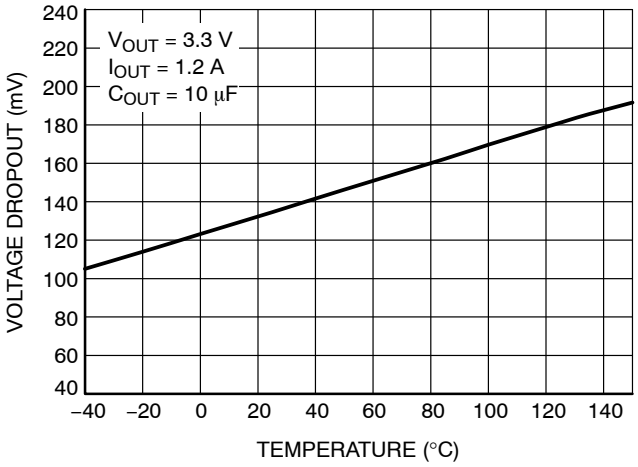

Figure 8. Dropout Voltage vs. Temperature – V_{OUT} = 3.3 V

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TYPICAL CHARACTERISTICS

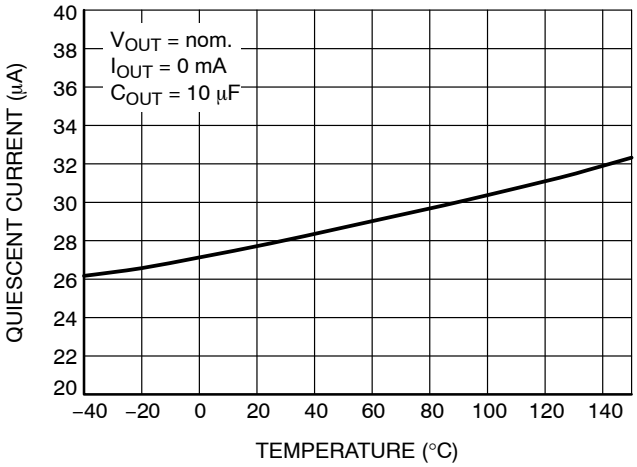

Figure 9. Quiescent Current vs. Temperature

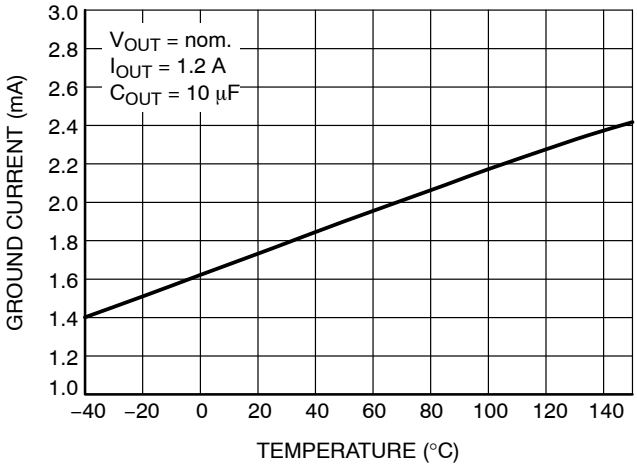

Figure 10. Ground Current vs. Temperature

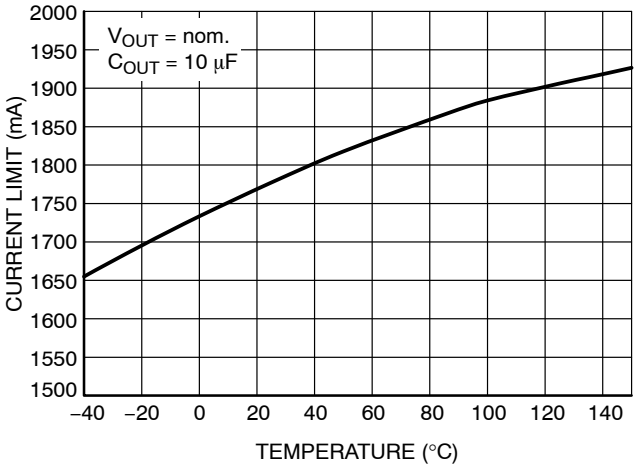

Figure 11. Current Limit vs. Temperature

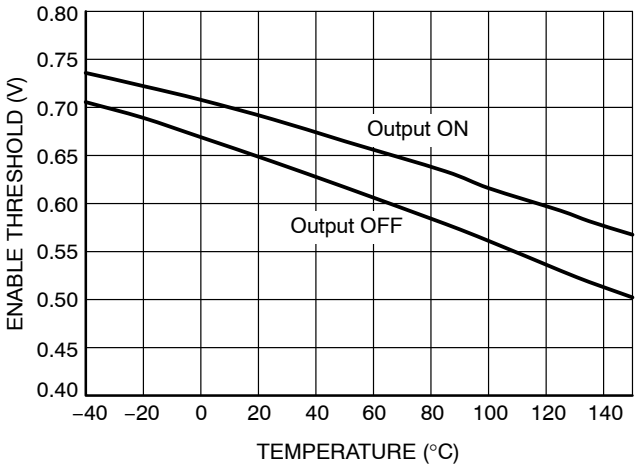

Figure 12. Enable Thresholds vs. Temperature

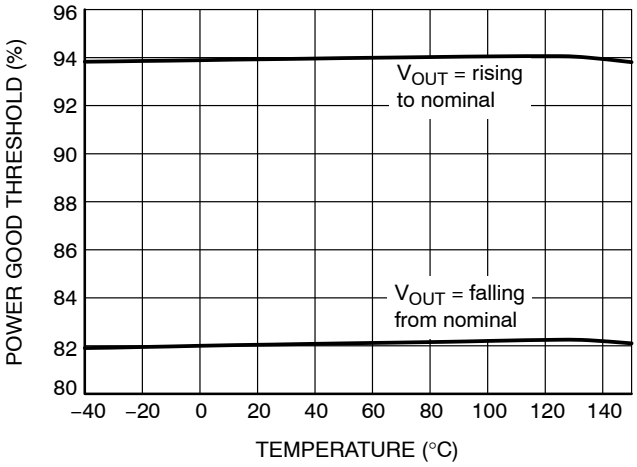

Figure 13. Power Good Thresholds vs. Temperature

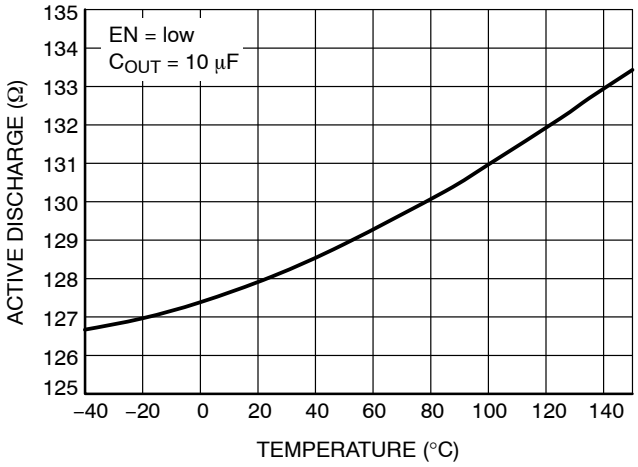

Figure 14. Active Discharge Resistance vs. Temperature

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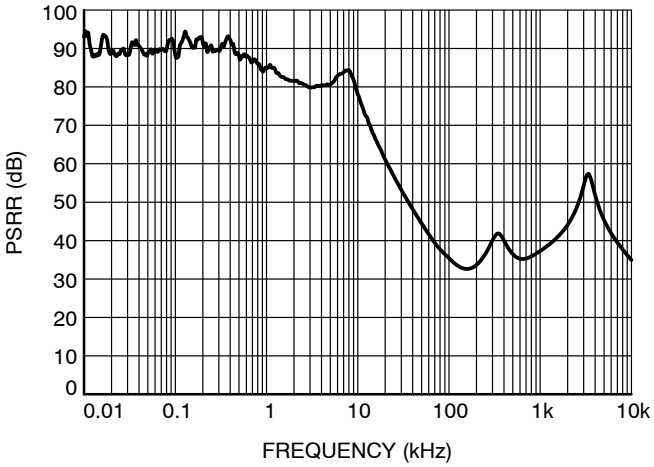

Figure 15. Power Supply Rejection Ratio for V_{OUT} = 1.8 V, I_{OUT} = 10 mA, C_{OUT} = 10 μF

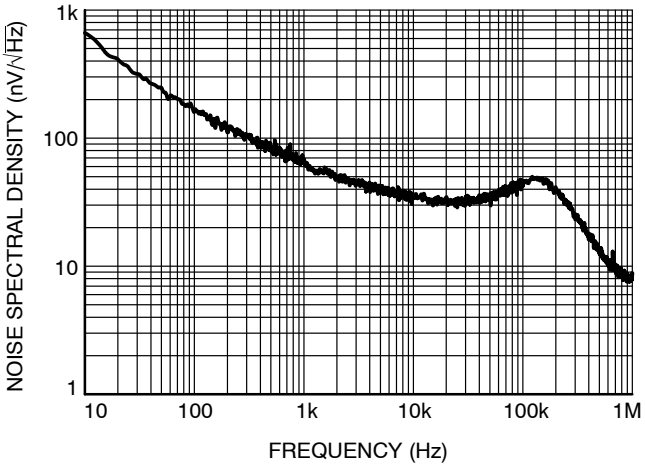

Figure 16. Output Voltage Noise Spectral Density for V_{OUT} = 1.8 V, I_{OUT} = 10 mA, C_{OUT} = 10 μF

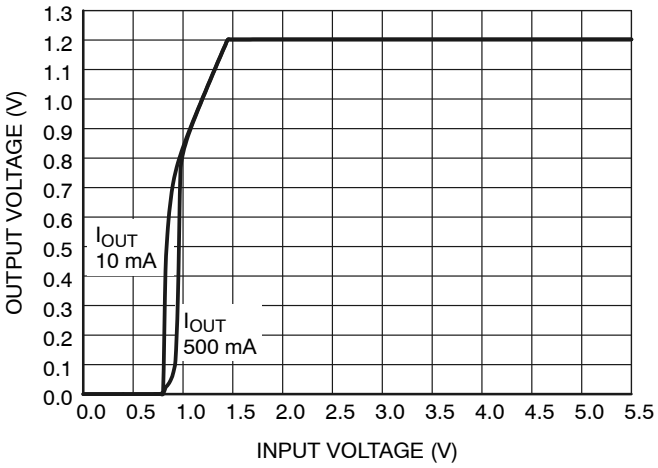

Figure 17. Output Voltage vs. Input Voltage, V_{OUT} = 1.2 V

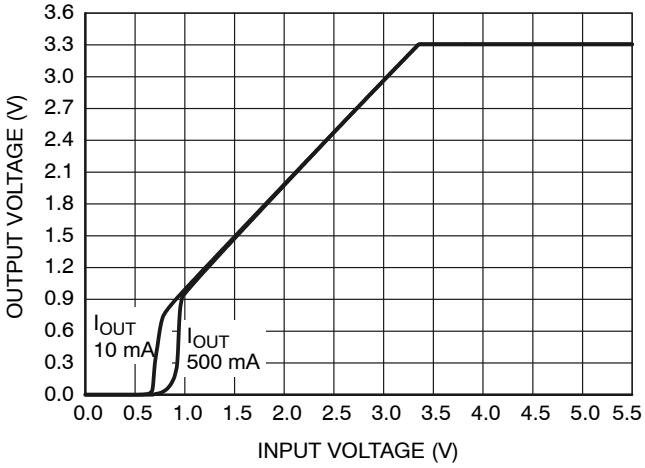

Figure 18. Output Voltage vs. Input Voltage, V_{OUT} = 3.3 V

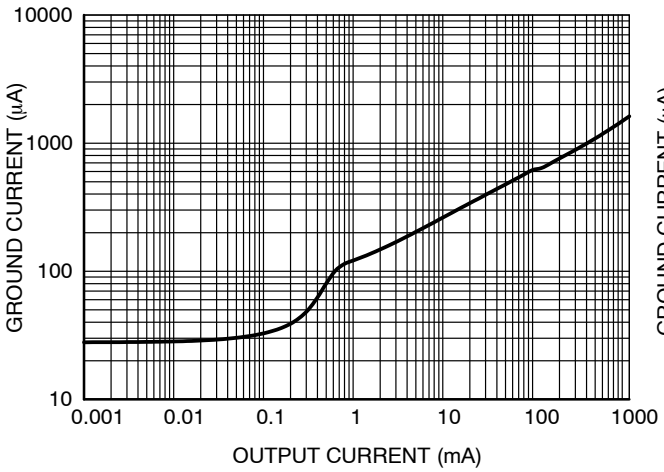

Figure 19. Ground Current vs. Output Current, V_{OUT} = 1.2 V

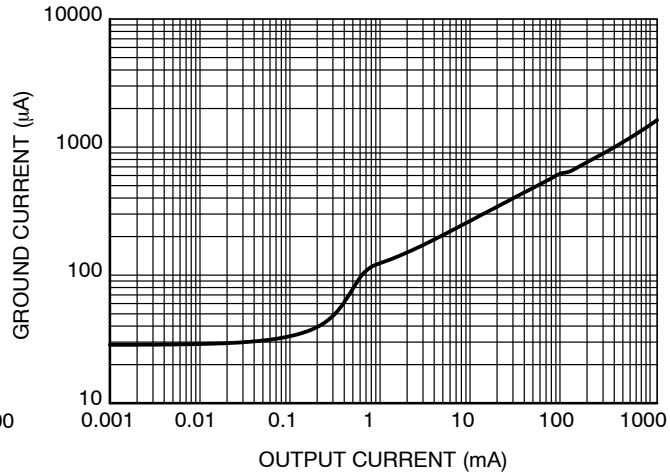

Figure 20. Ground Current vs. Output Current, V_{OUT} = 3.3 V

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TYPICAL CHARACTERISTICS

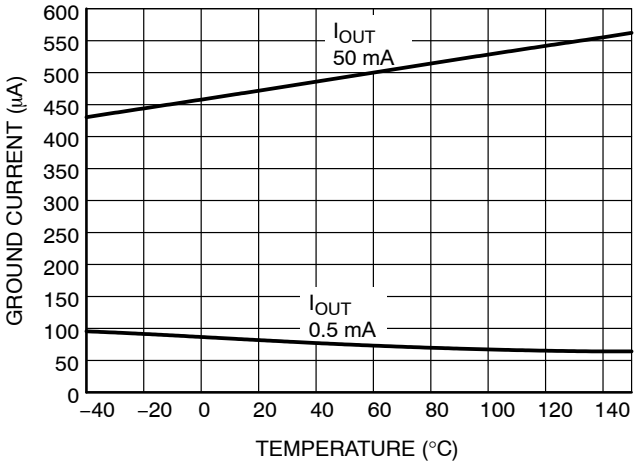

Figure 21. Ground Current vs. Temperature

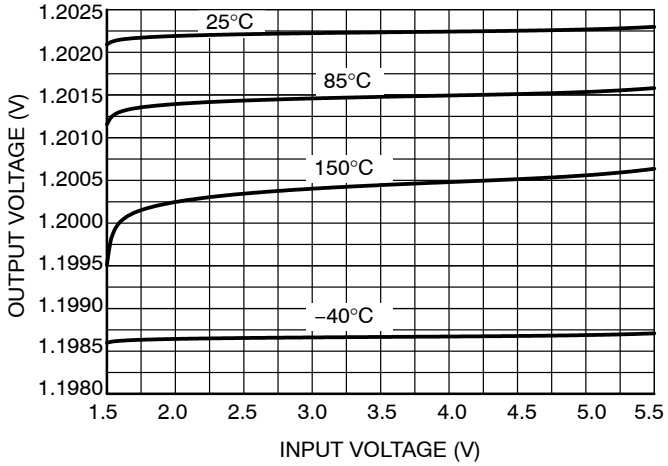

Figure 22. Line Regulation, V_{OUT} = 1.2 V

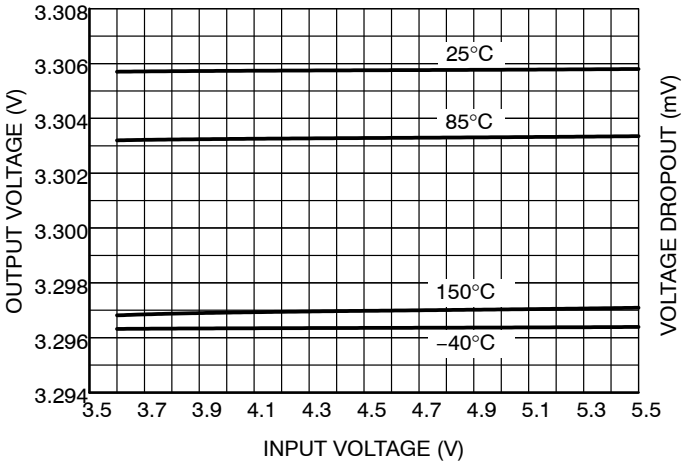

Figure 23. Line Regulation, V_{OUT} = 3.3 V

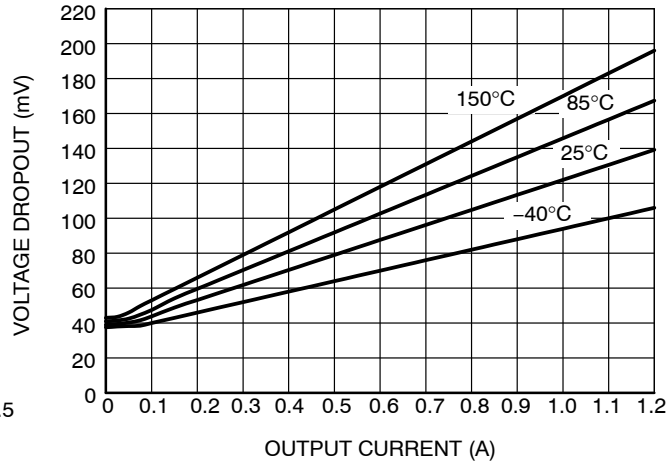

Figure 24. Dropout Voltage vs. Output Current, V_{OUT} = 3.3 V

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APPLICATIONS INFORMATION

The NCV8187 is the member of new family of high output current and low dropout regulators which delivers low quiescent and ground current consumption, good noise and power supply ripple rejection ratio performance. The NCV8187 incorporates EN pin and power good output for simple controlling by MCU or logic. Standard features include current limiting, soft−start feature and thermal protection.

Input Decoupling (C_{IN})

It is recommended to connect at least 1 μF ceramic X5R or X7R capacitor between IN and GND pin of the device. This capacitor will provide a low impedance path for any unwanted AC signals or noise superimposed onto constant input voltage. The good input capacitor will limit the influence of input trace inductances and source resistance during sudden load current changes. Higher capacitance and lower ESR capacitors will improve the overall line transient response.

Output Decoupling (C_{OUT})

The NCV8187 does not require a minimum Equivalent Series Resistance (ESR) for the output capacitor. The device is designed to be stable with standard ceramics capacitors with values of 4.7 μF or greater. Recommended capacitor for the best performance is 10 μF. The X5R and X7R types have the lowest capacitance variations over temperature thus they are recommended.

Power Good Output Connection

The NCV8187 include Power Good functionality for better interfacing to MCU system. Power Good output is open collector type, capable to sink up to 10 mA. Recommended operating current is between 10 μA and 1 mA to obtain low saturation voltage. External pull−up resistor can be connected to any voltage up to 5.5 V (please see Absolute Maximum Ratings table above). Please note that Power Good internal circuitry is non−functional (disabled) to achieve the lowest possible internal current consumption in case of disabled LDO through Enable input (EN = Low). In this case internal Power Good transistor is open and output logic level is defined by voltage used for pull−up resistor. When Power Good is intended to be used as part of power sequencing functionality, then please connect external pull−up resistor to output voltage of NCV8187. This will allow you to get correct low PG signal when LDO is disabled. Active discharge option is recommended to discharge output capacitors connected to LDO.

Power Dissipation and Heat Sinking

The maximum power dissipation supported by the device is dependent upon board design and layout. Mounting pad configuration on the PCB, the board material, and the ambient temperature affect the rate of junction temperature rise for the part. For reliable operation junction temperature should be limited to +125°C. The maximum power dissipation the NCV8187 can handle is given by:

$$P_{D(MAX)} = \frac{\left[T_{J(MAX)} - T_A\right]}{R_{\theta JA}} \quad \text{(eq. 1)}$$

The power dissipated by the NCV8187 for given application conditions can be calculated from the following equations:

$$P_D \approx V_{IN}\left(I_{GND}(I_{OUT})\right) + I_{OUT}\left(V_{IN} - V_{OUT}\right) \quad \text{(eq. 2)}$$

or

$$V_{IN(MAX)} \approx \frac{P_{D(MAX)} + \left(V_{OUT} \times I_{OUT}\right)}{I_{OUT} + I_{GND}} \quad \text{(eq. 3)}$$

Hints

V_{IN} and GND printed circuit board traces should be as wide as possible. When the impedance of these traces is high, there is a chance to pick up noise or cause the regulator to malfunction. Place external components, especially the output capacitor, as close as possible to the NCV8187, and make traces as short as possible.

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ADJUSTABLE VERSION

Not only adjustable version, but also any fixed version can be used to create adjustable voltage, where original fixed voltage becomes reference voltage for resistor divider and feedback loop. Output voltage can be equal or higher than original fixed option, while possible range is from 0.8 V up to 5.2 V. Picture below shows how to add external resistors to increase output voltage above fixed value.

Output voltage is then given by equation:

$$V_{OUT} = V_{FIX} \times (1 + R1/R2)$$

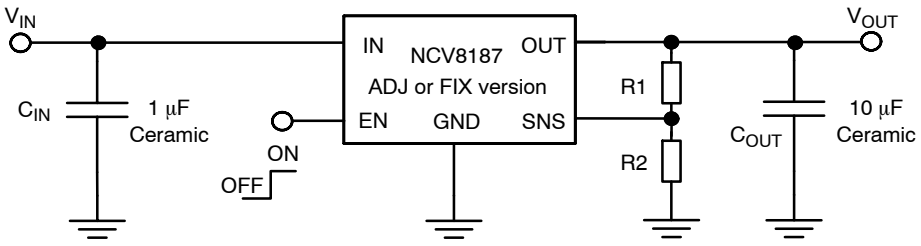

Figure 25.

Please note that output noise is amplified by V_{OUT} / V_{FIX} ratio. For example, if original 0.8 V fixed variant is used to create 3.6 V output voltage, output noise is increased 3.6/0.8 = 4.5 times and real value will be 4.5 × 15 μV_{rms} = 67.5 μV_{rms}. For noise sensitive applications it is recommended to use as high fixed variant as possible – for example in case above it is better to use 3.3 V fixed variant to create 3.6 V output voltage, as output noise will be amplified only 3.6/3.3 = 1.09 × (16.4 μV_{rms}).

where V_{FIX} is voltage of original fixed version (from 0.8 V up to 5.2 V). Do not operate the device at output voltage about 5.2 V, as device can be damaged.

In order to avoid influence of current flowing into SNS pin to output voltage accuracy (SNS current varies with voltage option and temperature, typical value is 300 nA) it is recommended to use values of R1 and R2 below 500 kΩ.

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ORDERING INFORMATION

Device Part No.	Voltage Option	Marking	Option	Package	Shipping†
NCV8187AMT110TAG	1.1 V	PM	With Active Output Discharge	WDFN6 2x2 non WF (Pb−Free)	3,000 / Tape & Reel
NCV8187AMT120TAG	1.2 V	PJ			
NCV8187AMT180TAG	1.8 V	PK			
NCV8187AMT330TAG	3.3 V	PL			
NCV8187AMN120TAG (Note 11)	1.2 V	NA	With Active Output Discharge	DFN6 3x3 non WF (Pb−Free)	3,000 or 5000 / Tape & Reel (Note 11)
NCV8187AMN180TAG (Note 11)	1.8 V	NH			
NCV8187AMTWADJTAG	ADJ	K2	With Active Output Discharge	WDFNW6 2x2 WF SLP (Pb−Free)	3,000 / Tape & Reel
NCV8187AMTW080TAG	0.8 V	KG			
NCV8187AMTW090TAG	0.9 V	KH			
NCV8187AMTW110TAG	1.1 V	KM			
NCV8187AMTW180TAG	1.8 V	KJ			
NCV8187AMTW330TAG	3.3 V	KK			
NCV8187AML120TAG (Note 11)	1.2 V	WD	With Active Output Discharge	DFNW6 3x3 WF SLP (Pb−Free)	3,000 or 5000 / Tape & Reel (Note 11)
NCV8187AML120TBG (Note 11)	1.2 V	WD			
NCV8187AML180TAG (Note 11)	1.8 V	WE			
NCV8187AMLE120TCG	1.2 V	CA	With Active Output Discharge	DFNW8 3x3 WF (Pb−Free)	3,000 / Tape & Reel
NCV8187AMLE180TCG	1.8 V	CC			
NCV8187AMLE280TCG	2.8 V	CE			
NCV8187AMLE330TCG	3.3 V	CD			
NCV8187AMLEADJTCG	ADJ	C2			
NCV8187ADT180RKG*	1.8 V	V8187BG	With Active Output Discharge	DPAK−5 (Pb−Free)	2,500 / Tape & Reel
NCV8187ADT330RKG*	3.3 V	V8187CG			
NCV8187ADTADJRKG*	ADJ	V8187AG			

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.
*Package in development.
11. Products processed after October 1, 2022 are shipped with quantity 5000 units / tape & reel.

REVISION HISTORY

Revision	Description of Changes	Date
10	Added NCV8187AML120TBG OPN to ordering table.	5/11/2026

*Please note that this document has been previously updated prior to the inclusion of this revision history table and that the changes tracked only reflect what has occurred on the noted approval dates.

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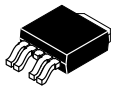
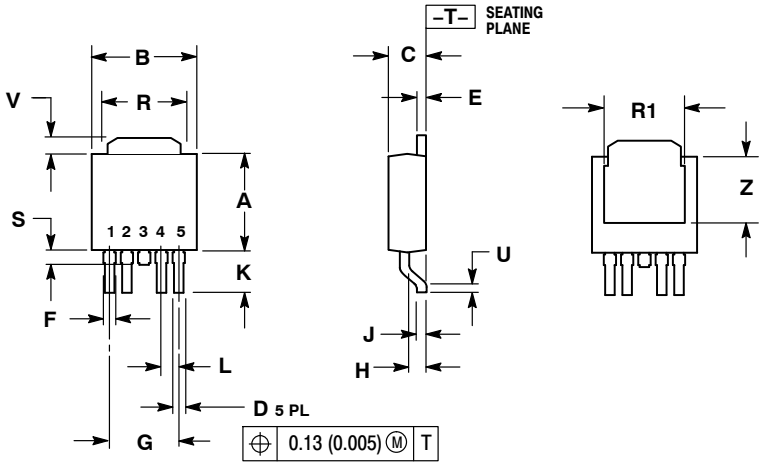


SCALE 1:1

DPAK−5, CENTER LEAD CROP
CASE 175AA
ISSUE B

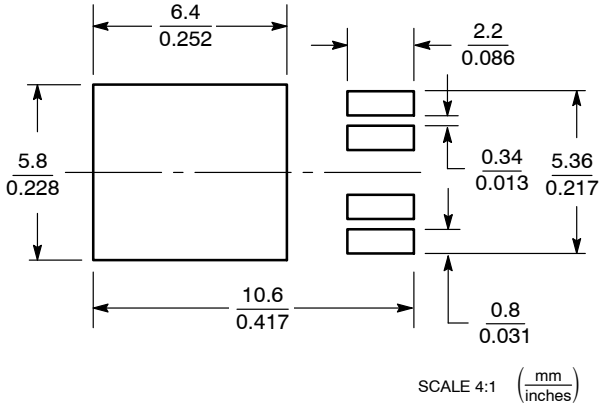
DATE 15 MAY 2014



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.

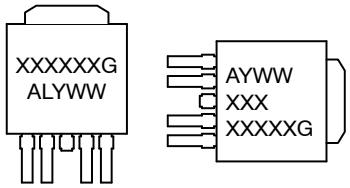
	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	0.235	0.245	5.97	6.22
B	0.250	0.265	6.35	6.73
C	0.086	0.094	2.19	2.38
D	0.020	0.028	0.51	0.71
E	0.018	0.023	0.46	0.58
F	0.024	0.032	0.61	0.81
G	0.180 BSC		4.56 BSC	
H	0.034	0.040	0.87	1.01
J	0.018	0.023	0.46	0.58
K	0.102	0.114	2.60	2.89
L	0.045 BSC		1.14 BSC	
R	0.170	0.190	4.32	4.83
R1	0.185	0.210	4.70	5.33
S	0.025	0.040	0.63	1.01
U	0.020	−−−	0.51	−−−
V	0.035	0.050	0.89	1.27
Z	0.155	0.170	3.93	4.32

RECOMMENDED SOLDERING FOOTPRINT*



*For additional information on our Pb−Free strategy and soldering details, please download the **onsemi** Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

GENERIC MARKING DIAGRAMS*



IC **Discrete**

XXXXXX	= Device Code
A	= Assembly Location
L	= Wafer Lot
Y	= Year
WW	= Work Week
G	= Pb−Free Package

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, “G” or microdot “ ▪”, may or may not be present.

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DESCRIPTION:	**DPAK−5 CENTER LEAD CROP**	**PAGE 1 OF 1**

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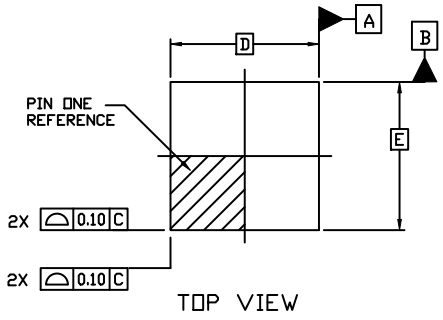
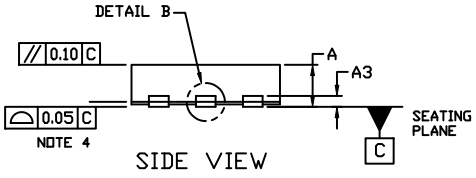
SCALE 2:1

DFNW6 3x3, 0.95P
CASE 506DK
ISSUE A

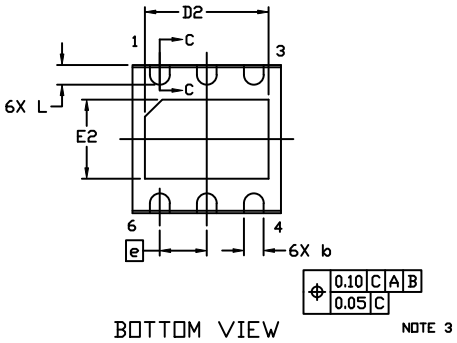
DATE 07 MAY 2021



TOP VIEW



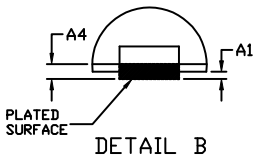
SIDE VIEW



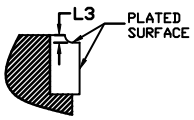
BOTTOM VIEW

NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS
3. DIMENSION b APPLIES TO THE PLATED TERMINALS AND IS MEASURED BETWEEN 0.10 AND 0.20mm FROM THE TERMINAL TIP.
4. PROFILE APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.

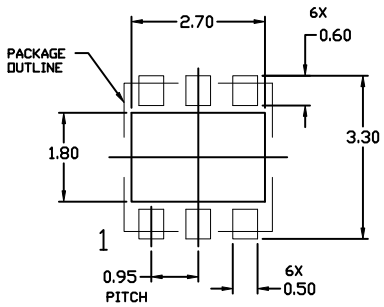


DETAIL B



SECTION C-C

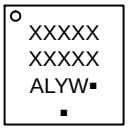
DIM	MILLIMETERS		
	MIN.	MAX.	MAX.
A	0.75	0.85	0.95
A1	0.00	---	0.05
A3	0.20 REF		
A4	0.10	---	---
b	0.35	0.40	0.45
D	3.00 BSC		
D2	2.40	2.50	2.60
E	3.00 BSC		
E2	1.50	1.60	1.70
e	0.95 BSC		
L	0.30	0.40	0.50
L3	0.00	0.05	0.10



RECOMMENDED
MOUNTING FOOTPRINT

* For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

GENERIC
MARKING DIAGRAM*



XXXXX = Specific Device Code
A = Assembly Location
L = Wafer Lot
Y = Year
W = Work Week
▪ = Pb−Free Package

(Note: Microdot may be in either location)

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, “G” or microdot “▪”, may or may not be present. Some products may not follow the Generic Marking.

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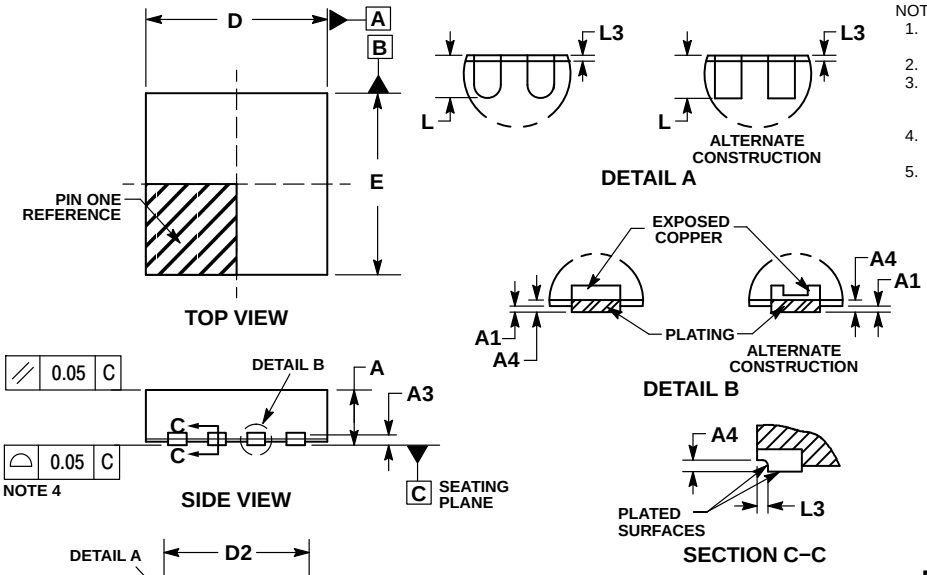
SCALE 2:1

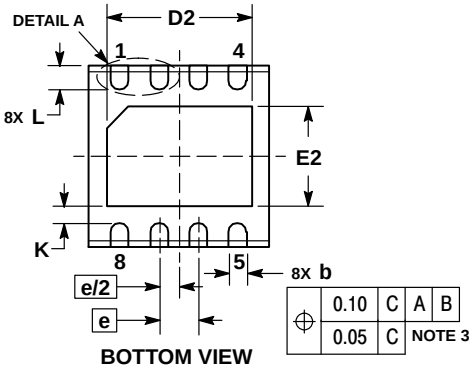
DFNW8 3x3, 0.65P
CASE 507AD
ISSUE A

DATE 15 JUN 2018

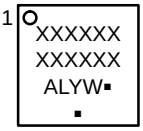


NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSION b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.15 AND 0.30mm FROM THE TERMINAL TIP.
4. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.
5. THIS DEVICE CONTAINS WETTABLE FLANK DESIGN FEATURE TO AID IN FILLET FORMATION ON THE LEADS DURING MOUNTING.

	MILLIMETERS		
DIM	MIN	NOM	MAX
A	0.80	0.90	1.00
A1	−−−	−−−	0.05
A3		0.20 REF	
A4	0.10	−−−	−−−
b	0.25	0.30	0.35
D	2.90	3.00	3.10
D2	2.30	2.40	2.50
E	2.90	3.00	3.10
E2	1.55	1.65	1.75
e		0.65 BSC	
K		0.28 REF	
L	0.30	0.40	0.50
L3		0.05 REF	



GENERIC MARKING DIAGRAM*



XXXXXX = Specific Device Code
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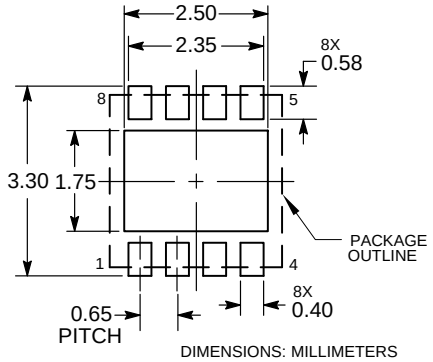
L = Wafer Lot
Y = Year
W = Work Week
▪ = Pb−Free Package

(Note: Microdot may be in either location)

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, “G” or microdot “ ▪”, may or may not be present. Some products may not follow the Generic Marking.

RECOMMENDED SOLDERING FOOTPRINT*



DIMENSIONS: MILLIMETERS

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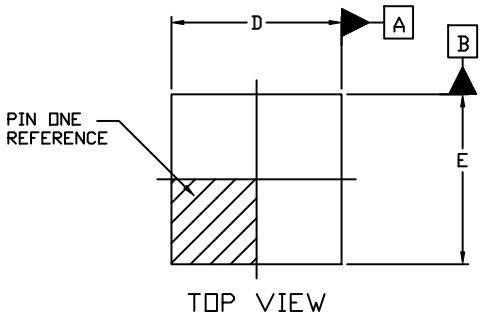
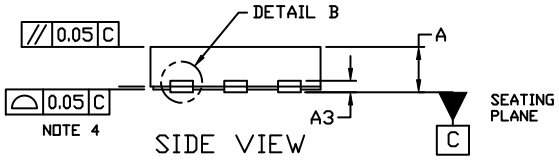
DFNW6 3X3, 0.95P
CASE 507AW
ISSUE O

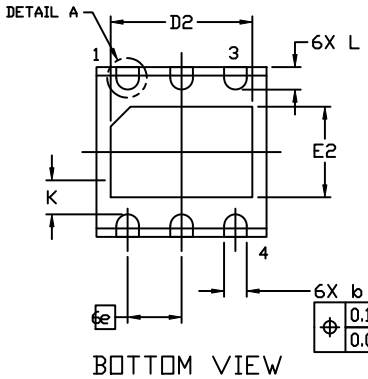
DATE 21 MAY 2019



TOP VIEW



SIDE VIEW

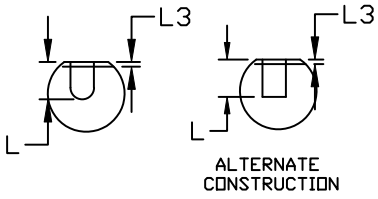


BOTTOM VIEW

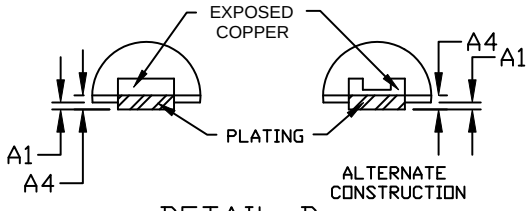
NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS
3. DIMENSION b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.15 AND 0.30 MM FROM THE TERMINAL TIP.
4. COPLANARITY APPLIES TO THE EXPOSED PADS AS WELL AS THE TERMINALS.

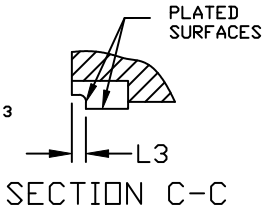
DIM	MILLIMETERS		
	MIN.	NOM.	MAX.
A	0.80	0.90	1.00
A1	0.00	---	0.05
A3		0.20 REF	
A4	0.10	---	---
b	0.35	0.40	0.45
D	2.90	3.00	3.10
D2	2.40	2.50	2.60
E	2.90	3.00	3.10
E2	1.50	1.60	1.70
e		0.95 BSC	
K	0.30	---	---
L	0.30	0.40	0.50
L3	---	---	0.10



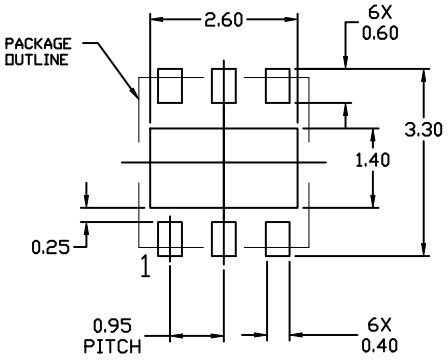
DETAIL A



DETAIL B



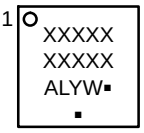
SECTION C-C



RECOMMENDED
MOUNTING FOOTPRINT

* For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

GENERIC
MARKING DIAGRAM*



XXXXX = Specific Device Code
A = Assembly Location
L = Wafer Lot
Y = Year
W = Work Week
▪ = Pb−Free Package

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, “G” or microdot “ ▪”, may or may not be present. Some products may not follow the Generic Marking.

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DESCRIPTION:	**DFNW6 3X3, 0.95P**	**PAGE 1 OF 1**

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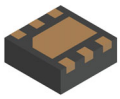
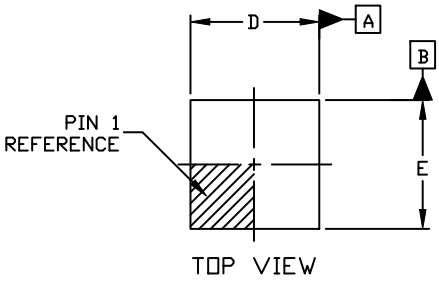
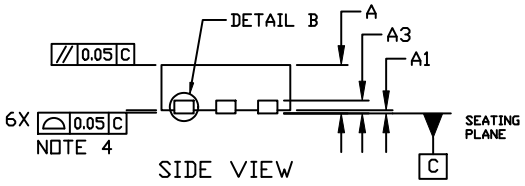
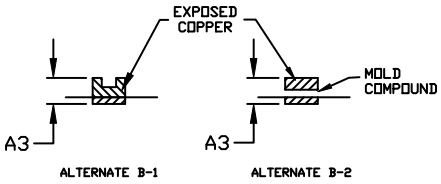


WDFN6 2x2, 0.65P
CASE 511BR
ISSUE C

DATE 01 DEC 2021



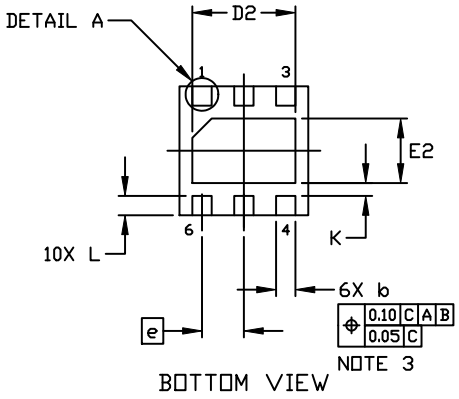


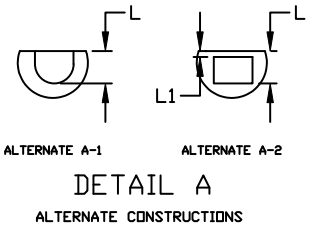


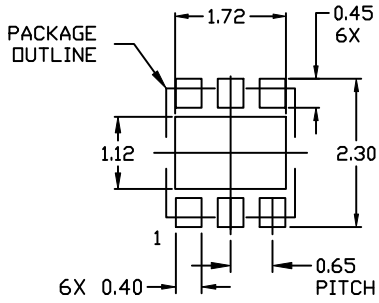
NOTES:

1. DIMENSION AND TOLERANCING PER ASME Y14.5, 2009.
2. CONTROLLING DIMENSION: MILLIMETERS
3. DIMENSION b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.15 AND 0.30 MM FROM THE TERMINAL TIP.
4. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.

DIM	MILLIMETERS		
	MIN.	NOM.	MAX.
A	0.70	0.75	0.80
A1	0.00	---	0.05
A3		0.20 REF	
b	0.25	0.30	0.35
D	1.90	2.00	2.10
D2	1.50	1.60	1.70
E	1.90	2.00	2.10
E2	0.90	1.00	1.10
e		0.65 BSC	
K		0.20 REF	
L	0.20	0.30	0.40
L1	---	---	0.15







For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

GENERIC
MARKING DIAGRAM*



XX = Specific Device Code
M = Date Code

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, “G” or microdot “▪”, may or may not be present. Some products may not follow the Generic Marking.

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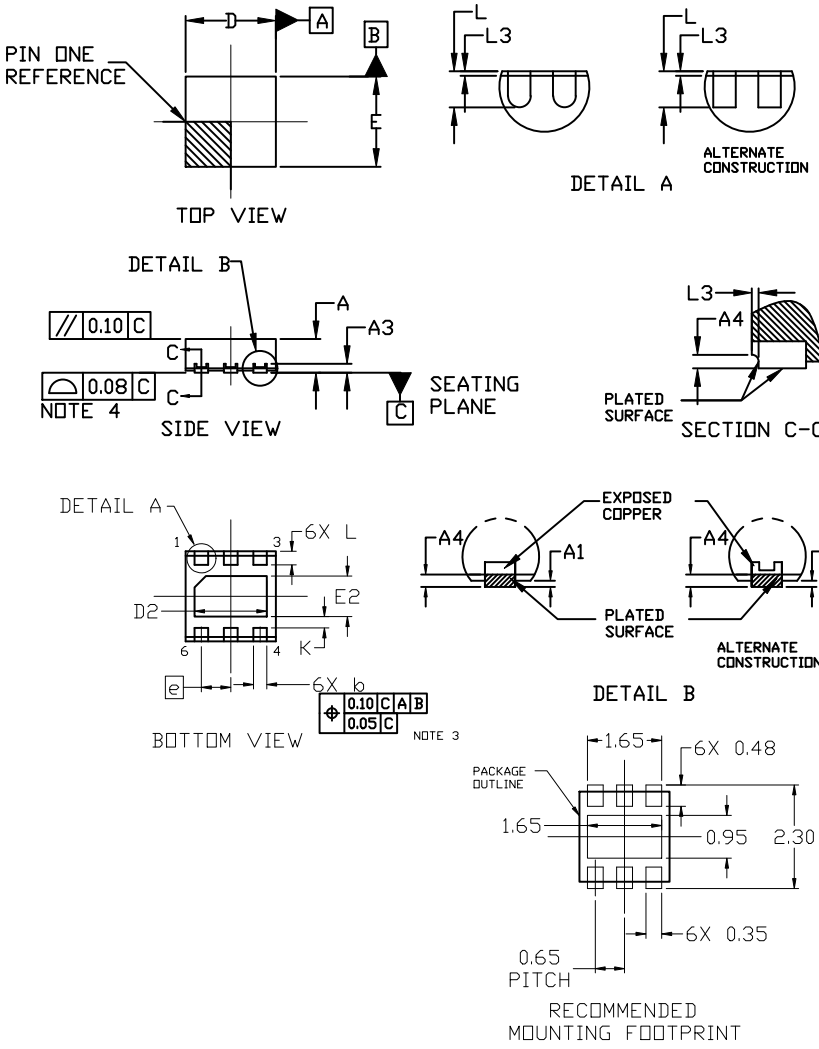
WDFNW6 2x2, 0.65P
CASE 511DW
ISSUE B

DATE 15 JUN 2018



SCALE 4:1

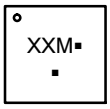


NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS
3. DIMENSION b APPLIES TO PLATED TERMINALS AND IS MEASURED BETWEEN 0.15 AND 0.30MM FROM THE TERMINAL TIP.
4. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.
5. THIS DEVICE CONTAINS WETTABLE FLANK DESIGN FEATURES TO AID IN FILLET FORMATION ON THE LEADS DURING MOUNTING.

DIM	MILLIMETERS		
	MIN.	NOM.	MAX.
A	0.70	0.75	0.80
A1	---	---	0.05
A3	0.20 REF		
A4	0.10	---	---
b	0.25	0.30	0.35
D	1.90	2.00	2.10
D2	1.50	1.60	1.70
E	1.90	2.00	2.10
E2	0.80	0.90	1.00
e	0.65 BSC		
K	0.25 REF		
L	0.25	0.30	0.35
L3	0.05 REF		

GENERIC MARKING DIAGRAM*



M = Month Code
▪ = Pb−Free Package

(Note: Microdot may be in either location)

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, “G” or microdot “ ▪”, may or may not be present. Some products may not follow the Generic Marking.

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