Linear Regulator - Low Dropout, Watchdog, Wake Up, RESET, ENABLE

NCV8518C

The NCV8518C device is a precision micropower voltage regulator. It has a fixed output voltage of 5.0 V and regulates within ±2%. It is suitable for use in all automotive environments and contains all the required functions to control a microprocessor. This device has low dropout voltage and low quiescent current. It includes a watchdog timer, adjustable reset, wake up and enable function. Also encompassed in this device are safety features such as thermal shutdown and short circuit protection. It is capable of handling up to 45 V transients.

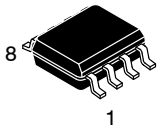
Features

- Output Voltage Option: 5.0 V
- Output Voltage Accuracy: ±2%
- Output Current up to 250 mA
- Low Dropout Voltage
- Low Quiescent Current of 70 μA
- Low Sleep Mode Current less than 1.0 μA
- Micropower Compatible Control Functions:
  - ENABLE
  - Watchdog
  - RESET
  - Wake Up
- Protection Features:
  - Thermal Shutdown
  - Current Limitation
- NCV Prefix for Automotive and Other Applications Requiring Site and Change Control
- AEC−Q100 Grade 1 Qualified and PPAP Capable
- These Devices are Pb−Free and are RoHS Compliant

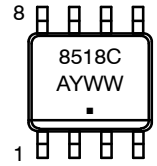
Applications (for safety applications refer to Figure 22)

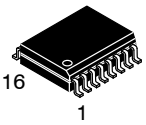
- Body and Chassis
- Instrument and Clusters
- Engine Control Unit

MARKING DIAGRAMS

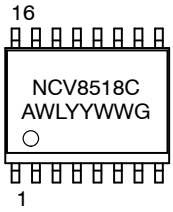


SOIC−8 EP
CASE 751AC





SOIC−16 WB EP
CASE 751AG



A	= Assembly Location
WL	= Wafer Lot
YY, Y	= Year
WW	= Work Week
▪ or G	= Pb−Free Package

ORDERING INFORMATION

Device	Package	Shipping†
NCV8518CPDR2G	SOIC−8 EP (Pb−Free)	2500 / Tape & Reel
NCV8518CPWR2G	SOIC−16 WB EP (Pb−Free)	1000 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

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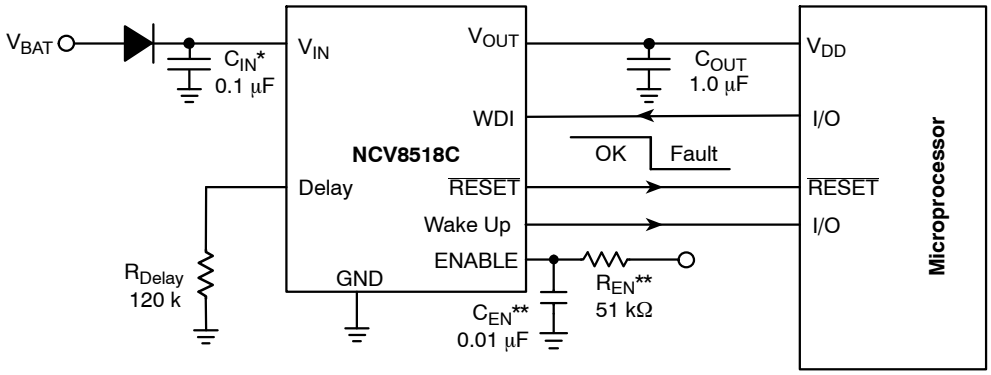
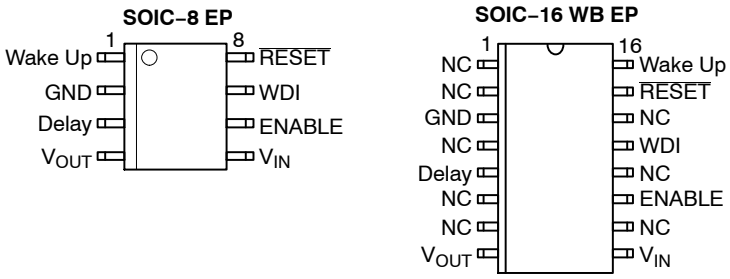


*C_{IN} required if regulator is located far from power supply filter. If extremely fast input voltage transients are expected then appropriate input filter must be used. The filter can be composed of several capacitors in parallel.

**The RC filter is only required when transients with slew rate in excess of 1 V/μs may be present on the ENABLE voltage source during operation. The filter is not required when ENABLE is connected to a noise−free DC voltage.

Figure 1. Application Circuit

PIN CONNECTIONS



PIN FUNCTION DESCRIPTION

Pin No.		Pin Name	Description
SOIC−8 EP	SOIC−16 WB EP		
4	8	V_{OUT}	Regulated Output Voltage.
5	9	V_{IN}	Positive Power Supply. Connect capacitor to ground.
7	13	WDI	CMOS compatible Watchdog Input. The watchdog function monitors the falling edge of the incoming signal.
2	3	GND	Power Supply Ground.
6	11	ENABLE	ENABLE Input. Low level disables the chip. Connect to V_{IN} if this function is not needed.
8	15	$\overline{\text{RESET}}$	CMOS compatible output $\overline{\text{RESET}}$ goes low whenever V_{OUT} drops by more than 7.0% from nominal, or during the absence of a correct watchdog signal.
3	5	Delay	Delay Timing. Buffered reference voltage used to create timing current for $\overline{\text{RESET}}$ and Watchdog threshold frequency from R_{Delay}.
−	1, 2, 4, 6, 7, 10, 12, 14	NC	Not Connected. Not internally bonded.
1	16	Wake Up	Continuously generated signal that interrupts the microprocessor from sleep mode.
EPAD	EPAD	Exposed Pad	Connect to Ground potential or leave unconnected.

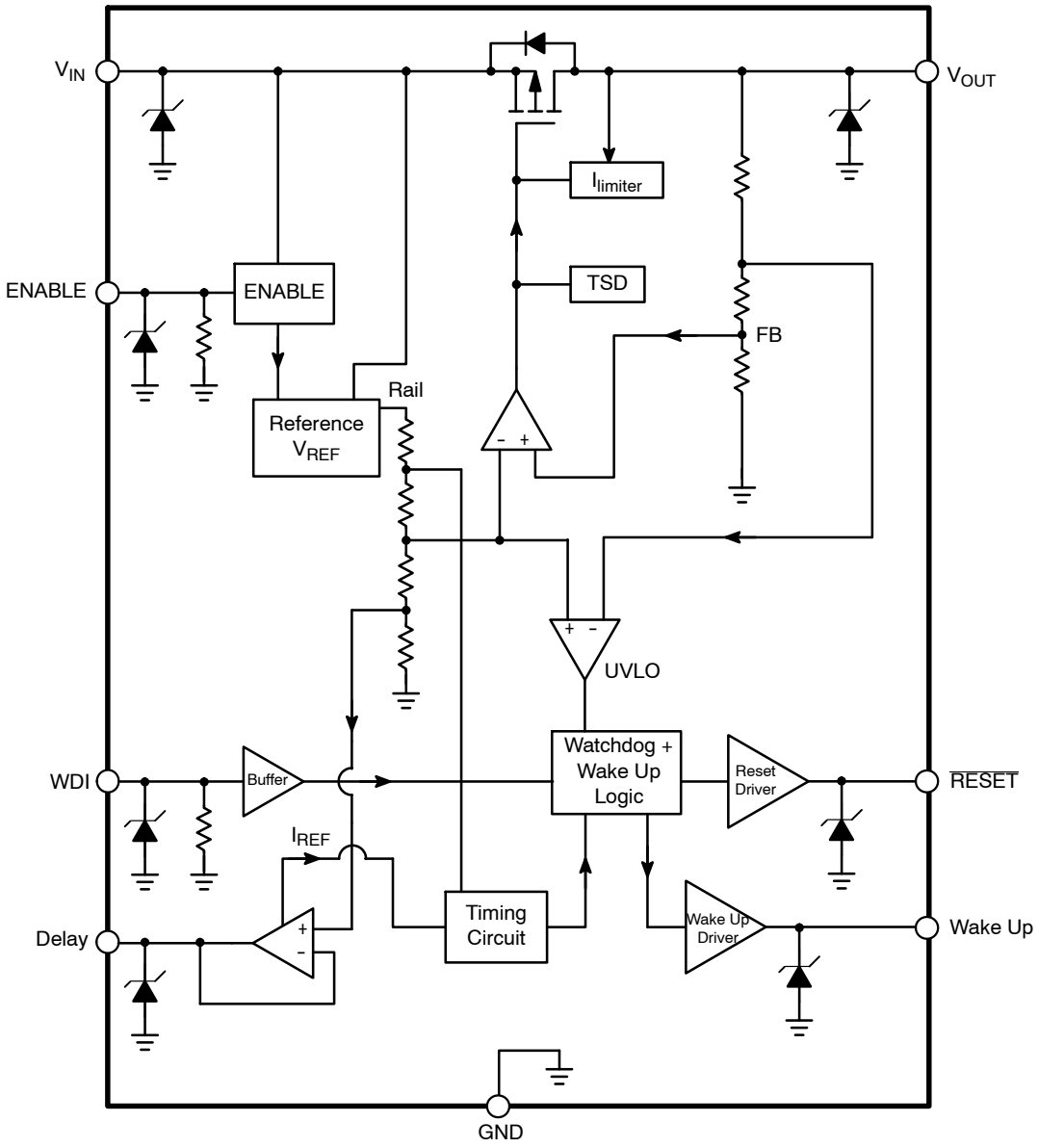


Figure 1. Block Diagram

MAXIMUM RATINGS

Rating	Symbol	Min	Max	Unit
DC Voltage (Note 1) Input Voltage ENABLE Voltage	 V_{IN} V_{ENABLE}	 −0.3	 40	V
Peak Transient Voltage (Load Dump) (Note 2) Input Voltage ENABLE Voltage	 V_{IN} V_{ENABLE}		 45	V
Output Voltage	V_{OUT}	−0.3	+7.0	V
$\overline{\text{RESET}}$ Output Voltage Powered chip or connected external components to chip Pin to Ground only, all other pins left disconnected	V_{RESET}	 −0.3 −0.3	 V_{OUT} +7.0	V
$\overline{\text{RESET}}$ Output Current ($\overline{\text{RESET}}$ may be incidentally shorted either to V_{OUT} or to GND without damage)	I_{RESET}	–	Internally Limited	mA
Wake Up Voltage Powered chip or connected external components to chip Pin to Ground only, all other pins left disconnected	V_{Wake_Up}	 −0.3 −0.3	 V_{OUT} +7.0	V
Watchdog Input Voltage	V_{WDI}	−0.3	+7.0	V
Delay Timing Voltage	V_{Delay}	−0.3	+3.6	V
Operating Junction Temperature	T_J	−40	+150	°C
Storage Temperature Range	T_S	−55	+150	°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. Refer to ELECTRICAL CHARACTERISTICS and APPLICATION INFORMATION for Safe Operating Area.
2. Load Dump Test B (with centralized load dump suppression) according to ISO16750−2 standard. Guaranteed by design. Not tested in production. Passed Class B according to ISO16750−1.

ESD CAPABILITY (Note 3)

Rating	Symbol	Min	Max	Unit
ESD Capability, Human Body Model	ESD_{HBM}	−2	2	kV
ESD Capability, Charged Device Model	ESD_{CDM}	−1	1	kV

3. This device series incorporates ESD protection and is tested by the following methods:
   ESD Human Body Model tested per AEC−Q100−002 (JS−001−2017).
   Field Induced Charge Device Model ESD characterization is not performed on plastic molded packages with body sizes smaller than 2 x 2 mm due to the inability of a small package body to acquire and retain enough charge to meet the minimum CDM discharge current waveform characteristic defined in JEDEC JS−002−2018.

LEAD SOLDERING TEMPERATURE AND MSL (Note 4)

Rating	Symbol	Min	Max	Unit
Moisture Sensitivity Level SOIC−16 WB EP (Case 751AG) SOIC−8 EP (Case 751AC)	MSL	 1 2		–
Lead Temperature Soldering: Reflow Leaded Part 60−150 sec above 183 °C, 30 sec max at peak Lead−Free Part 60−150 sec above 217 °C, 40 sec max at peak	T_{SLD}	 – –	 240 peak 265 peak	 °C °C

4. For more information, please refer to our Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

THERMAL CHARACTERISTICS (Note 6)

Parameter	Board/Mounting Conditions Typical Value		Unit
SOIC−8 EP Package			
	100 sq. mm spreader board	1 sq. inch spreader board	
Junction to case top (Ψ_{JT})	11.5	8.0	°C/W
Junction to lead2 (Ψ_{JL2})	28.5	20.0	°C/W
Junction to board (Ψ_{JB}) (Notes 5)	7.0	7.5	°C/W
Junction to ambient (θ_{JA})	132.3	85.3	°C/W
SOIC−16 WB EP Package			
	100 sq. mm spreader board	1 sq. inch spreader board	
Junction to case top (Ψ_{JT})	17.5	14.5	°C/W
Junction to lead2 (Ψ_{JL2})	34.5	27.5	°C/W
Junction to board (Ψ_{JB}) (Notes 5)	8.0	8.0	°C/W
Junction to ambient (θ_{JA})	97.3	73.8	°C/W

All boards are 0.062″ thick FR4, 3″ square, with varying amounts of copper heat spreader, in still air (free convection) conditions. Numerical values are derived from an axisymmetric finite−element model where active die area, total die area, flag area, pad area, and board area are equated to the actual corresponding areas.

5. “board” is defined as center of exposed pad soldered to board; this is the recommended number to be used for thermal calculations, as it best represents the primary heat flow path and is least sensitive to board and ambient properties.
6. Values based on copper area of 645 mm^2 (or 1 in^2) of 1 oz copper thickness and FR4 PCB substrate. Single layer − according to JEDEC51.3, 4 layers − according to JEDEC51.7.

RECOMMENDED OPERATING RANGES

Rating	Symbol	Min	Max	Unit
Input Voltage	V_{IN}	6.0	28	V
Output Current	I_{OUT}	0.1	150	mA
Junction Temperature	T_J	−40	150	°C
Input Capacitor (Note 7)	C_{IN}	0.1	−	μF
Output Capacitor (Note 7)	C_{OUT}	1.0		μF

Functional operation above the stresses listed in the Recommended Operating Ranges is not implied. Extended exposure to stresses beyond the Recommended Operating Ranges limits may affect device reliability.

7. Including de−ratings.

ELECTRICAL CHARACTERISTICS (6.0 V ≤ V_{IN} ≤ 28 V, V_{ENABLE} = 5 V, 100 μA ≤ I_{OUT} ≤ 150 mA, C_{IN} = 100 nF, C_{OUT} = 1.0 μF ceramic, R_{Delay} = 60 kΩ. Min and Max values are valid for temperature range −40°C ≤ T_J ≤ 150°C unless otherwise noted and are guaranteed by test design or statistical correlation. Typical values are referenced to T_J = 25°C.) (Notes 9 and 10)

Characteristic	Symbol	Min	Typ	Max	Unit
Output					
Output Voltage	V_{OUT}	4.9 −2%	5.00	5.10 +2%	V
Dropout Voltage (V_{IN} − V_{OUT}, I_{OUT} = 150 mA) (Note 8)	V_{DO}	–	356	750	mV
Load Regulation (V_{IN} = 13.5 V, I_{OUT} = 100 μA to 150 mA)	Reg_{load}	−30	–	30	mV
Line Regulation (I_{OUT} = 5.0 mA, V_{IN} = 6.0 V to 28 V)	Reg_{line}	−20	–	20	mV
Current Limit (V_{OUT} = 0.95 x V_{OUT_nom}, V_{in} = 13.5 V)	I_{LIM}	255	510	–	mA
Thermal Shutdown (Guaranteed by Design)	T_{Jmax}	150	175	210	°C
Quiescent Current (V_{IN} = 13.5 V, I_{OUT} = 100 μA, V_{ENABLE} = 2.0 V)	I_q	–	70	85	μA
Disable Current (V_{ENABLE} = 0 V, T_A ≤ +125°C)	I_{DIS}	–	–	1.0	μA
$\overline{\text{RESET}}$					
Threshold Voltage 	–	4.5	4.65	4.75	V
Output Low (R_{RESET} = 10 kΩ to V_{OUT}, V_{OUT} = 1.0 V)	–	–	0.025	0.4	V
Output High (R_{RESET} = 10 kΩ to GND)	–	4.5	4.86	–	V
Power On Reset Delay Time (V_{IN} = 13.5 V, R_{Delay} = 60 kΩ, I_{OUT} = 5.0 mA) (V_{IN} = 13.5 V, R_{Delay} = 120 kΩ, I_{OUT} = 5.0 mA) (V_{IN} = 13.5 V, R_{Delay} = 500 kΩ, I_{OUT} = 5.0 mA)	POR	 2.0 – –	 3.1 6.2 26	 4.0 – –	ms
Reset Reaction Time	t_{RR}	–	20	–	μs
Watchdog Input					
Threshold Voltage	WDI_{high}	30	50	70	% of V_{OUT}
Hysteresis (Guaranteed by design) 	WDI_{hys}	25	100	–	mV
Input Current (WDI = 6.0 V)	–	–	1.1	2.0	μA
ENABLE					
Threshold Voltage Logic Low (V_{OUT} ≤ 0.1 V) Logic High (V_{OUT} ≥ 4.5 V)	$V_{th(ENABLE)}$	 – 2.0	 – –	 0.8 –	V
Input Current (V_{ENABLE} = 2.0 V)	I_{ENABLE}	–	2.4	10	μA

8. Measured when the output voltage has dropped 100 mV from the nominal value obtained at nominal input voltage.
9. Refer to ABSOLUTE MAXIMUM RATINGS and OPERATION DESCRIPTION for Safe Operating Area.
10. Performance guaranteed over the indicated operating temperature range by design and/or characterization tested at $T_A \approx T_J$. Low duty cycle pulse techniques are used during testing to maintain the junction temperature as close to ambient as possible.

ELECTRICAL CHARACTERISTICS (continued) (6.0 V ≤ V_{IN} ≤ 28 V, V_{ENABLE} = 5 V, 100 μA ≤ I_{OUT} ≤ 150 mA, C_{IN} = 100 nF, C_{OUT} = 1.0 μF ceramic, R_{Delay} = 60 kΩ. Min and Max values are valid for temperature range −40°C ≤ T_J ≤ 150°C unless otherwise noted and are guaranteed by test design or statistical correlation. Typical values are referenced to T_J = 25°C.)

Characteristic	Symbol	Min	Typ	Max	Unit
Wake Up Output (V_{IN} = 13.5 V, I_{OUT} = 5.0 mA)					
Wake Up Period (R_{Delay} = 60 kΩ) (R_{Delay} = 120 kΩ) (R_{Delay} = 500 kΩ)	–	 18 – –	 24 47 194	 32 – –	ms
Wake Up Duty Cycle Nominal	–	45	50	55	%
$\overline{\text{RESET}}$ HIGH to Wake Up Rising Delay Time (R_{Delay} = 60 kΩ) (R_{Delay} = 120 kΩ) (R_{Delay} = 500 kΩ) 50% $\overline{\text{RESET}}$ Rising Edge to 50% Wake Up Edge	–	 9.0 – –	 12 23.5 97	 16 – –	ms
Wake Up Response to Watchdog Input 50% WDI Falling Edge to 50% Wake Up Falling Edge	–	–	0.65	2.0	μs
Wake Up Response to $\overline{\text{RESET}}$ 50% $\overline{\text{RESET}}$ Falling Edge to 50% Wake Up Falling Edge (V_{OUT} = 5.0 V→ 4.5 V)	–	–	0.012	1.0	μs
Output Low (R_{WakeUp} = 10 kΩ to V_{OUT})	–	–	0.085	0.4	V
Output High (R_{WakeUp} = 10 kΩ to GND)	–	4.5	4.86	–	V
Delay					
Output Voltage (R_{Delay} = 60 kΩ, 120 k, 500 kΩ)	–	–	0.48	–	V

DEFINITION OF TERMS

Dropout Voltage: The input−to−output voltage differential at which the circuit ceases to regulate against further reduction in input voltage. Measured when the output voltage has dropped 100 mV from the nominal value obtained at nominal input voltage, dropout voltage is dependent upon load current and junction temperature.

Input Voltage: The DC voltage applied to the input terminals with respect to ground.

Line Regulation: The change in output voltage for a change in the input voltage. The measurement is made under conditions of low dissipation or by using pulse techniques such that the average chip temperature is not significantly affected.

Load Regulation: The change in output voltage for a change in load current at constant chip temperature.

Quiescent Current: The part of the positive input current that does not contribute to the positive load current. The regulator ground lead current with no load.

Current Limit: Peak current that can be delivered to the output.

TIMING DIAGRAMS

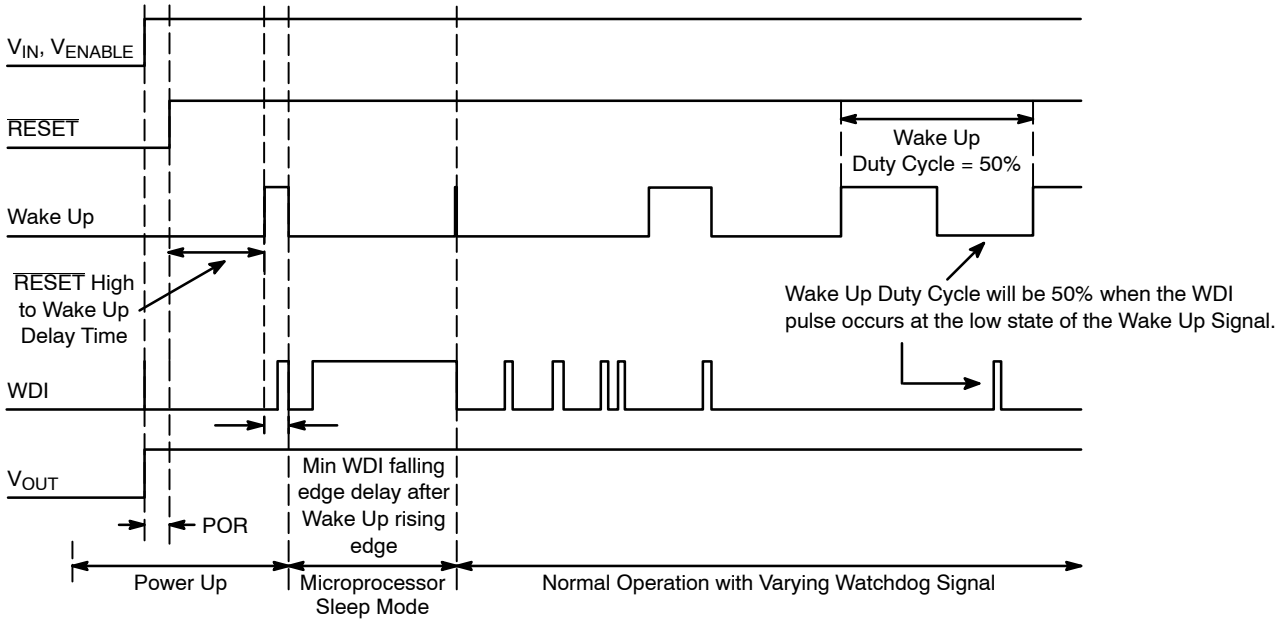


Figure 2. Power Up, Sleep Mode and Normal Operation

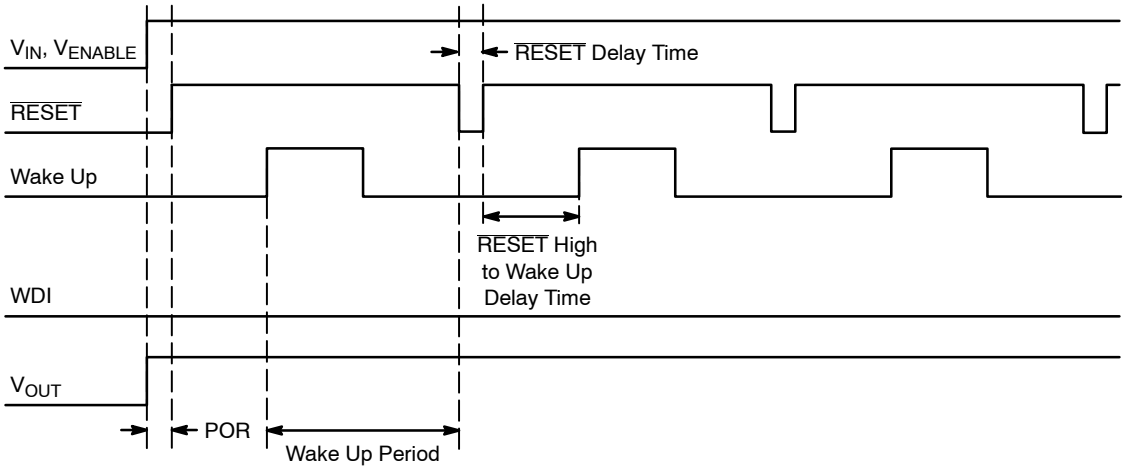


Figure 3. Error Condition: Watchdog Remains Low and a RESET is Issued

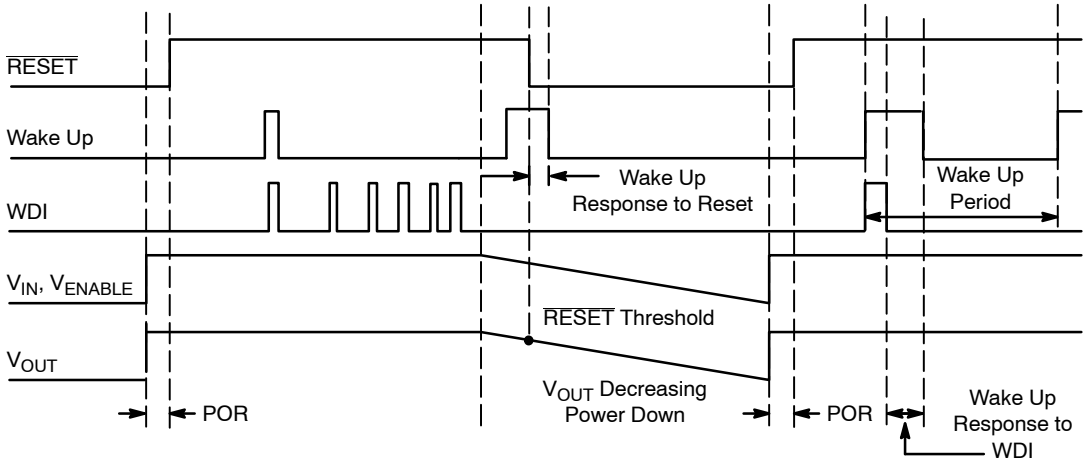


Figure 4. Power Down, Restart Sequence, and Wake Up Response to WDI

TYPICAL CHARACTERISTICS

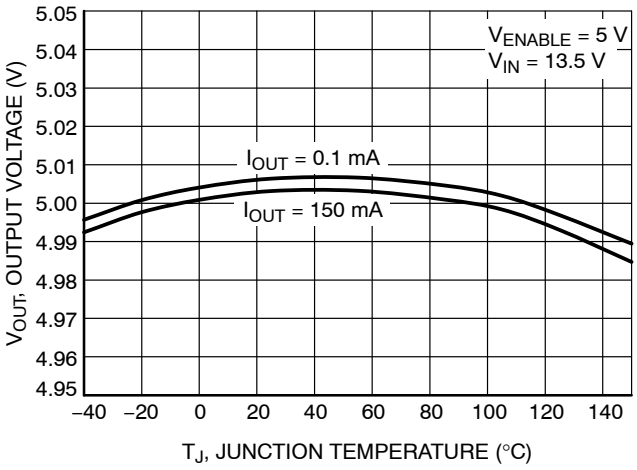


Figure 5. Output Voltage vs. Temperature

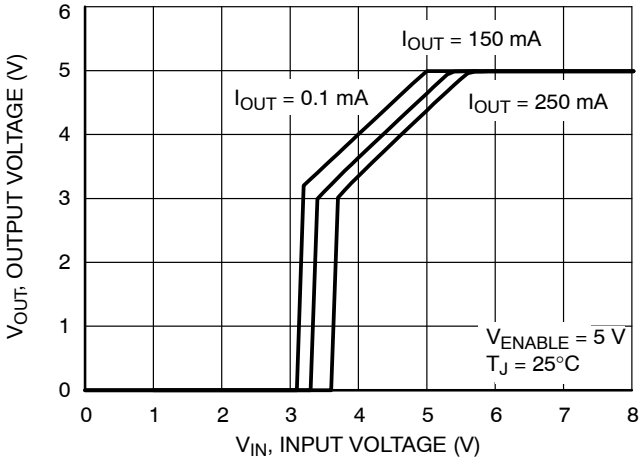


Figure 6. Output Voltage vs. Input Voltage

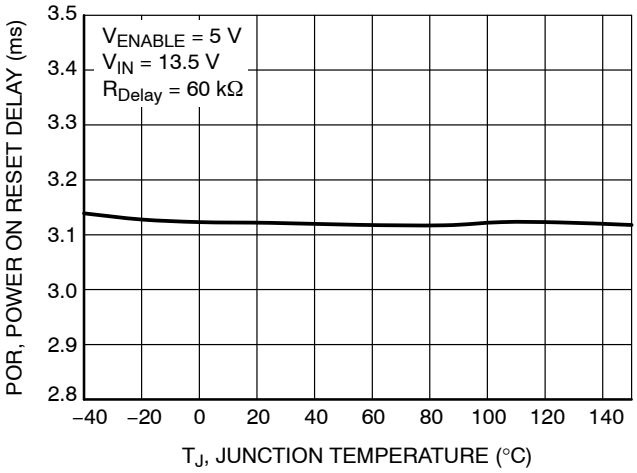


Figure 7. POR, Power On Reset Delay Time vs. Temperature, R_{Delay} = 60 kΩ

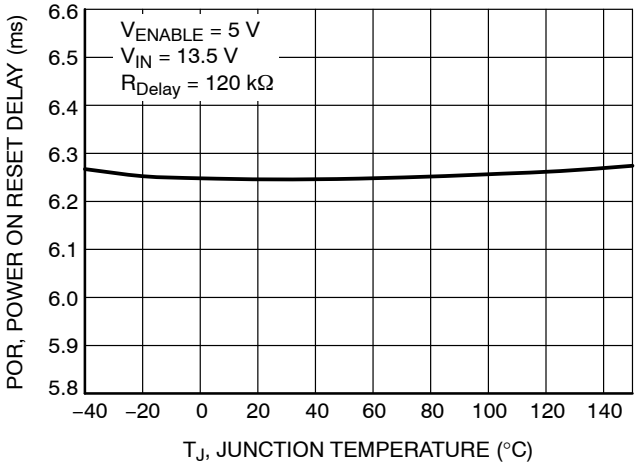


Figure 8. POR, Power On Reset Delay Time vs. Temperature, R_{Delay} = 120 kΩ

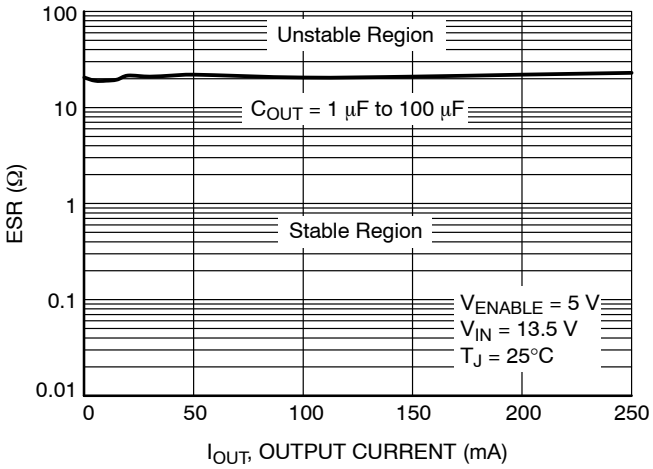


Figure 9. Stability Region of Capacitive ESR vs. Output Current

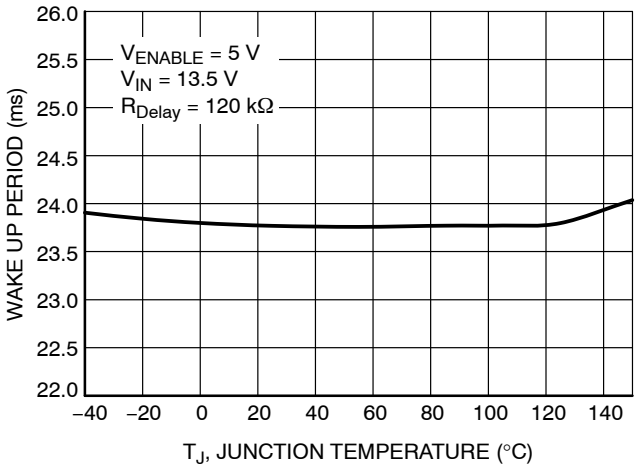


Figure 10. Wake Up Period vs. Temperature, R_{Delay} = 120 kΩ

TYPICAL CHARACTERISTICS

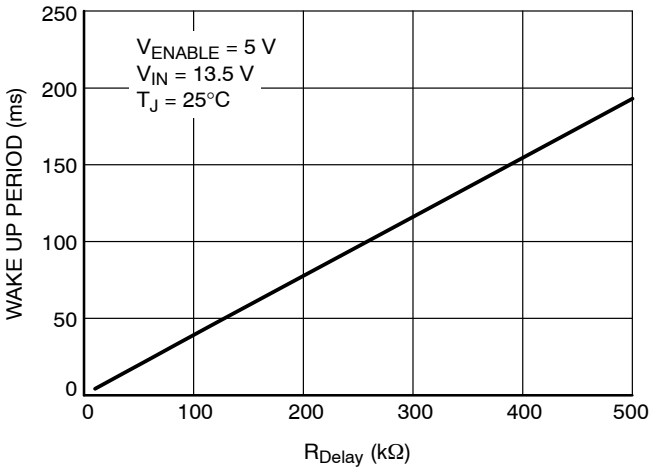


Figure 11. Wake Up Period vs. R_{Delay}

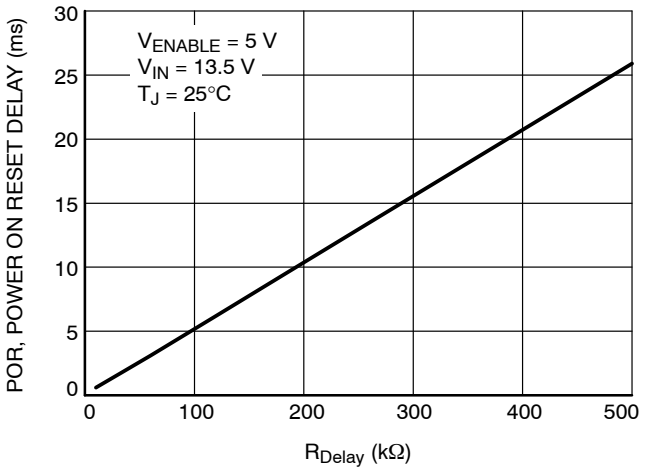


Figure 12. POR, Power On Reset Delay Time vs. R_{Delay}

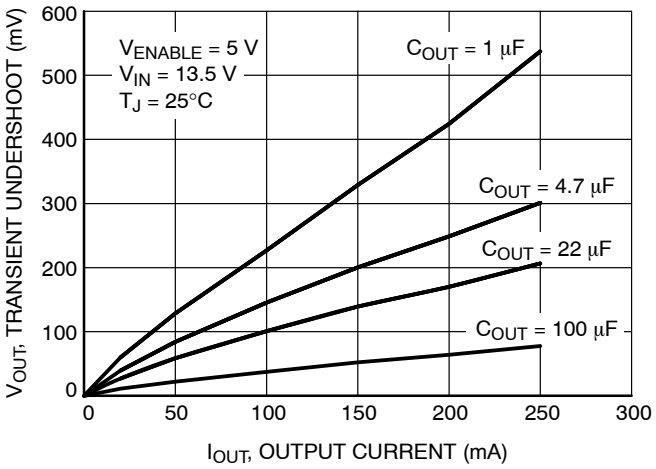


Figure 13. Load Transient Response

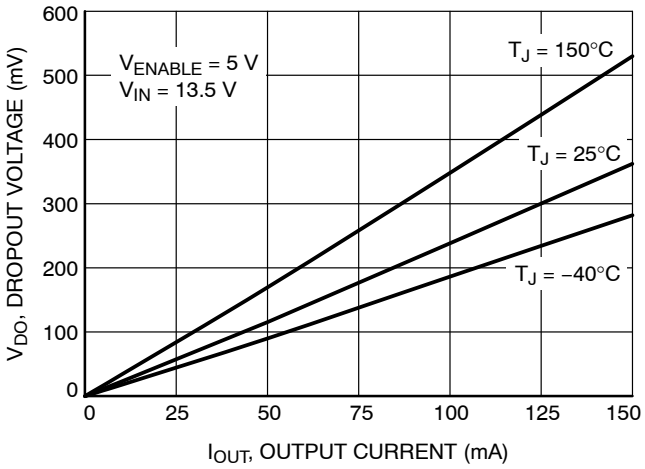


Figure 14. Dropout Voltage vs. Output Current

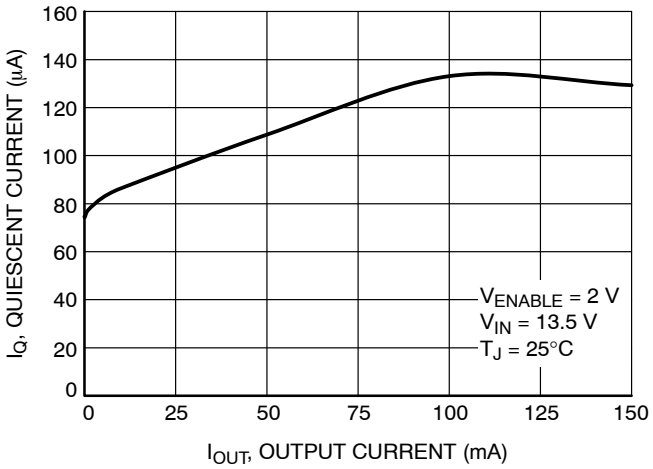


Figure 15. Quiescent Current vs. Output Current

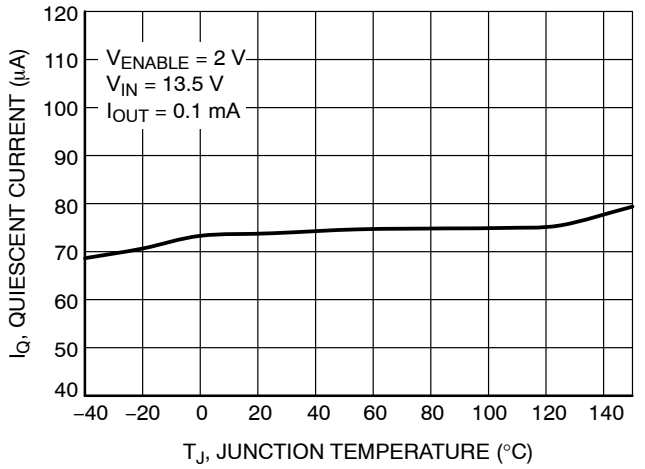


Figure 16. Quiescent Current vs. Junction Temperature

TYPICAL CHARACTERISTICS

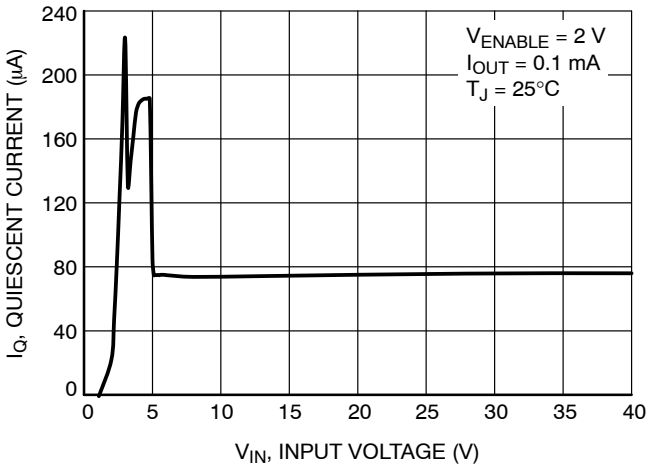


Figure 17. Quiescent Current vs. Input Voltage

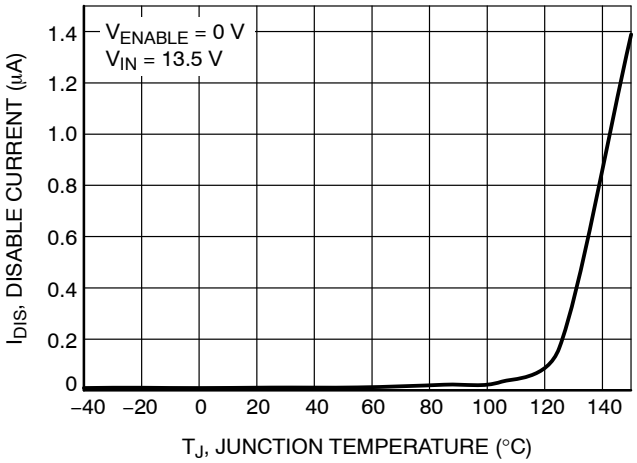


Figure 18. Disable Current vs. Junction Temperature

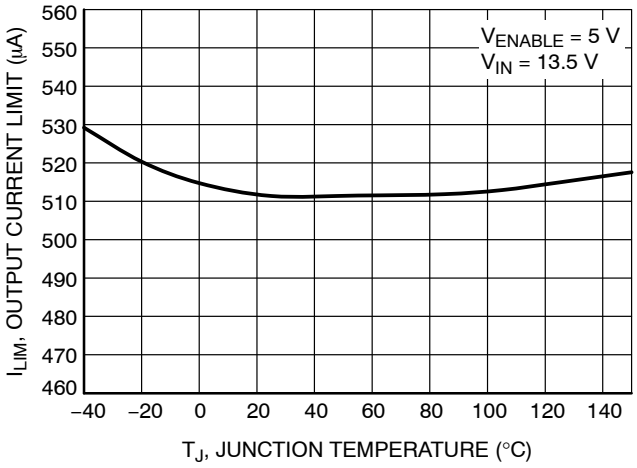


Figure 19. Output Current Limit vs. Junction Temperature

OPERATING DESCRIPTION

General

The NCV8518C is a precision micropower voltage regulator featuring low quiescent current (126 μA typical at 150 mA load) and low dropout voltage (356 mV typical at 150 mA). Integrated microprocessor control functions include Watchdog, Wake Up and $\overline{\text{RESET}}$. An Enable input is provided for logic level control of the regulator state. The combination of low quiescent current and comprehensive microprocessor interface functions make the NCV8518C ideal for use in both battery operated and automotive applications.

The NCV8518C is internally protected against short circuit and thermal runaway conditions. No external components are required to engage these protective mechanisms. The device continues to operate through 45 volt input transients, an important consideration in automotive environments.

Wake Up and Watchdog

To reduce battery drain, a microprocessor or microcontroller can transition to a low current consumption (“sleep”) mode when code execution is suspended or complete. The NCV8518C Wake Up signal is generated and output periodically to interrupt sleep mode. The nominal Wake Up output is a 5 volt square wave (generated from V_{OUT}) with a duty cycle of 50%, at a frequency determined by external timing resistor R_{Delay}. In response to the rising edge of the Wake Up signal, the microprocessor will subsequently output a Watchdog pulse and check its inputs to decide if it should resume normal operation or remain in sleep mode.

The NCV8518C responds to the falling edge of the Watchdog signal, which it expects at least once during each Wake Up period. Minimum WDI pulse width must be higher than 1 μs and WDI falling edge must not occur during 5 μs after Wake Up signal rising edge, otherwise WDI falling edge may not be accepted by watchdog logic. This provides higher robustness of watchdog logic against glitch pulses and disturbances in the application. When the correct Watchdog signal is received, the Wake Up output is forced low. Other Watchdog pulses received within the same cycle are ignored. The Watchdog circuitry continuously monitors the input Watchdog signal (WDI) from the microprocessor. The absence of a falling edge on the Watchdog input during one Wake Up cycle will cause a Reset pulse to be output at the end of the Wake Up cycle (see Figure 4).

$\overline{\text{RESET}}$

As output voltage falls, the $\overline{\text{RESET}}$ output will maintain its current state down to V_{OUT} = 1 V. A Reset signal (active low) is asserted for any of four conditions:

1. During power up, $\overline{\text{RESET}}$ is held low until the output voltage is in regulation.
2. During operation, if the output voltage falls below the Reset Threshold Voltage, $\overline{\text{RESET}}$ switches low, and will remain low until both the output voltage has recovered and the Reset delay timer cycle has completed following that recovery.
3. $\overline{\text{RESET}}$ will switch low if the regulator does not receive a Watchdog input signal within a Wake Up period.
4. Regardless of output voltage, $\overline{\text{RESET}}$ will switch low if the regulator input voltage V_{IN}, falls below a level required to sustain the internal control circuits. The specific voltage is temperature dependent, and is approximately 4.65 V at 20°C.

The Wake Up output is pulled low during a $\overline{\text{RESET}}$ regardless of the cause of the $\overline{\text{RESET}}$. After the $\overline{\text{RESET}}$ returns high, the Wake Up cycle begins again (see Figure 4).

The Reset Delay Time, Wake Up signal frequency and $\overline{\text{RESET}}$ HIGH to Wake Up Rising Delay Time are all set by one external resistor, R_{Delay}, according to the following equations:

$$\text{Wake Up Period (seconds)} = (3.95 \times 10^{-7}) * R_{Delay}\ (\Omega)$$

$$\overline{\text{RESET}}\ \text{Delay Time (seconds)} = (5.2 \times 10^{-8}) * R_{Delay}\ (\Omega)$$

$$\overline{\text{RESET}}\ \text{HIGH to Wake Up Rising Delay Time (seconds)} = (1.96 \times 10^{-7}) * R_{Delay}\ (\Omega)$$

ENABLE

This is a standard TTL and CMOS logic compatible input that can be used to turn the regulator on or off. Logic high enables the regulator; logic low disables it (also called *shutdown*). In the disabled/shutdown state, the pass transistor is off and total quiescent current is less than 1 μA.

Thermal Considerations

As power in the NCV8518C increases, it might become necessary to provide some thermal relief. The maximum power dissipation supported by the device is dependent upon board design and layout. Mounting pad configuration on the PCB, the board material and the ambient temperature affect the rate of junction temperature rise for the part. When the NCV8518C has good thermal conductivity through the PCB, the junction temperature will be relatively low with high power applications. The maximum dissipation the NCV8518C can handle is given by:

$$P_{D(MAX)} = \frac{\left(T_{J(MAX)} - T_A\right)}{\theta_{JA}}$$

Since T_J is not recommended to exceed 150°C, then the NCV8518C (SOIC−8 EP) soldered on 645 mm^2, 1 oz copper area, FR4 can dissipate up to 1.465 W when the ambient temperature (T_A) is 25°C. See Figure 20 and 21 for θ_{JA} versus PCB Cu area. The power dissipated by the NCV8518C can be calculated from the following equations:

$$P_D \approx V_{in}\left(I_q @ I_{out}\right) + I_{out}\left(V_{in} - V_{out}\right)$$

or

$$V_{in(MAX)} \approx \frac{P_{D(MAX)} + \left(V_{out} \times I_{out}\right)}{I_{out} + I_q}$$

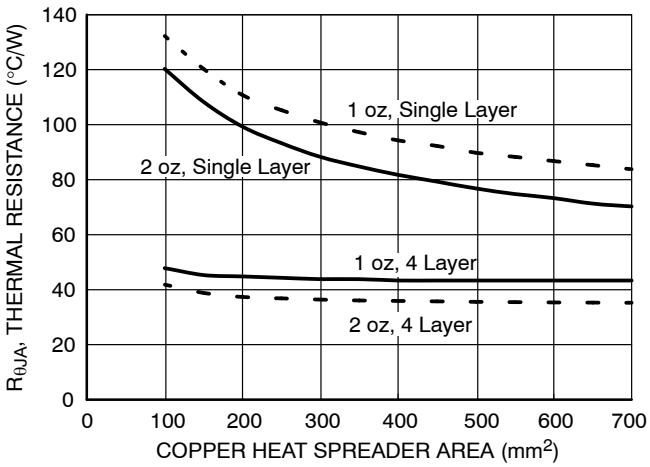


Figure 20. Thermal Resistance vs. PCB Copper Area (SOIC−8 EP)

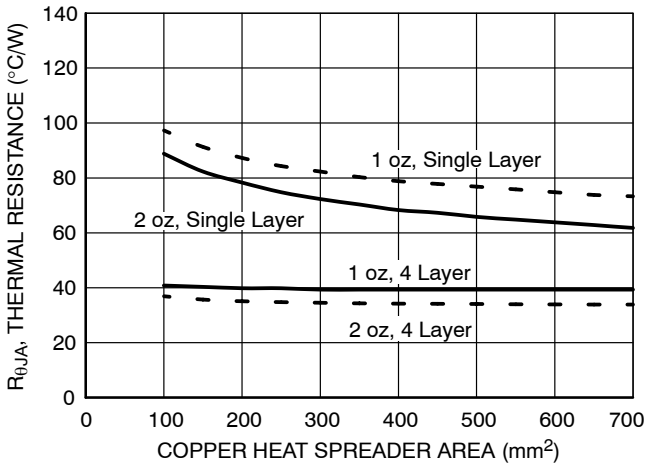


Figure 21. Thermal Resistance vs. PCB Copper Area (SOIC−16 WB EP)

Hints

V_{IN} and GND printed circuit board traces should be as wide as possible. When the impedance of these traces is high, there is a chance to pick up noise or cause the regulator to malfunction. Place external components, especially the output capacitor, as close as possible to the NCV8518C and make traces as short as possible.

The NCV8518C is not developed in compliance with ISO26262 standard. If application is safety critical then the below application example diagram shown in Figure 22 can be used.

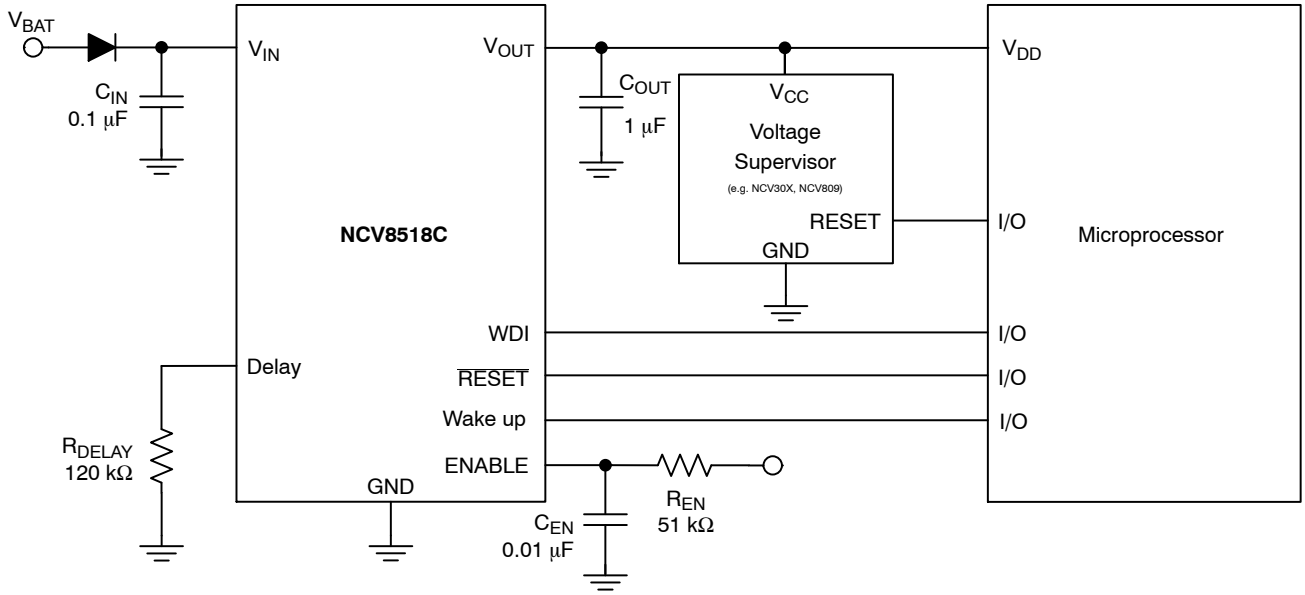


Figure 22. Application Diagram



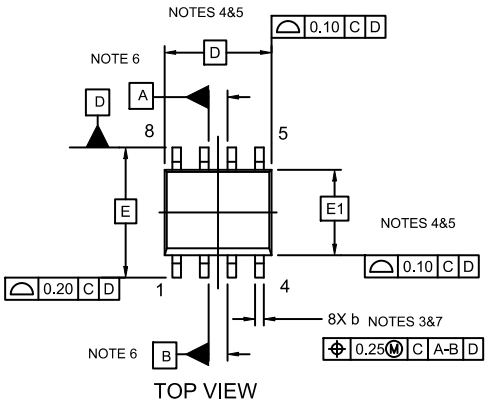
SCALE 1:1

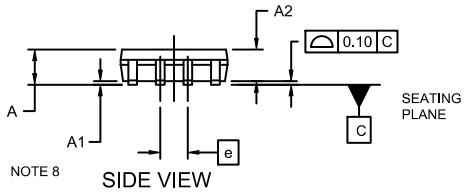
SOIC−8 EP
CASE 751AC
ISSUE E

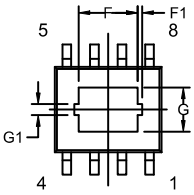
DATE 05 OCT 2022

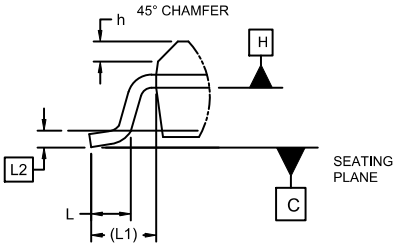
NOTES:

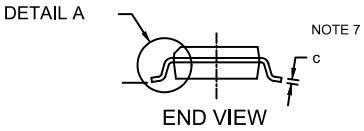
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS
3. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE PROTRUSION SHALL BE 0.004 IN EXCESS OF MAXIMUM MATERIAL CONDITION.
4. DIMENSION D DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR GATE BURRS. MOLD FLASH, PROTRUSIONS, OR GATE BURRS SHALL NOT EXCEED 0.006 PER SIDE. DIMENSION E1 DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.010 mm PER SIDE.
5. THE PACKAGE TOP MAY BE SMALLER THAN THE PACKAGE BOTTOM. DIMENSIONS D AND E1 ARE DETERMINED AT THE OUTERMOST EXTREMES OF THE PLASTIC BODY AT DATUM H.
6. DATUMS A AND B ARE TO BE DETERMINED AT DATUM H.
7. DIMENSIONS b AND c APPLY TO THE FLAT SECTION OF THE LEAD BETWEEN 0.10 TO 0.25 FROM THE LEAD TIP.
8. A1 IS DEFINED AS THE VERTICAL DISTANCE FROM THE SEATING PLANE TO THE LOWEST POINT ON THE PACKAGE BODY.

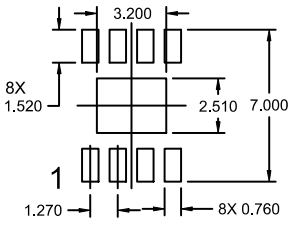








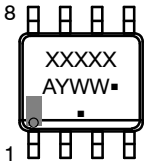




DIM	MILLIMETERS		
	MIN.	NOM..	MAX.
A	1.35	1.55	1.75
A1	---	0.05	0.10
A2	1.35	1.50	1.65
b	0.31	0.41	0.51
c	0.17	0.21	0.23
D	4.90 BSC		
E	6.00 BSC		
E1	3.90 BSC		
e	1.27 BSC		
F	2.24	2.72	3.20
F1		0.20 REF	
G	1.55	2.03	2.51
G1		0.46 REF	
h	0.25	0.38	0.50
L	0.40	0.84	1.27
L1	1.04 REF		
L2	0.25 REF		
Ø	0°	4°	8°

*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D."

GENERIC MARKING DIAGRAM*



XXXXXX = Specific Device Code
A = Assembly Location
Y = Year
WW = Work Week
▪ = Pb−Free Package

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, "G" or microdot " ▪", may or may not be present and may be in either location. Some products may not follow the Generic Marking.

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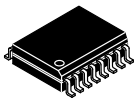
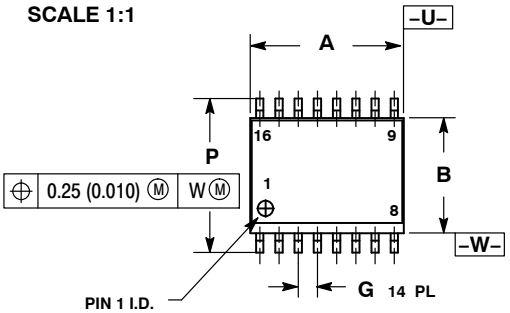
SOIC 16 LEAD WIDE BODY, EXPOSED PAD

CASE 751AG
ISSUE B

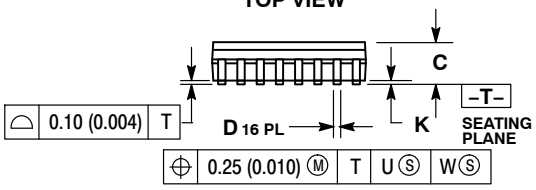
DATE 31 MAY 2016



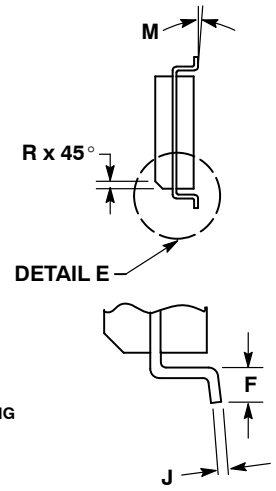
SCALE 1:1



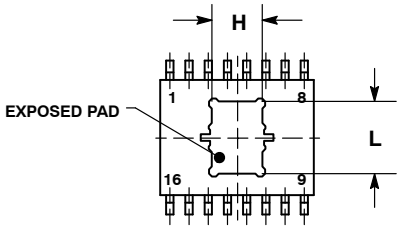
TOP VIEW



SIDE VIEW

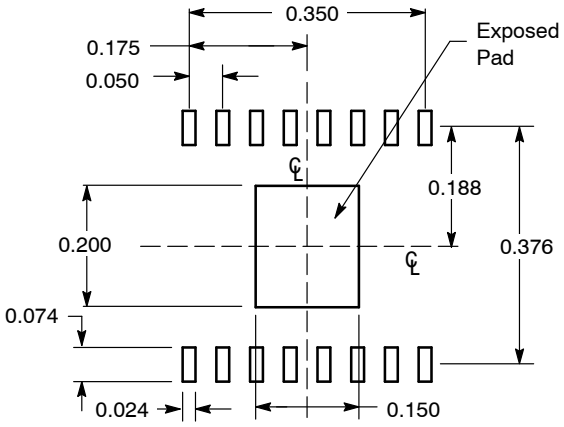


DETAIL E



BOTTOM VIEW

SOLDERING FOOTPRINT*



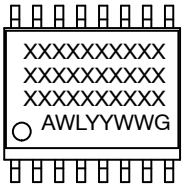
DIMENSIONS: INCHES

*For additional information on our Pb–Free strategy and soldering details, please download the **onsemi** Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A AND B DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE PROTRUSION SHALL BE 0.13 (0.005) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.
6. 751R–01 OBSOLETE, NEW STANDARD 751R–02.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	10.15	10.45	0.400	0.411
B	7.40	7.60	0.292	0.299
C	2.35	2.65	0.093	0.104
D	0.35	0.49	0.014	0.019
F	0.50	0.90	0.020	0.035
G	1.27 BSC		0.050 BSC	
H	3.45	3.66	0.136	0.144
J	0.25	0.32	0.010	0.012
K	0.00	0.10	0.000	0.004
L	4.72	4.93	0.186	0.194
M	0 °	7 °	0 °	7 °
P	10.05	10.55	0.395	0.415
R	0.25	0.75	0.010	0.029

GENERIC MARKING DIAGRAM*



XXXXX = Specific Device Code
A = Assembly Location
WL = Wafer Lot
YY = Year
WW = Work Week
G = Pb–Free Package

*This information is generic. Please refer to device data sheet for actual part marking. Pb–Free indicator, “G” or microdot “ ▪”, may or may not be present.

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