# Linear Regulator - Low Dropout, Very Low $I_q$

# NCV8664

The NCV8664 is a precision 3.3 V and 5.0 V fixed output, low dropout integrated voltage regulator with an output current capability of 150 mA. Careful management of light load current consumption, combined with a low leakage process, achieve a typical quiescent current of 22 μA.

NCV8664 is pin and functionally compatible with NCV4264 and NCV4264−2, and it could replace these parts when very low quiescent current is required.

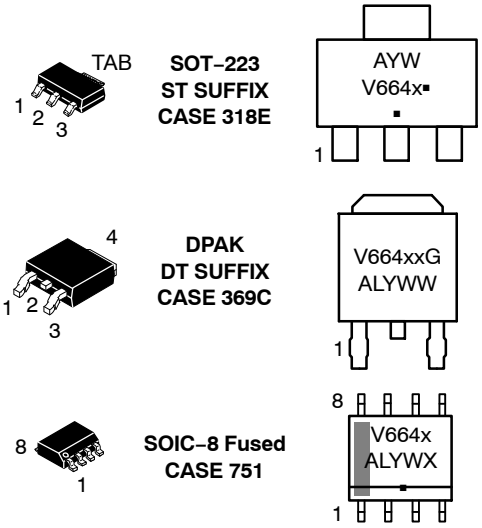
The output voltage is accurate within ±2.0%, and maximum dropout voltage is 600 mV at full rated load current.

It is internally protected against input supply reversal, output overcurrent faults, and excess die temperature. No external components are required to enable these features.

### Features

- 3.3 V, 5.0 V Fixed Output
- ±2.0% Output Accuracy, Over Full Temperature Range
- 30 μA Maximum Quiescent Current at $I_{OUT}$ = 100 μA
- 600 mV Maximum Dropout Voltage at 150 mA Load Current
- Wide Input Voltage Operating Range of 4.5 V to 45 V
- Internal Fault Protection
  - −42 V Reverse Voltage
  - Short Circuit/Overcurrent
  - Thermal Overload
- NCV Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC−Q100 Qualified and PPAP Capable
- EMC Compliant
- These are Pb−Free Devices

### MARKING DIAGRAMS




xx = Voltage Rating DPAK
(50 = 5.0 V Version)
(33 = 3.3 V Version)
x = Voltage Rating SOT223
(5 = 5.0 V Version)
(3 = 3.3 V Version)
A = Assembly Location
L = Wafer Lot
Y = Year
W, WW = Work Week
▪ or G = Pb−Free Package

(Note: Microdot may be in either location)

### PIN CONNECTIONS

| (SOT−223/DPAK) | | (SOIC−8 Fused) | |
|---|---|---|---|
| PIN | FUNCTION | PIN | FUNCTION |
| 1 | $V_{IN}$ | 1 | NC |
| 2,TAB | GND | 2, | $V_{IN}$ |
| 3 | $V_{OUT}$ | 3 | GND |
| | | 4. | $V_{OUT}$ |
| | | 5−8. | NC |

### ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 11 of this data sheet.

NOTE: Some of the devices on this data sheet have been **DISCONTINUED**. Please refer to the table on page 11.

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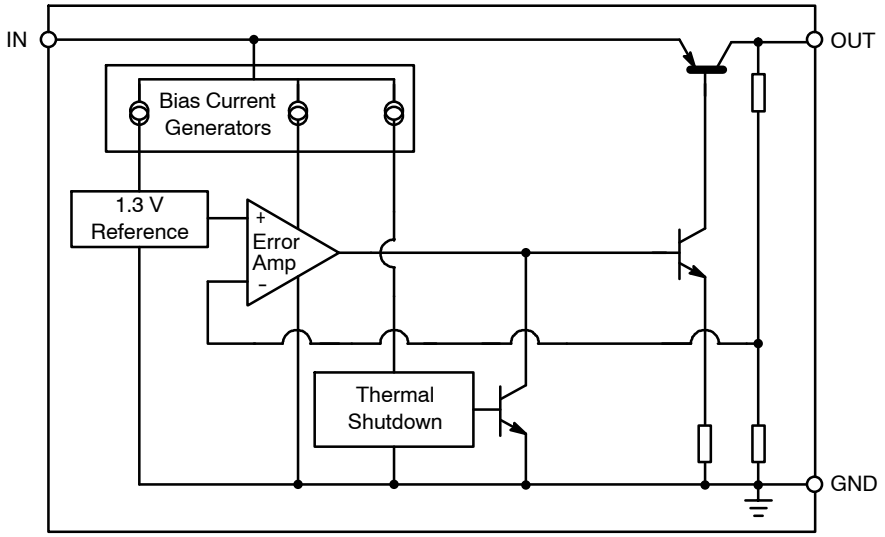



**Figure 1. Block Diagram**

## PIN FUNCTION DESCRIPTION

| Pin No. | | Symbol | Function |
|---|---|---|---|
| DPAK/SOT−223 | SOIC−8 | | |
| 1 | 2 | $V_{IN}$ | Unregulated input voltage; 4.5 V to 45 V. |
| 2 | 3 | GND | Ground; substrate. |
| 3 | 4 | $V_{OUT}$ | Regulated output voltage; collector of the internal PNP pass transistor. |
| TAB | – | GND | Ground; substrate and best thermal connection to the die. |
| – | 1, 5−8 | NC | No Connection. |

## OPERATING RANGE

| Pin Symbol, Parameter | Symbol | Min | Max | Unit |
|---|---|---|---|---|
| $V_{IN}$, DC Input Operating Voltage | $V_{IN}$ | 4.5 | +45 | V |
| Junction Temperature Operating Range | $T_J$ | −40 | +150 | °C |

## MAXIMUM RATINGS

| Rating | Symbol | Min | Max | Unit |
|---|---|---|---|---|
| $V_{IN}$, DC Voltage | $V_{IN}$ | −42 | +45 | V |
| $V_{OUT}$, DC Voltage | $V_{OUT}$ | −0.3 | +18 | V |
| Storage Temperature | $T_{stg}$ | −55 | +150 | °C |
| ESD Capability, Human Body Model (Note 1) | $V_{ESDHB}$ | 4000 | – | V |
| ESD Capability, Machine Model (Note 1) | $V_{ESDMIM}$ | 200 | – | V |

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. This device series incorporates ESD protection and is tested by the following methods:
   ESD HBM tested per AEC−Q100−002 (EIA/JESD22−A 114C)
   ESD MM tested per AEC−Q100−003 (EIA/JESD22−A 115C)

## THERMAL RESISTANCE

| Parameter | | Symbol | Condition | Min | Max | Unit |
|---|---|---|---|---|---|---|
| Junction−to−Ambient | DPAK<br>SOT−223<br>SOIC−8 Fused | $R_{\theta JA}$ | | –<br>–<br>– | 101 (Note 2)<br>99 (Note 2)<br>145 | °C/W |
| Junction−to−Case | DPAK<br>SOT−223<br>SOIC−8 Fused | $R_{\theta JC}$ | | –<br>–<br>– | 9.0<br>17<br>– | °C/W |

2. 1 oz., 100 $mm^2$ copper area.

## LEAD SOLDERING TEMPERATURE AND MSL

| Rating | | Symbol | Min | Max | Unit |
|---|---|---|---|---|---|
| Lead Temperature Soldering<br>Reflow (SMD Styles Only), Lead Free (Note 3) | | $T_{sld}$ | <br>– | <br>265 pk | °C |
| Moisture Sensitivity Level | SOT223<br>DPAK<br>SOIC−8 Fused | MSL | 3<br>2<br>1 | –<br>–<br>– | – |

3. Lead Free, 60 sec – 150 sec above 217°C, 40 sec max at peak.

## ELECTRICAL CHARACTERISTICS ($V_{IN}$ = 13.5 V, Tj = −40°C to +150°C, unless otherwise noted.)

| Characteristic | Symbol | Test Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| Output Voltage<br>5.0 V Version | $V_{OUT}$ | 0.1 mA ≤ $I_{OUT}$ ≤ 150 mA (Note 4)<br>6.0 V ≤ $V_{IN}$ ≤ 28 V | 4.900 | 5.000 | 5.100 | V |
| Output Voltage<br>5.0 V Version | $V_{OUT}$ | 0 mA ≤ $I_{OUT}$ ≤ 150 mA<br>5.5 V ≤ $V_{IN}$ ≤ 28 V<br>−40°C ≤ $T_J$ ≤ 125°C | 4.900 | 5.000 | 5.100 | V |
| Output Voltage<br>3.3 V Version | $V_{OUT}$ | 0.1 mA ≤ $I_{OUT}$ ≤ 150 mA (Note 4)<br>4.5 V ≤ $V_{IN}$ ≤ 28 V | 3.234 | 3.300 | 3.366 | V |
| Line Regulation<br>5.0 V Version | $\Delta V_{OUT}$ vs. $V_{IN}$ | $I_{OUT}$ = 5.0 mA<br>6.0 V ≤ $V_{IN}$ ≤ 28 V | −25 | 5.0 | +25 | mV |
| Line Regulation<br>3.3 V Version | $\Delta V_{OUT}$ vs. $V_{IN}$ | $I_{OUT}$ = 5.0 mA<br>4.5 V ≤ $V_{IN}$ ≤ 28 V | −25 | 5.0 | +25 | mV |
| Load Regulation | $\Delta V_{OUT}$ vs. $I_{OUT}$ | 1.0 mA ≤ $I_{OUT}$ ≤ 150 mA<br>(Note 4) | −35 | 5.0 | +35 | mV |
| Dropout Voltage<br>5.0 V Version | $V_{IN}$–$V_{OUT}$ | $I_Q$ = 100 mA (Notes 4 & 5)<br>$I_Q$ = 150 mA (Notes 4 & 5) | –<br>– | 265<br>315 | 500<br>600 | mV |
| Dropout Voltage<br>3.3 V Version | $V_{IN}$–$V_{OUT}$ | $I_Q$ = 100 mA (Notes 4 & 7)<br>$I_Q$ = 150 mA (Notes 4 & 7) | –<br>– | –<br>– | 1.266<br>1.266 | V |
| Quiescent Current | $I_q$ | $I_{OUT}$ = 100 μA<br>$T_J$ = 25°C<br>$T_J$ = −40°C to +85°C | <br>–<br>– | <br>21<br>22 | <br>29<br>30 | μA |
| Active Ground Current | $I_{G(ON)}$ | $I_{OUT}$ = 50 mA (Note 4)<br>$I_{OUT}$ = 150 mA (Note 4) | –<br>– | 1.3<br>8.0 | 3<br>15 | mA |
| Power Supply Rejection | PSRR | $V_{RIPPLE}$ = 0.5 $V_{P-P}$, F = 100 Hz | – | 67 | – | dB |
| Output Capacitor for Stability<br>5.0 V Version | $C_{OUT}$<br>ESR | $I_{OUT}$ = 0.1 mA to 150 mA<br>(Note 4) | 10<br>– | –<br>– | –<br>9.0 | μF<br>Ω |
| Output Capacitor for Stability<br>3.3 V Version | $C_{OUT}$<br>ESR | $I_{OUT}$ = 0.1 mA to 150 mA<br>(Note 4) | 22<br>– | –<br>– | –<br>18 | μF<br>Ω |

### PROTECTION

| | | | | | | |
|---|---|---|---|---|---|---|
| Current Limit | $I_{OUT(LIM)}$ | $V_{OUT}$ = 4.5 V (5.0 V Version) (Note 4)<br>$V_{OUT}$ = 3.0 V (3.3 V Version) (Note 4) | 150<br>150 | –<br>– | 500<br>500 | mA |
| Short Circuit Current Limit | $I_{OUT(SC)}$ | $V_{OUT}$ = 0 V (Note 4) | 100 | – | 500 | mA |
| Thermal Shutdown Threshold | $T_{TSD}$ | (Note 6) | 150 | – | 200 | °C |

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

4. Use pulse loading to limit power dissipation.
5. Dropout voltage = ($V_{IN}$ – $V_{OUT}$), measured when the output voltage has dropped 100 mV relative to the nominal value obtained with $V_{IN}$ = 13.5 V.
6. Not tested in production. Limits are guaranteed by design.
7. $V_{DO}$ = $V_{IN}$ – $V_{OUT}$. For output voltage set to < 4.5 V, $V_{DO}$ will be constrained by the minimum input voltage.

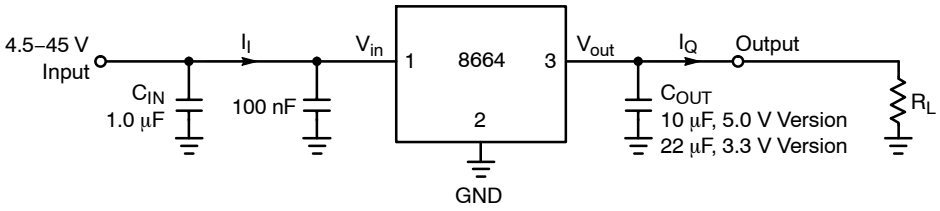



**Figure 2. Measurement Circuit**

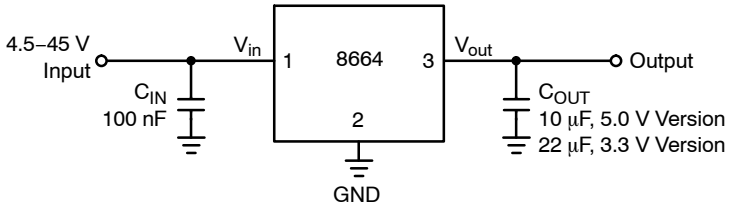



**Figure 3. Applications Circuit**

## Typical Curves

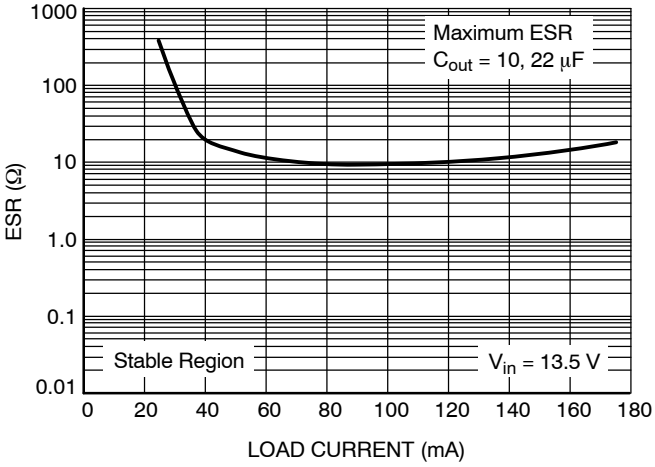



**Figure 4. ESR Characterization, 5.0 V Version**

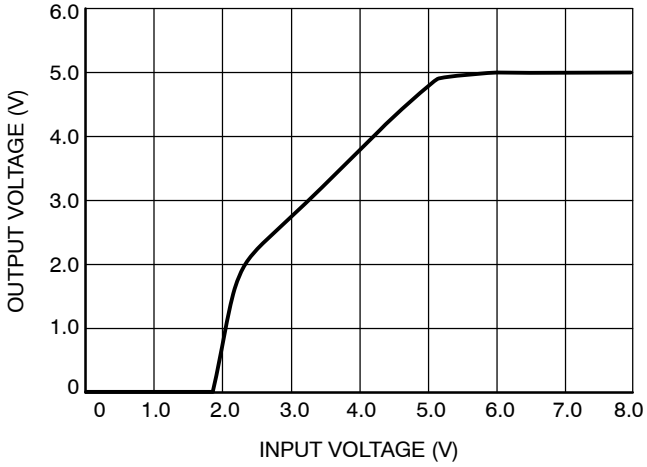



**Figure 5. Output Voltage vs. Input Voltage, 5.0 V Version**

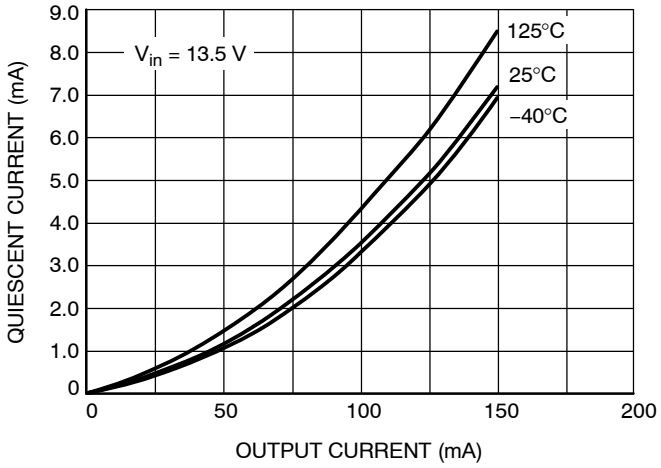



**Figure 6. Current Consumption vs. Output Load, 5.0 V Version**

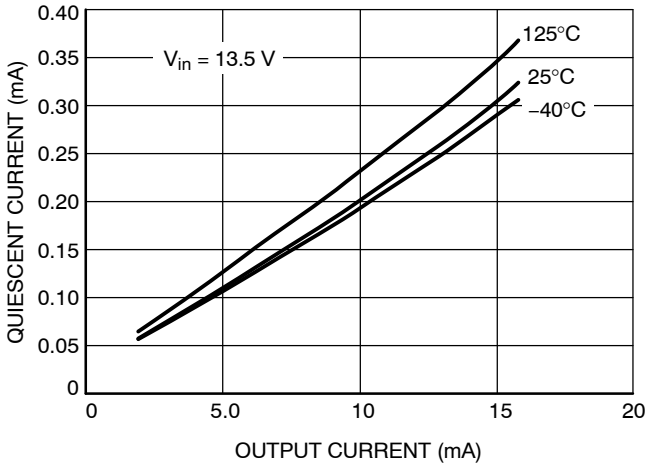



**Figure 7. Current Consumption vs. Output Load (Low Load), 5.0 V Version**

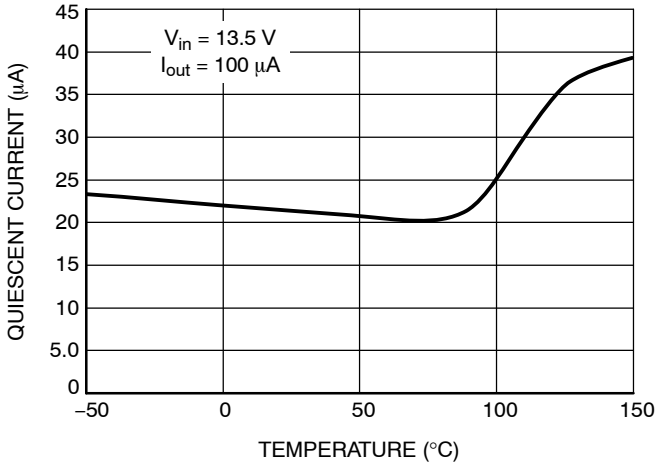



**Figure 8. Quiescent Current vs. Temperature, 5.0 V Version**

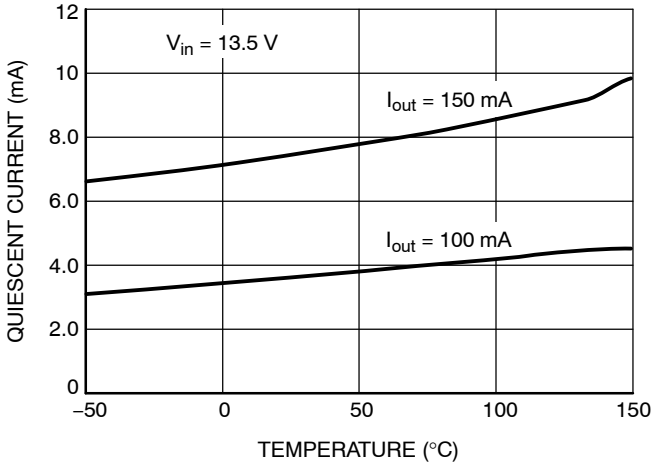



**Figure 9. Quiescent Current vs. Temperature, 5.0 V Version**

## Typical Curves

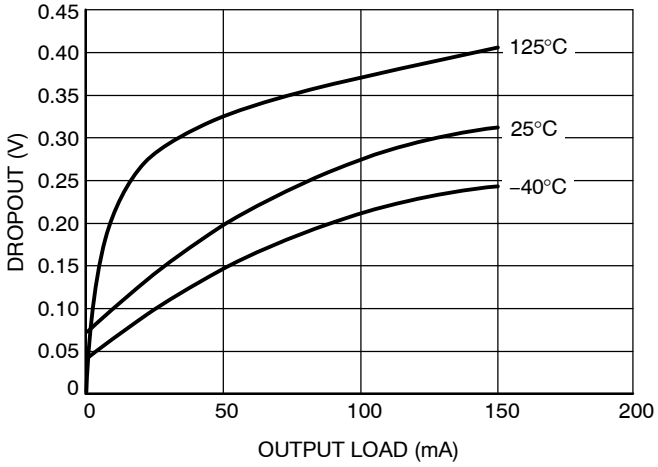



**Figure 10. Dropout Voltage vs. Output Load, 5.0 V Version**

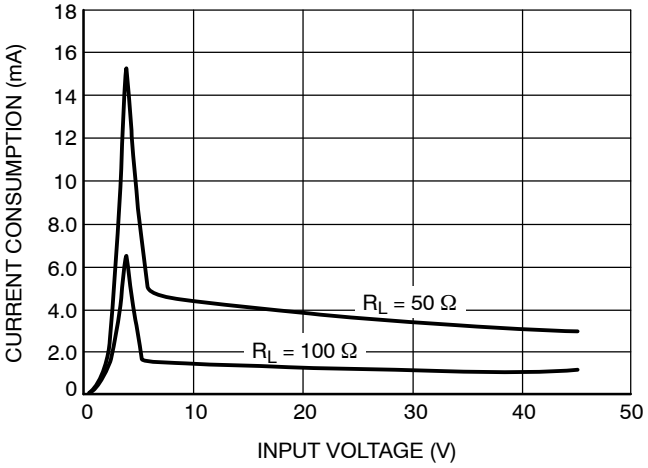



**Figure 11. Current Consumption vs. Input Voltage, 5.0 V Version**

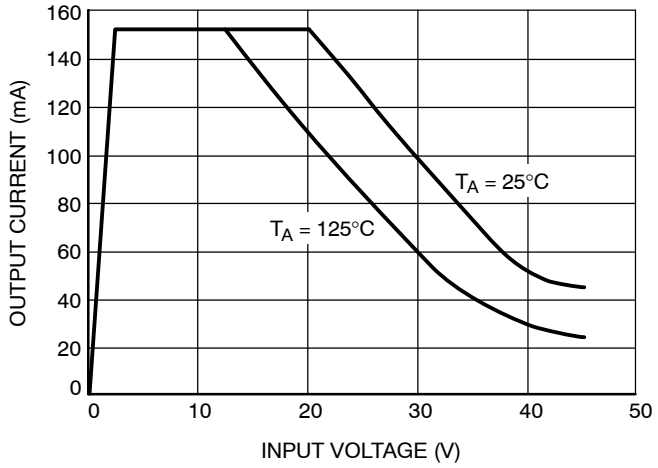



**Figure 12. Output Current vs. Input Voltage, 5.0 V Version**

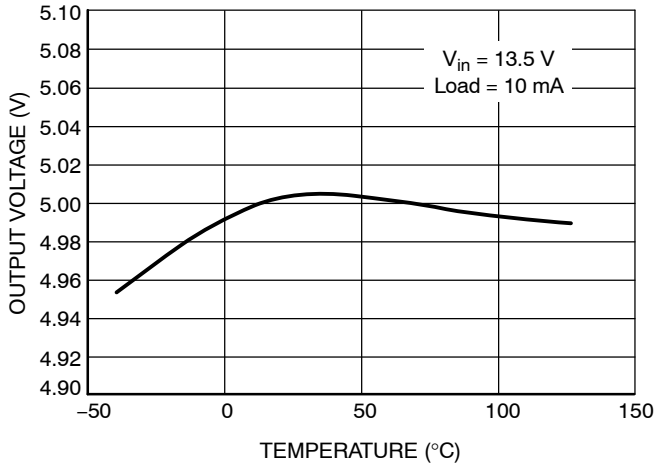



**Figure 13. Output Voltage vs. Temperature, 5.0 V Version**

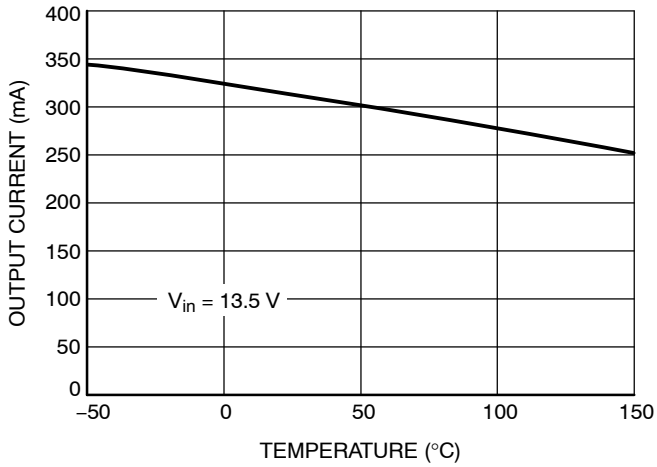



**Figure 14. Current Limit vs. Temperature, 5.0 V Version**

## Typical Curves

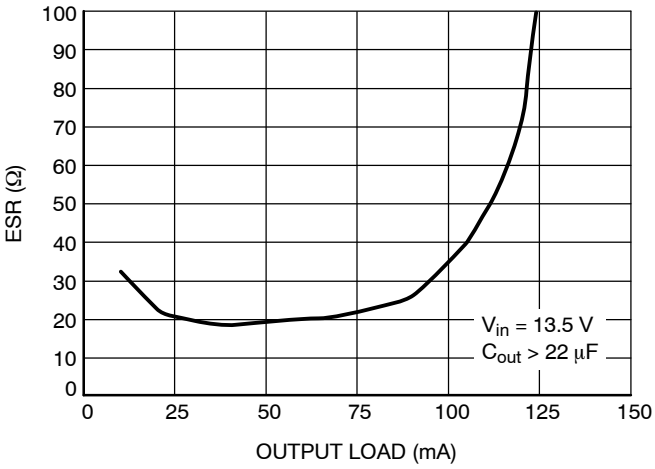



**Figure 15. ESR Stability, 3.3 V Version**

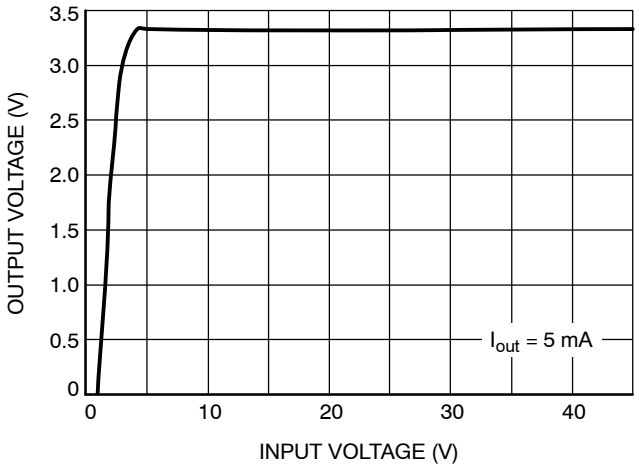



**Figure 16. Output Voltage vs. Input Voltage, 3.3 V Version**

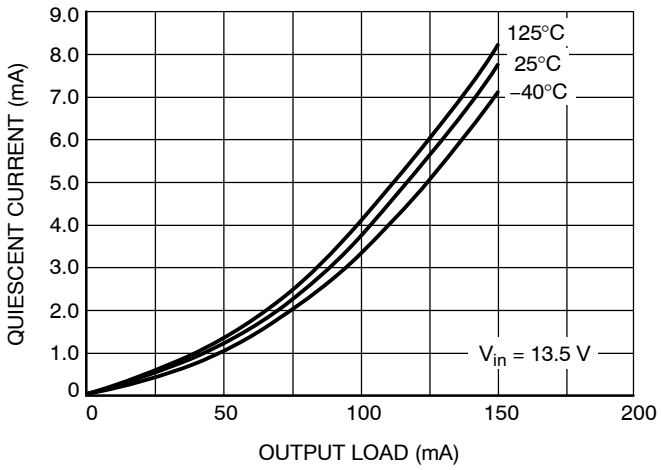



**Figure 17. Current Consumption vs. Output Load, 3.3 V Version**

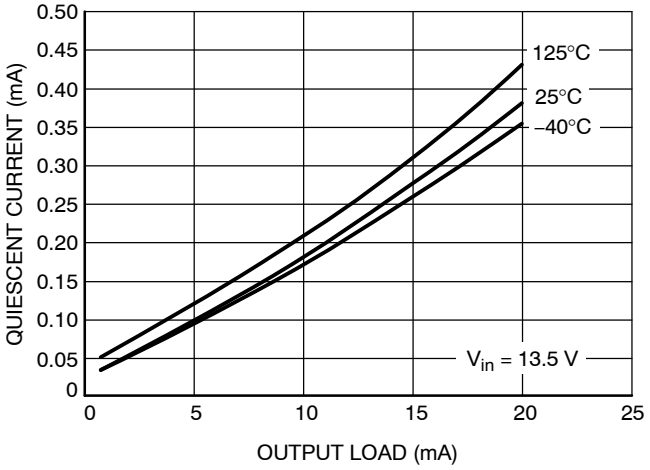



**Figure 18. Current Consumption vs. Output Load (Low Load), 3.3 V Version**

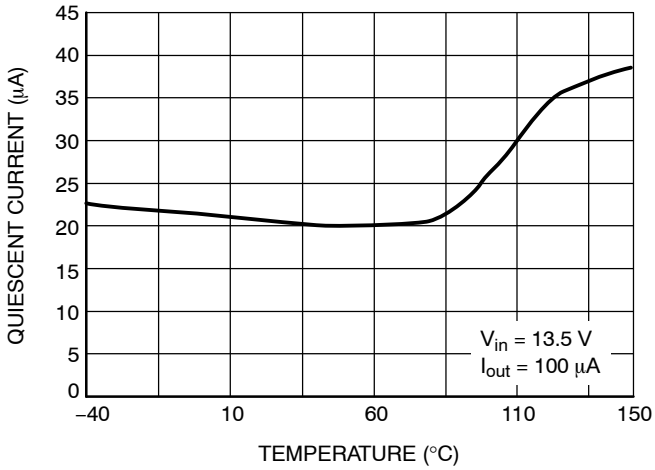



**Figure 19. Quiescent Current vs. Temperature, 3.3 V Version**

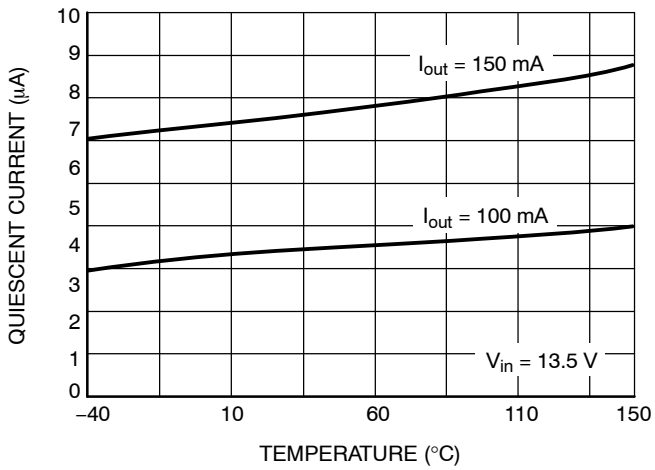



**Figure 20. Quiescent Current vs. Temperature, 3.3 V Version**

## Typical Curves

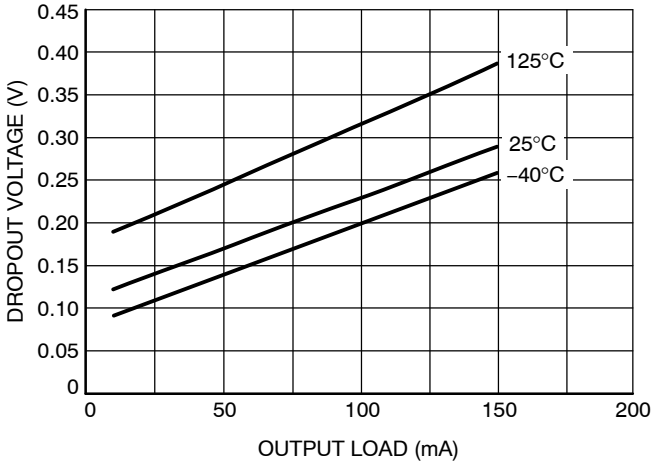



**Figure 21. Dropout Voltage, 3.3 V Version**

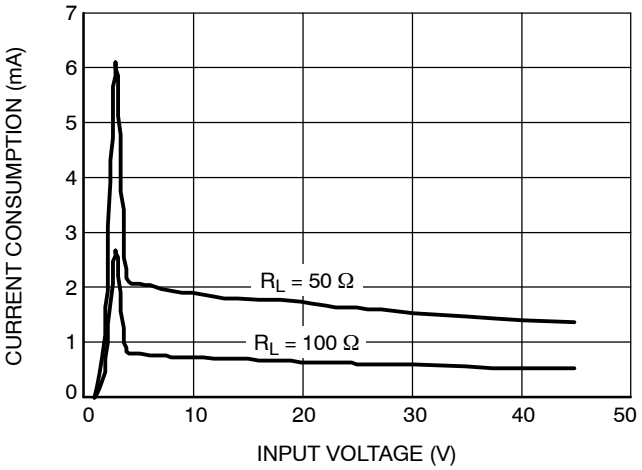



**Figure 22. Current Consumption vs. Input Voltage, 3.3 V Version**

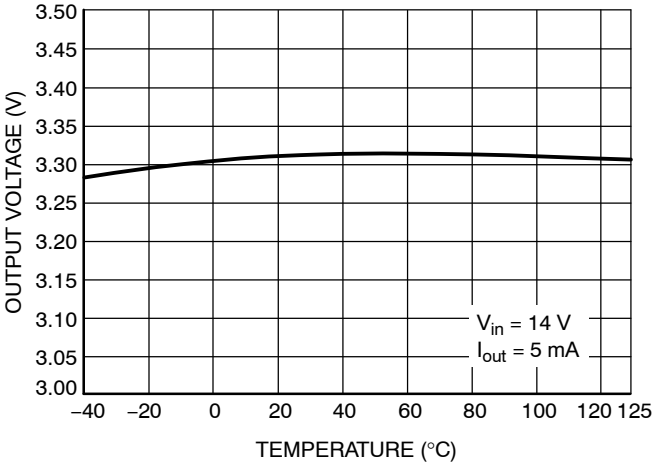



**Figure 23. Output Voltage vs. Temperature, 3.3 V Version**

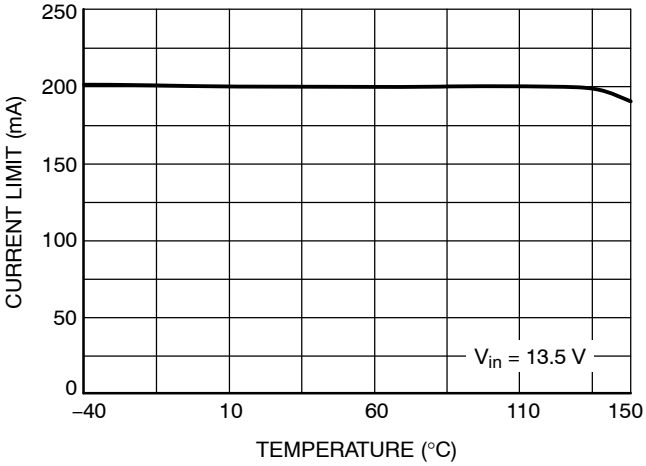



**Figure 24. Short Circuit Current Limit vs. Temperature, 3.3 V Version**

### Circuit Description

The NCV8664 is a precision trimmed 3.3 V and 5.0 V fixed output regulator. Careful management of light load consumption combined with a low leakage process results in a typical quiescent current of 22 μA. The device has current capability of 150 mA, with 600 mV of dropout voltage at full rated load current. The regulation is provided by a PNP pass transistor controlled by an error amplifier with a bandgap reference. The regulator is protected by both current limit and short circuit protection. Thermal shutdown occurs above 150°C to protect the IC during overloads and extreme ambient temperatures.

### Regulator

The error amplifier compares the reference voltage to a sample of the output voltage ($V_{out}$) and drives the base of a PNP series pass transistor by a buffer. The reference is a bandgap design to give it a temperature−stable output. Saturation control of the PNP is a function of the load current and input voltage. Over saturation of the output power device is prevented, and quiescent current in the ground pin is minimized. The NCV8664 is equipped with foldback current protection. This protection is designed to reduce the current limit during an overcurrent situation.

### Regulator Stability Considerations

The input capacitor $C_{IN}$ in Figure 2 is necessary for compensating input line reactance. Possible oscillations caused by input inductance and input capacitance can be damped by using a resistor of approximately 1 Ω in series with $C_{IN}$. The output or compensation capacitor, $C_{OUT}$ helps determine three main characteristics of a linear regulator: startup delay, load transient response and loop stability. The capacitor value and type should be based on cost, availability, size and temperature constraints. Tantalum, aluminum electrolytic, film, or ceramic capacitors are all acceptable solutions, however, attention must be paid to ESR constraints. The aluminum electrolytic capacitor is the least expensive solution, but, if the circuit operates at low temperatures (−25°C to −40°C), both the value and ESR of the capacitor will vary considerably. The capacitor manufacturer's data sheet usually provides this information. The value for the output capacitor $C_{OUT}$ shown in Figure 2 should work for most applications; however, it is not necessarily the optimized solution. Stability is guaranteed at values $C_{OUT} \geq 10$ μF and ESR ≤ 9 Ω for 5.0 V version, and $C_{OUT} \geq 22$ μF and ESR ≤ 18 Ω for 3.3 V version, within the operating temperature range. Actual limits are shown in a graph in the Typical Performance Characteristics section.

### Calculating Power Dissipation in a Single Output Linear Regulator

The maximum power dissipation for a single output regulator (Figure 3) is:

$$P_{D(max)} = [V_{IN(max)} - V_{OUT(min)}] \cdot I_{Q(max)} + V_{I(max)} \cdot I_q \quad \text{(eq. 1)}$$

Where:

$V_{IN(max)}$ is the maximum input voltage,

$V_{OUT(min)}$ is the minimum output voltage,

$I_{Q(max)}$ is the maximum output current for the application, and $I_q$ is the quiescent current the regulator consumes at $I_{Q(max)}$.

Once the value of $P_{D(Max)}$ is known, the maximum permissible value of $R_{\theta JA}$ can be calculated:

$$P_{\theta JA} = \frac{150^{o}C - T_A}{P_D} \quad \text{(eq. 2)}$$

The value of $R_{\theta JA}$ can then be compared with those in the package section of the data sheet. Those packages with $R_{\theta JA}$'s less than the calculated value in Equation 2 will keep the die temperature below 150°C. In some cases, none of the packages will be sufficient to dissipate the heat generated by the IC, and an external heat sink will be required. The current flow and voltages are shown in the Measurement Circuit Diagram.

### Heat Sinks

For proper heat sinking of the SOIC−8 Lead device, connect pins 5 − 8 to the heat sink.

A heat sink effectively increases the surface area of the package to improve the flow of heat away from the IC and into the surrounding air. Each material in the heat flow path between the IC and the outside environment will have a thermal resistance. Like series electrical resistances, these resistances are summed to determine the value of $R_{\theta JA}$:

$$R_{\theta JA} = R_{\theta JC} + R_{\theta CS} + R_{\theta SA} \quad \text{(eq. 3)}$$

Where:

$R_{\theta JC}$ = the junction−to−case thermal resistance,

$R_{\theta CS}$ = the case−to−heat sink thermal resistance, and

$R_{\theta SA}$ = the heat sink−to−ambient thermal resistance.

$R_{\theta JA}$ appears in the package section of the data sheet.

Like $R_{\theta JA}$, it too is a function of package type. $R_{\theta CS}$ and $R_{\theta SA}$ are functions of the package type, heat sink and the interface between them. These values appear in data sheets of heat sink manufacturers. Thermal, mounting, and heat sinking are discussed in the **onsemi** application note AN1040/D, available on the **onsemi** Website.

**EMC−Characteristics: Conducted Susceptibility**

All EMC−Characteristics are based on limited samples and not part of production testing, according to 47A/658/CD IEC62132−4 (Direct Power Injection)

**Test Conditions**

| | |
|---|---|
| Supply Voltage | $V_{IN}$ = 12 V |
| Temperature | $T_A$ = 23°C ±5°C |
| Load | $R_L$ = 35 Ω |

**Direct Power Injection:** 33 dBm forward power CW

**Acceptance Criteria:** Amplitude Dev. max 2% of Output Voltage

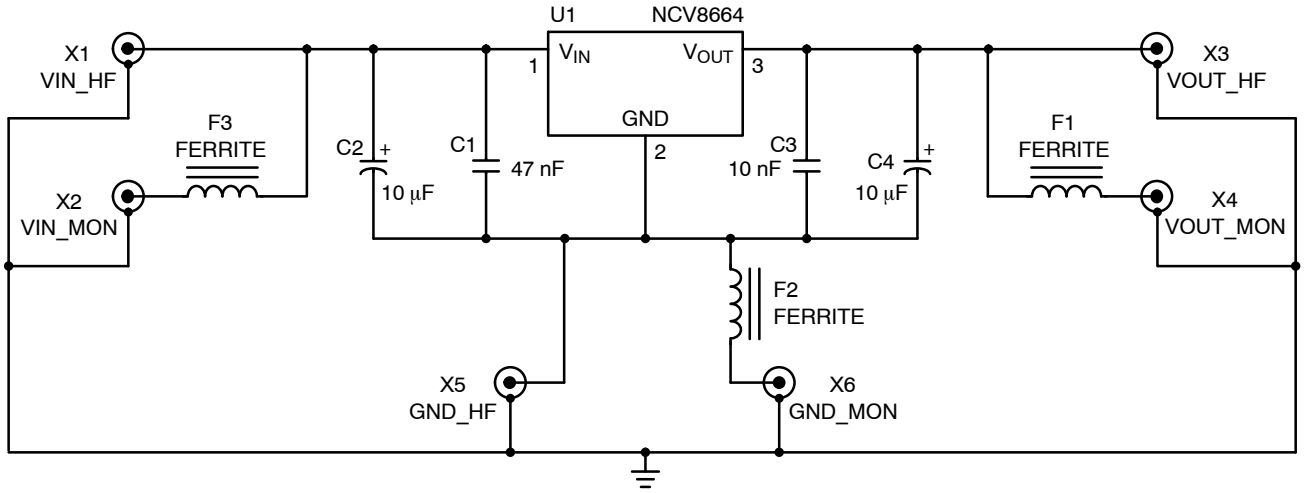



**Figure 25. Test Circuit**

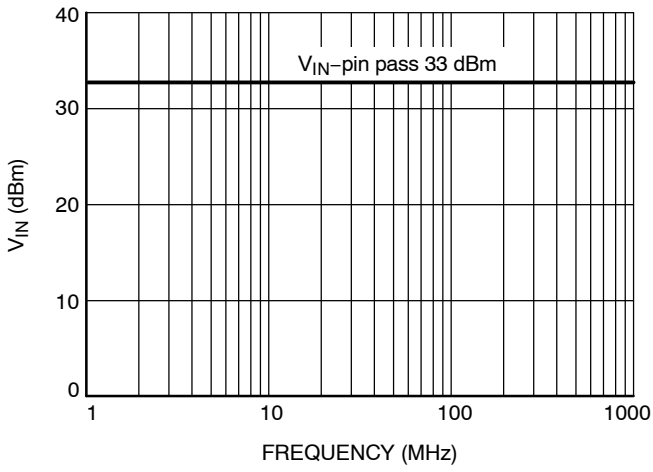



**Figure 26. Typical $V_{IN}$−pin Susceptibility**

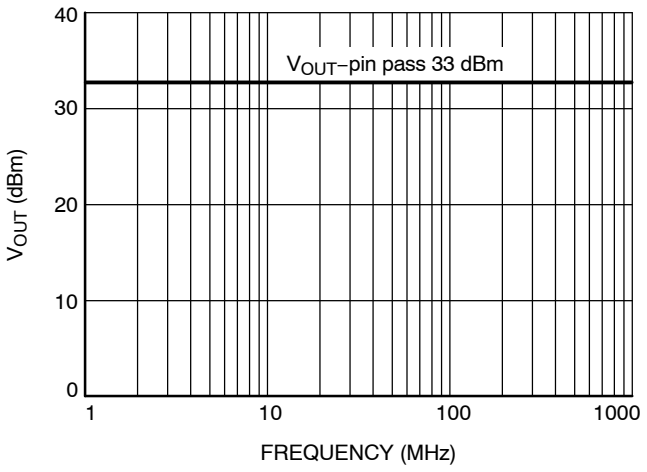



**Figure 27. Typical $V_{OUT}$−pin Susceptibility**

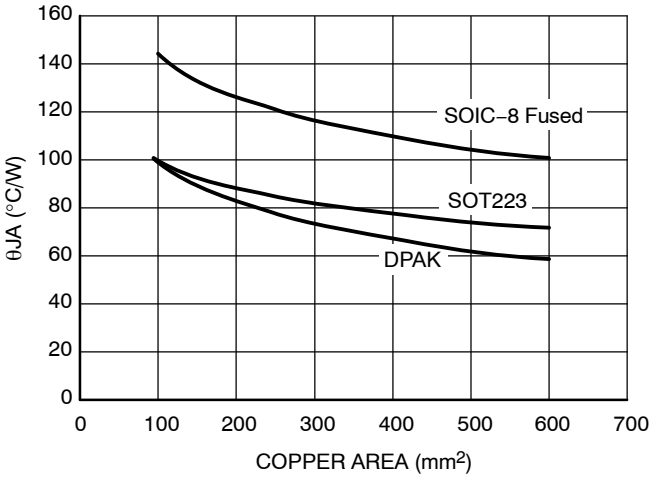



**Figure 28. θJA vs. Copper Spreader Area**

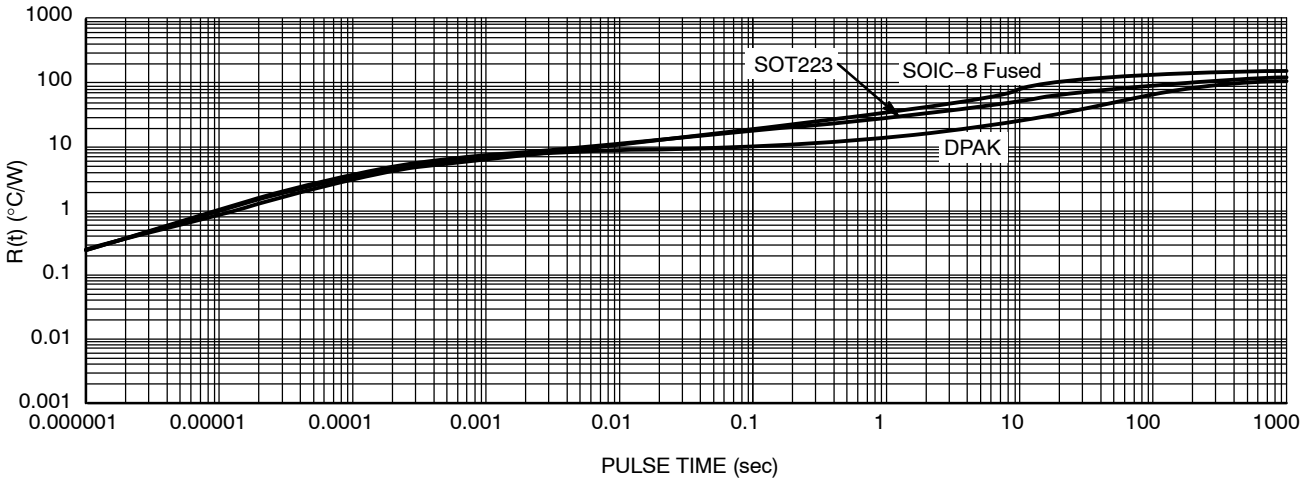



**Figure 29. Single−Pulse Heating Curves**

## ORDERING INFORMATION

| Device* | Marking | Package | Shipping† |
|---|---|---|---|
| NCV8664DT50RKG | V66450G | DPAK (Pb−Free) | 2500 / Tape & Reel |
| NCV8664ST50T3G | V6645 | SOT−223 (Pb−Free) | 4000 / Tape & Reel |

**DISCONTINUED** (Note 8)

| | | | |
|---|---|---|---|
| NCV8664D50R2G | V6645 | SOIC−8 Fused (Pb−Free) | 2500 / Tape & Reel |
| NCV8664D50G | V6645 | SOIC−8 Fused (Pb−Free) | 98 Units / Rail |
| NCV8664DT33RKG | V66433G | DPAK (Pb−Free) | 2500 / Tape & Reel |
| NCV8664ST33T3G | V6643 | SOT−223 (Pb−Free) | 4000 / Tape & Reel |

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specification Brochure, BRD8011/D.

*NCV Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC−Q100 Qualified and PPAP Capable.

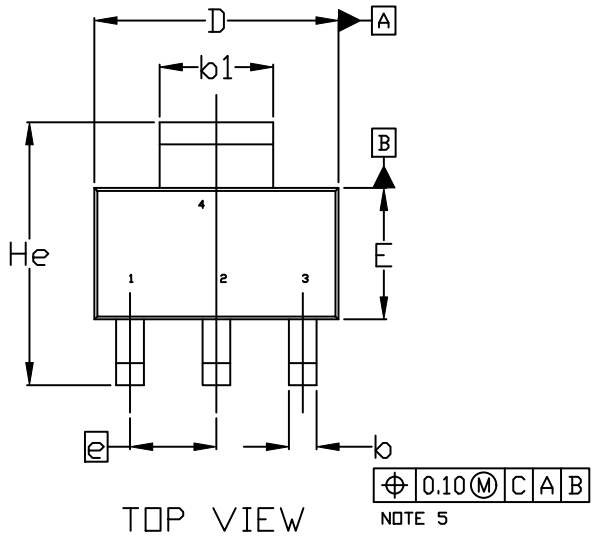
8. **DISCONTINUED:** These devices are not recommended for new design. Please contact your **onsemi** representative for information. The most current information on these devices may be available on www.onsemi.com.

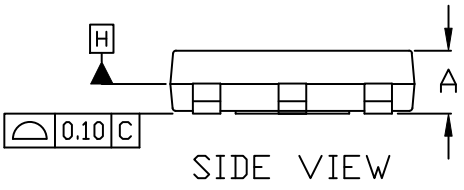


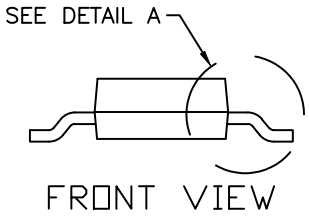
**SCALE 1:1**

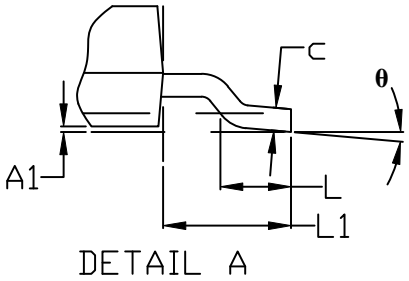
**SOT−223 (TO−261)**
CASE 318E−04
ISSUE R

DATE 02 OCT 2018



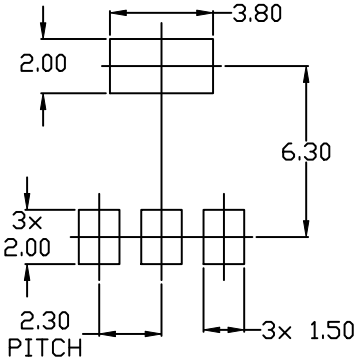




NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS
3. DIMENSIONS D & E DO NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH, PROTRUSIONS OR GATE BURRS SHALL NOT EXCEED 0.200MM PER SIDE.
4. DATUMS A AND B ARE DETERMINED AT DATUM H.
5. A1 IS DEFINED AS THE VERTICAL DISTANCE FROM THE SEATING PLANE TO THE LOWEST POINT OF THE PACKAGE BODY.
6. POSITIONAL TOLERANCE APPLIES TO DIMENSIONS b AND b1.

| | MILLIMETERS | | |
|---|---|---|---|
| DIM | MIN. | NOM. | MAX. |
| A | 1.50 | 1.63 | 1.75 |
| A1 | 0.02 | 0.06 | 0.10 |
| b | 0.60 | 0.75 | 0.89 |
| b1 | 2.90 | 3.06 | 3.20 |
| c | 0.24 | 0.29 | 0.35 |
| D | 6.30 | 6.50 | 6.70 |
| E | 3.30 | 3.50 | 3.70 |
| e | 2.30 BSC | | |
| L | 0.20 | --- | --- |
| L1 | 1.50 | 1.75 | 2.00 |
| He | 6.70 | 7.00 | 7.30 |
| θ | 0° | --- | 10° |




RECOMMENDED MOUNTING FOOTPRINT



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**SOT−223 (TO−261)**
CASE 318E−04
ISSUE R

DATE 02 OCT 2018

STYLE 1:
PIN 1. BASE
2. COLLECTOR
3. EMITTER
4. COLLECTOR

STYLE 2:
PIN 1. ANODE
2. CATHODE
3. NC
4. CATHODE

STYLE 3:
PIN 1. GATE
2. DRAIN
3. SOURCE
4. DRAIN

STYLE 4:
PIN 1. SOURCE
2. DRAIN
3. GATE
4. DRAIN

STYLE 5:
PIN 1. DRAIN
2. GATE
3. SOURCE
4. GATE

STYLE 6:
PIN 1. RETURN
2. INPUT
3. OUTPUT
4. INPUT

STYLE 7:
PIN 1. ANODE 1
2. CATHODE
3. ANODE 2
4. CATHODE

STYLE 8:
CANCELLED

STYLE 9:
PIN 1. INPUT
2. GROUND
3. LOGIC
4. GROUND

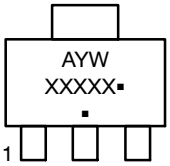
STYLE 10:
PIN 1. CATHODE
2. ANODE
3. GATE
4. ANODE

STYLE 11:
PIN 1. MT 1
2. MT 2
3. GATE
4. MT 2

STYLE 12:
PIN 1. INPUT
2. OUTPUT
3. NC
4. OUTPUT

STYLE 13:
PIN 1. GATE
2. COLLECTOR
3. EMITTER
4. COLLECTOR

## GENERIC MARKING DIAGRAM*




A = Assembly Location
Y = Year
W = Work Week
XXXXX = Specific Device Code
▪ = Pb−Free Package

(Note: Microdot may be in either location)

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, “G” or microdot “▪”, may or may not be present. Some products may not follow the Generic Marking.

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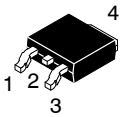
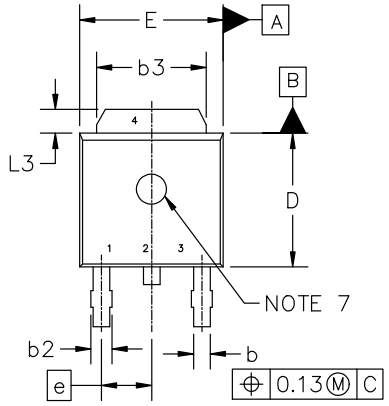


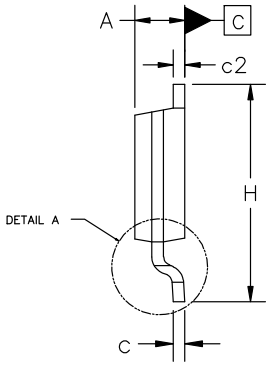

**SCALE 1:1**

**DPAK−3 6.10x6.54x2.28, 2.29P**
CASE 369C
ISSUE L

DATE 24 AUG 2026

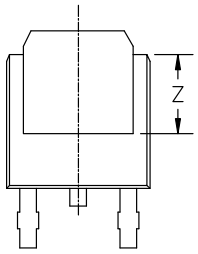



TOP VIEW

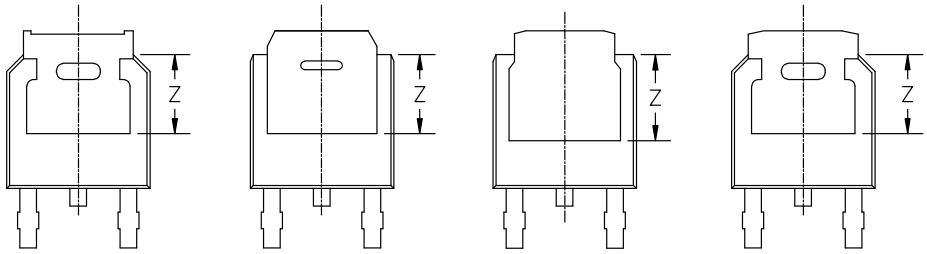



SIDE VIEW

| MILLIMETERS | | | |
|---|---|---|---|
| DIM | MIN | NOM | MAX |
| A | 2.18 | 2.28 | 2.38 |
| A1 | 0.00 | −−− | 0.13 |
| b | 0.63 | 0.76 | 0.89 |
| b2 | 0.72 | 0.93 | 1.14 |
| b3 | 4.57 | 5.02 | 5.46 |
| c | 0.46 | 0.54 | 0.61 |
| c2 | 0.46 | 0.54 | 0.61 |
| D | 5.97 | 6.10 | 6.22 |
| E | 6.35 | 6.54 | 6.73 |
| e | 2.29 BSC | | |
| H | 9.40 | 9.91 | 10.41 |
| L | 1.40 | 1.59 | 1.78 |
| L1 | 2.90 REF | | |
| L2 | 0.51 BSC | | |
| L3 | 0.89 | −−− | 1.27 |
| L4 | −−− | −−− | 1.01 |
| Z | 3.93 | −−− | −−− |



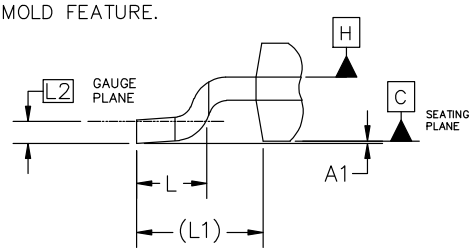

BOTTOM VIEW



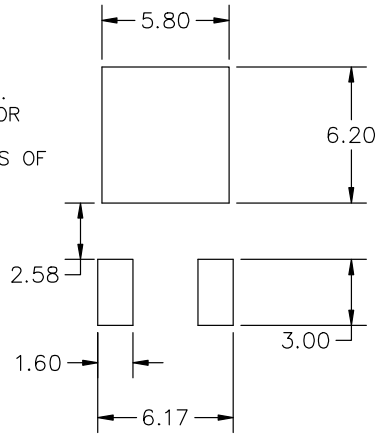

ALTERNATE CONSTRUCTIONS

NOTES:

1. DIMENSIONING AND TOLERANCING ASME Y14.5M, 2018.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. THERMAL PAD CONTOUR OPTIONAL WITHIN DIMENSIONS b3, L3, AND Z.
4. DIMENSIONS D AND E DO NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR BURRS.
5. DIMENSIONS D AND E ARE DETERMINED AT THE OUTERMOST EXTREMES OF THE PLASTIC BODY.
6. DATUMS A AND B ARE DETERMINED AT DATUM PLANE H.
7. OPTIONAL MOLD FEATURE.




DETAIL A
ROTATED 90° CW




RECOMMENDED MOUNTING FOOTPRINT*
*For additional information on our Pb−Free strategy and soldering details, please download the onsemi Soldering and Mounting Techniques reference manual, SOLDERRM/D.

| | | |
|---|---|---|
| **DOCUMENT NUMBER:** | **98AON10527D** | Electronic versions are uncontrolled except when accessed directly from the Document Repository. Printed versions are uncontrolled except when stamped "CONTROLLED COPY" in red. |
| **DESCRIPTION:** | **DPAK−3 6.10x6.54x2.28, 2.29P** | **PAGE 1 OF 2** |

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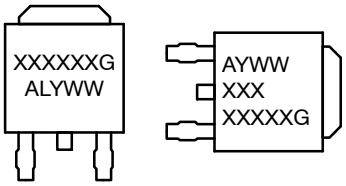
**DPAK−3 6.10x6.54x2.28, 2.29P**
CASE 369C
ISSUE L

DATE 24 AUG 2026

## GENERIC MARKING DIAGRAM*




**IC** **Discrete**

| | |
|---|---|
| XXXXXX | = Device Code |
| A | = Assembly Location |
| L | = Wafer Lot |
| Y | = Year |
| WW | = Work Week |
| G | = Pb−Free Package |

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, “G” or microdot “▪”, may or may not be present. Some products may not follow the Generic Marking.

STYLE 1:
PIN 1. BASE
2. COLLECTOR
3. EMITTER
4. COLLECTOR

STYLE 2:
PIN 1. GATE
2. DRAIN
3. SOURCE
4. DRAIN

STYLE 3:
PIN 1. ANODE
2. CATHODE
3. ANODE
4. CATHODE

STYLE 4:
PIN 1. CATHODE
2. ANODE
3. GATE
4. ANODE

STYLE 5:
PIN 1. GATE
2. ANODE
3. CATHODE
4. ANODE

STYLE 6:
PIN 1. MT1
2. MT2
3. GATE
4. MT2

STYLE 7:
PIN 1. GATE
2. COLLECTOR
3. EMITTER
4. COLLECTOR

STYLE 8:
PIN 1. N/C
2. CATHODE
3. ANODE
4. CATHODE

STYLE 9:
PIN 1. ANODE
2. CATHODE
3. RESISTOR ADJUST
4. CATHODE

STYLE 10:
PIN 1. CATHODE
2. ANODE
3. CATHODE
4. ANODE

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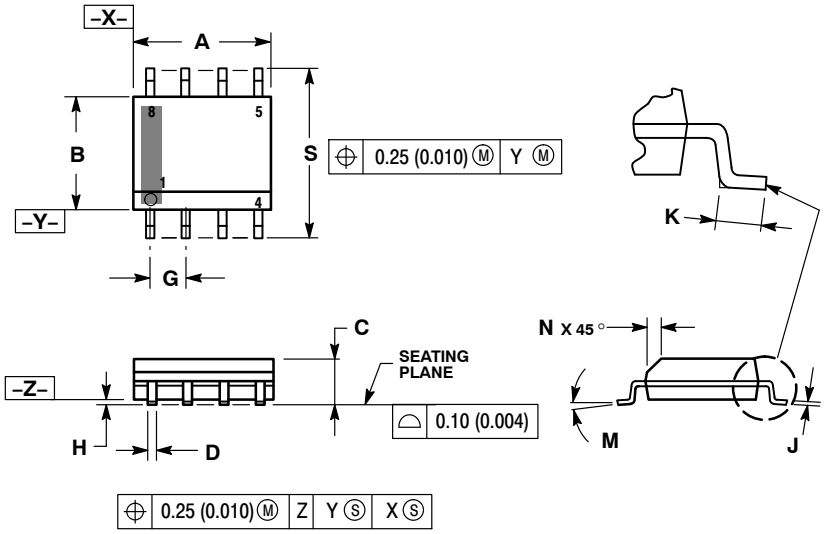
**SCALE 1:1**

**SOIC−8 NB**
CASE 751−07
ISSUE AK

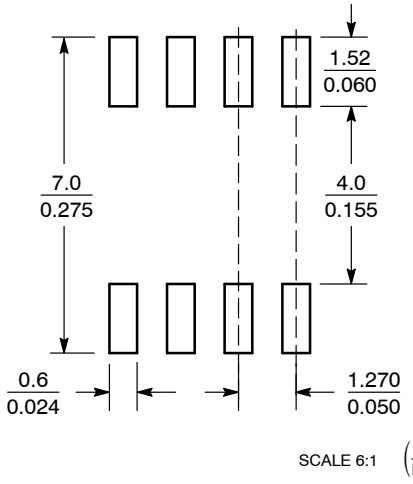
DATE 16 FEB 2011




NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A AND B DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 (0.005) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.
6. 751−01 THRU 751−06 ARE OBSOLETE. NEW STANDARD IS 751−07.

| | MILLIMETERS | | INCHES | |
|---|---|---|---|---|
| DIM | MIN | MAX | MIN | MAX |
| A | 4.80 | 5.00 | 0.189 | 0.197 |
| B | 3.80 | 4.00 | 0.150 | 0.157 |
| C | 1.35 | 1.75 | 0.053 | 0.069 |
| D | 0.33 | 0.51 | 0.013 | 0.020 |
| G | 1.27 BSC | | 0.050 BSC | |
| H | 0.10 | 0.25 | 0.004 | 0.010 |
| J | 0.19 | 0.25 | 0.007 | 0.010 |
| K | 0.40 | 1.27 | 0.016 | 0.050 |
| M | 0° | 8° | 0° | 8° |
| N | 0.25 | 0.50 | 0.010 | 0.020 |
| S | 5.80 | 6.20 | 0.228 | 0.244 |

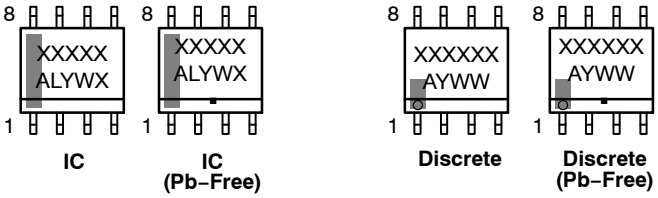
## SOLDERING FOOTPRINT*




SCALE 6:1 (mm / inches)

*For additional information on our Pb−Free strategy and soldering details, please download the **onsemi** Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

## GENERIC MARKING DIAGRAM*




XXXXX = Specific Device Code
A = Assembly Location
L = Wafer Lot
Y = Year
W = Work Week
▪ = Pb−Free Package

XXXXXX = Specific Device Code
A = Assembly Location
Y = Year
WW = Work Week
▪ = Pb−Free Package

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, "G" or microdot "▪", may or may not be present. Some products may not follow the Generic Marking.

**STYLES ON PAGE 2**

| | | | |
|---|---|---|---|
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| **DESCRIPTION:** | **SOIC−8 NB** | | **PAGE 1 OF 2** |

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**SOIC−8 NB**
CASE 751−07
ISSUE AK

DATE 16 FEB 2011

STYLE 1:
PIN 1. EMITTER
2. COLLECTOR
3. COLLECTOR
4. EMITTER
5. EMITTER
6. BASE
7. BASE
8. EMITTER

STYLE 2:
PIN 1. COLLECTOR, DIE, #1
2. COLLECTOR, #1
3. COLLECTOR, #2
4. COLLECTOR, #2
5. BASE, #2
6. EMITTER, #2
7. BASE, #1
8. EMITTER, #1

STYLE 3:
PIN 1. DRAIN, DIE #1
2. DRAIN, #1
3. DRAIN, #2
4. DRAIN, #2
5. GATE, #2
6. SOURCE, #2
7. GATE, #1
8. SOURCE, #1

STYLE 4:
PIN 1. ANODE
2. ANODE
3. ANODE
4. ANODE
5. ANODE
6. ANODE
7. ANODE
8. COMMON CATHODE

STYLE 5:
PIN 1. DRAIN
2. DRAIN
3. DRAIN
4. DRAIN
5. GATE
6. GATE
7. SOURCE
8. SOURCE

STYLE 6:
PIN 1. SOURCE
2. DRAIN
3. DRAIN
4. SOURCE
5. SOURCE
6. GATE
7. GATE
8. SOURCE

STYLE 7:
PIN 1. INPUT
2. EXTERNAL BYPASS
3. THIRD STAGE SOURCE
4. GROUND
5. DRAIN
6. GATE 3
7. SECOND STAGE Vd
8. FIRST STAGE Vd

STYLE 8:
PIN 1. COLLECTOR, DIE #1
2. BASE, #1
3. BASE, #2
4. COLLECTOR, #2
5. COLLECTOR, #2
6. EMITTER, #2
7. EMITTER, #1
8. COLLECTOR, #1

STYLE 9:
PIN 1. EMITTER, COMMON
2. COLLECTOR, DIE #1
3. COLLECTOR, DIE #2
4. EMITTER, COMMON
5. EMITTER, COMMON
6. BASE, DIE #2
7. BASE, DIE #1
8. EMITTER, COMMON

STYLE 10:
PIN 1. GROUND
2. BIAS 1
3. OUTPUT
4. GROUND
5. GROUND
6. BIAS 2
7. INPUT
8. GROUND

STYLE 11:
PIN 1. SOURCE 1
2. GATE 1
3. SOURCE 2
4. GATE 2
5. DRAIN 2
6. DRAIN 2
7. DRAIN 1
8. DRAIN 1

STYLE 12:
PIN 1. SOURCE
2. SOURCE
3. SOURCE
4. GATE
5. DRAIN
6. DRAIN
7. DRAIN
8. DRAIN

STYLE 13:
PIN 1. N.C.
2. SOURCE
3. SOURCE
4. GATE
5. DRAIN
6. DRAIN
7. DRAIN
8. DRAIN

STYLE 14:
PIN 1. N−SOURCE
2. N−GATE
3. P−SOURCE
4. P−GATE
5. P−DRAIN
6. P−DRAIN
7. N−DRAIN
8. N−DRAIN

STYLE 15:
PIN 1. ANODE 1
2. ANODE 1
3. ANODE 1
4. ANODE 1
5. CATHODE, COMMON
6. CATHODE, COMMON
7. CATHODE, COMMON
8. CATHODE, COMMON

STYLE 16:
PIN 1. EMITTER, DIE #1
2. BASE, DIE #1
3. EMITTER, DIE #2
4. BASE, DIE #2
5. COLLECTOR, DIE #2
6. COLLECTOR, DIE #2
7. COLLECTOR, DIE #1
8. COLLECTOR, DIE #1

STYLE 17:
PIN 1. VCC
2. V2OUT
3. V1OUT
4. TXE
5. RXE
6. VEE
7. GND
8. ACC

STYLE 18:
PIN 1. ANODE
2. ANODE
3. SOURCE
4. GATE
5. DRAIN
6. DRAIN
7. CATHODE
8. CATHODE

STYLE 19:
PIN 1. SOURCE 1
2. GATE 1
3. SOURCE 2
4. GATE 2
5. DRAIN 2
6. MIRROR 2
7. DRAIN 1
8. MIRROR 1

STYLE 20:
PIN 1. SOURCE (N)
2. GATE (N)
3. SOURCE (P)
4. GATE (P)
5. DRAIN
6. DRAIN
7. DRAIN
8. DRAIN

STYLE 21:
PIN 1. CATHODE 1
2. CATHODE 2
3. CATHODE 3
4. CATHODE 4
5. CATHODE 5
6. COMMON ANODE
7. COMMON ANODE
8. CATHODE 6

STYLE 22:
PIN 1. I/O LINE 1
2. COMMON CATHODE/VCC
3. COMMON CATHODE/VCC
4. I/O LINE 3
5. COMMON ANODE/GND
6. I/O LINE 4
7. I/O LINE 5
8. COMMON ANODE/GND

STYLE 23:
PIN 1. LINE 1 IN
2. COMMON ANODE/GND
3. COMMON ANODE/GND
4. LINE 2 IN
5. LINE 2 OUT
6. COMMON ANODE/GND
7. COMMON ANODE/GND
8. LINE 1 OUT

STYLE 24:
PIN 1. BASE
2. EMITTER
3. COLLECTOR/ANODE
4. COLLECTOR/ANODE
5. CATHODE
6. CATHODE
7. COLLECTOR/ANODE
8. COLLECTOR/ANODE

STYLE 25:
PIN 1. VIN
2. N/C
3. REXT
4. GND
5. IOUT
6. IOUT
7. IOUT
8. IOUT

STYLE 26:
PIN 1. GND
2. dv/dt
3. ENABLE
4. ILIMIT
5. SOURCE
6. SOURCE
7. SOURCE
8. VCC

STYLE 27:
PIN 1. ILIMIT
2. OVLO
3. UVLO
4. INPUT+
5. SOURCE
6. SOURCE
7. SOURCE
8. DRAIN

STYLE 28:
PIN 1. SW_TO_GND
2. DASIC_OFF
3. DASIC_SW_DET
4. GND
5. V_MON
6. VBULK
7. VBULK
8. VIN

STYLE 29:
PIN 1. BASE, DIE #1
2. EMITTER, #1
3. BASE, #2
4. EMITTER, #2
5. COLLECTOR, #2
6. COLLECTOR, #2
7. COLLECTOR, #1
8. COLLECTOR, #1

STYLE 30:
PIN 1. DRAIN 1
2. DRAIN 1
3. GATE 2
4. SOURCE 2
5. SOURCE 1/DRAIN 2
6. SOURCE 1/DRAIN 2
7. SOURCE 1/DRAIN 2
8. GATE 1

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