ON Semiconductor

Is Now



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LD0 Regulator with RESET and Delay Time Select, Ultra Low I_q, 150 mA

NCV8760C

The NCV8760C is a precision ultra low Iq low dropout voltage regulator. Quiescent currents as low as 18 μA typical make it ideal for automotive applications requiring low quiescent current. Integrated control features such as Reset and Delay Time Select make it ideal for powering microprocessors.

It is available with a fixed output voltage of 5.0 V and 3.3 V and regulates within ±2.0%.

Features

- Output Voltage Options: 3.3 V and 5 V
- Output Voltage Accuracy: ±2.0%
- Output Current up to 150 mA
- Microprocessor Compatible Control Functions:
  - Delay Time Select
  - RESET Output
- Low Dropout Voltage
- Ultra Low Quiescent Current of 18 μA Typical
- Protection Features:
  - Thermal Shutdown
  - Current Limitation
- NCV Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC−Q100 Qualified and PPAP Capable
- EMC Compliant
- These Devices are Pb−Free and RoHS Compliant

Applications (for safety applications refer to Figure 29)

- Automotive:
  - Body Control Module
  - Instruments and Clusters
  - Occupant Protection and Comfort
  - Conventional Powertrain
- Battery Powered Consumer Electronics

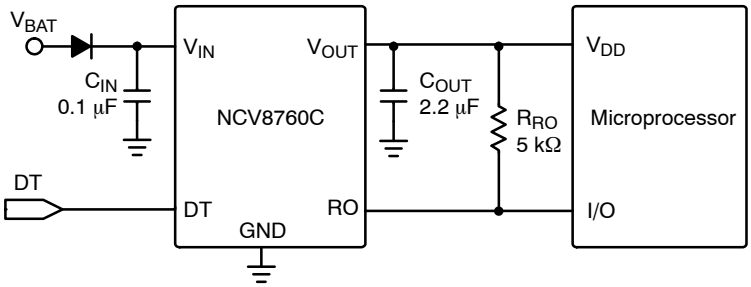

Figure 1. Application Diagram

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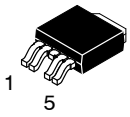
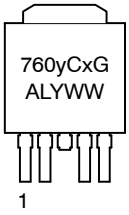
MARKING DIAGRAMS



DPAK 5−PIN
DT SUFFIX
CASE 175AA



x	= 5 for 5 V Output, 3 for 3.3 V Output
y	= 1 for 8 ms, 128 ms Reset Delay, = 2 for 8 ms, 32 ms Reset Delay = 3 for 16 ms, 64 ms Reset Delay = 4 for 32 ms, 128 ms Reset Delay
A	= Assembly Location
L	= Wafer Lot
Y	= Year
WW	= Work Week
G	= Pb−Free Package

ORDERING INFORMATION

See detailed ordering and shipping information in the dimensions section on page 13 of this data sheet.

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PIN CONNECTIONS

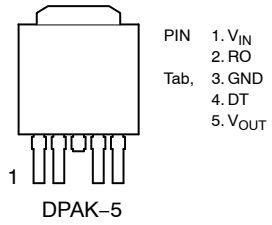


Figure 2. Pin Connections

PIN DESCRIPTIONS

Pin	Symbol	Function
1	V_{IN}	Input Supply Voltage. Connect a 0.1 μF bypass capacitor to GND at the IC.
2	RO	Reset Output. Open Drain connected to the V_{OUT} via an internal 30 kΩ pull−up resistor. Goes low when V_{OUT} drops by more than 7% from its nominal level.
3, Tab	GND	Ground
4	DT	Reset Delay Time Select. Short to GND or connect to V_{OUT} to reset delay select time value. (See DETAILED OPERATING DESCRIPTION)
5	V_{OUT}	Regulated Voltage Output. Connect a 2.2 μF capacitor to ground for typical applications.

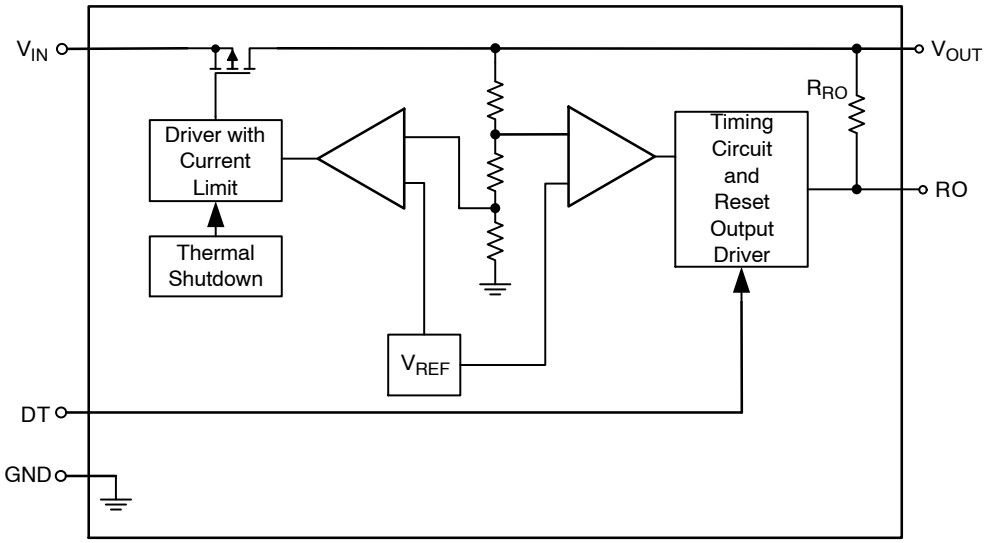


Figure 3. Block Diagram

ABSOLUTE MAXIMUM RATINGS

Rating		Symbol	Min	Max	Unit
Input Voltage (Note 1)	DC	V_{IN}	−0.3	40	V
Input Voltage (Note 2)	Load Dump − Suppressed	V_{IN}	−	45	V
Output Voltage		V_{OUT}	−0.3	7.0	V
DT (Reset Delay Time Select) Voltage		V_{DT}	−0.3	7.0	V
Reset Output Voltage		V_{RO}	−0.3	7.0	V
Junction Temperature Range		T_J	−40	150	°C
Storage Temperature Range		T_{STG}	−55	150	°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. Refer to ELECTRICAL CHARACTERISTICS and APPLICATION INFORMATION for Safe Operating Area.
2. Load Dump Test B (with centralized load dump suppression) according to ISO16750−2 standard. Guaranteed by design. Not tested in production. Passed Class B according to ISO16750−1.

ESD CAPABILITY (Note 3)

Rating	Symbol	Min	Max	Unit
ESD Capability, Human Body Model	ESD_{HBM}	−4.0	4.0	kV
ESD Capability, Charged Device Model	ESD_{CDM}	−1.0	1.0	kV

3. This device series incorporates ESD protection and is tested by the following methods:
   ESD HBM tested per AEC−Q100−002 (JS−001−2017).
   Field Induced Charge Device Model ESD characterization is not performed on plastic molded packages with body sizes 2x2 mm due to the inability of a small package body to acquire and retain enough charge to meet the minimum CDM discharge current waveform characteristic defined in JEDEC JS−002−2018.

LEAD SOLDERING TEMPERATURE AND MSL (Note 4)

Rating		Symbol	Value	Unit
Moisture Sensitivity Level	DPAK 5	MSL	1	−

4. For more information, please refer to our Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

THERMAL CHARACTERISTICS

Rating	Symbol	Value	Unit
Thermal Characteristics, DPAK−5 (Note 1)			°C/W
Thermal Resistance, Junction−to−Air (Note 5)	$R_{\theta JA}$	47	
Thermal Reference, Junction−to−Top Case (Note 5)	$R_{\Psi JC}$	9.1	
Thermal Resistance, Junction−to−Air (Note 6)	$R_{\theta JA}$	28	
Thermal Reference, Junction−to−Top Case (Note 6)	$R_{\Psi JC}$	7.4	

5. Values based on 1s0p copper area of 645 mm^2 (or 1 in^2) of 1 oz. copper thickness and FR4 PCB substrate. Single layer according to JEDEC51.3.
6. Values based on 2s2p copper area of 645 mm^2 (or 1 in^2) of 1 oz. copper thickness and FR4 PCB substrate. 4 layer according to JEDEC51.7.

RECOMMENDED OPERATING RANGES (Note 1)

Rating	Symbol	Min	Max	Unit
Input Voltage (Note 7)	V_{IN}	4.5	40	V
Junction Temperature Range	T_J	−40	150	°C

Functional operation above the stresses listed in the Recommended Operating Ranges is not implied. Extended exposure to stresses beyond the Recommended Operating Ranges limits may affect device reliability.

7. Minimum V_{IN} = 4.5 V or (V_{OUT} + V_{DO}), whichever is higher.

ELECTRICAL CHARACTERISTICS

(V_{IN} = 13.5 V, C_{IN} = 0.1 μF, C_{OUT} = 2.2 μF, Min and Max values are valid for temperature range −40°C ≤ T_J ≤ 150°C unless noted otherwise and are guaranteed by test, design or statistical correlation. Typical values are referenced to T_J = 25°C) (Note 8)

Parameter	Test Conditions	Symbol	Min	Typ	Max	Unit
Regulator Output						
Output Voltage (Accuracy %) 5.0 V 3.3 V	 V_{IN} = 5.7 V to 16 V, I_{OUT} = 0 mA to 150 mA V_{IN} = 5.55 V to 40 V, I_{OUT} = 0 mA to 100 mA V_{IN} = 4.5 V to 16 V, I_{OUT} = 0 mA to 150 mA V_{IN} = 4.5 V to 40 V, I_{OUT} = 0 mA to 100 mA	V_{OUT}	 4.9 4.9 3.234 3.234	 5.0 5.0 3.3 3.3	 5.1 5.1 3.366 3.366	V
Line Regulation	V_{IN} = 6 V to 28 V, I_{OUT} = 5 mA	Reg_{LINE}	−20	0	20	mV
Load Regulation	I_{OUT} = 0.1 mA to 150 mA	Reg_{LOAD}	−40	10	40	mV
Dropout Voltage (Note 9) 5.0 V	I_{OUT} = 100 mA I_{OUT} = 150 mA	V_{DO}	– –	125 200	300 450	mV
Quiescent Current						
Quiescent Current, $I_Q = I_{IN} - I_{OUT}$	I_{OUT} = 0 mA, T_J = 25°C I_{OUT} = 0 mA, T_J ≤ 125°C I_{OUT} = 0.1 mA, T_J = 25°C I_{OUT} = 0.1 mA, T_J ≤ 125°C	I_Q	– – – –	18 – 20 –	21 23 24 26	μA
Current Limit Protection						
Current Limit	V_{OUT} = 0.96 x V_{OUT_NOM}	I_{LIM}	205	–	525	mA
Short Circuit Current Limit	V_{OUT} = 0 V	I_{SC}	205	–	525	mA
PSRR						
Power Supply Ripple Rejection	f = 100 Hz, 0.5 V_{P-P}	PSRR	–	70	–	dB
DT (Reset Delay Time Select)						
DT Threshold Voltage Logic Low Logic High		$V_{TH(DT)}$	 – 2.0	 – –	 0.8 –	V
DT Input Current	V_{DT} = 5 V	I_{DT}	–	–	1.0	μA
Reset Output RO						
Input Voltage Reset Threshold 3.3 V	V_{IN} decreasing, $V_{OUT} > V_{RT}$	V_{IN_RT}	–	3.8	4.25	V
Output Voltage Reset Threshold	V_{OUT} decreasing	V_{RT}	90	93	96	$\%V_{OUT_NOM}$
Reset Hysteresis		V_{RH}	–	2.0	–	$\%V_{OUT_NOM}$
Reset Output Low Voltage	$V_{OUT} < V_{RT}$, I_{RO} = −1 mA	V_{ROL}	–	0.2	0.4	V
Reset Output High Voltage		V_{ROH}	V_{OUT} − 0.4	V_{OUT} − 0.2	–	V
Integrated Reset Pull Up Resistor		R_{RO}	15	30	50	kΩ
Reset Reaction Time	V_{OUT} into UV to RESET Low	t_{RR}	16	25	38	μs
RESET Delay with DT Selection						
Reset Time Out of RESET 8 ms version 16 ms version 32 ms version 64 ms version 128 ms version	V_{OUT} into regulation to RO High	t_{RDx}	 5.0 10 20 40 80	 8.0 16 32 64 128	 11.5 23 46 92 184	ms
Thermal Shutdown (Note 10)						
Thermal Shutdown Temperature		T_{SD}	150	175	195	°C
Thermal Shutdown Hysteresis		T_{SH}	–	10	–	°C

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

8. Performance guaranteed over the indicated operating temperature range by design and/or characterization tested at TA ~ TJ. Low duty cycle pulse techniques are used during testing to maintain the junction temperature as close to ambient as possible.
9. Measured when output voltage falls 100 mV below the regulated voltage at V_{IN} = 13.5 V. If V_{OUT} < 5 V, then $V_{DO} = V_{IN} - V_{OUT}$. Maximum dropout voltage value is limited by minimum input voltage V_{IN} = 4.5 V recommended for guaranteed operation at maximum output current.
10. Values based on design and/or characterization.

CHARACTERISTICS CURVES – 5.0 V Option

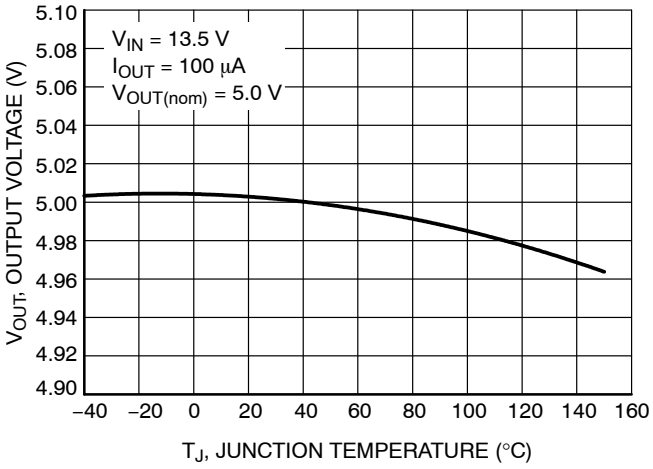


Figure 4. Output Voltage vs. Junction Temperature

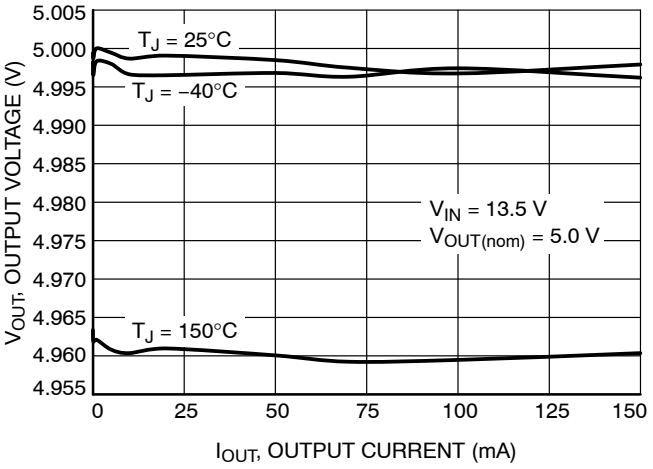


Figure 5. Output Voltage vs. Output Current

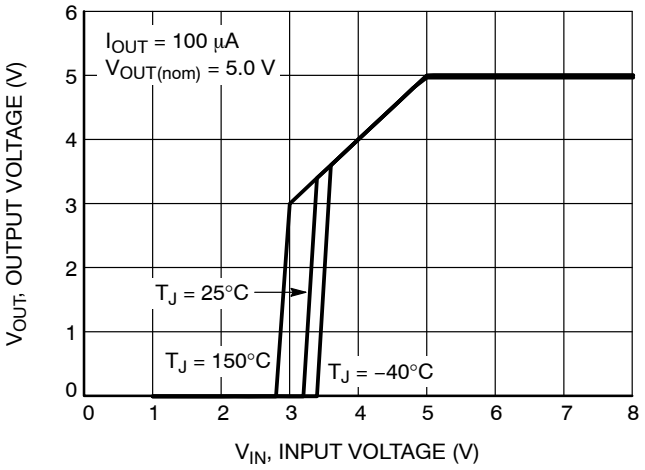


Figure 6. Output Voltage vs. Input Voltage

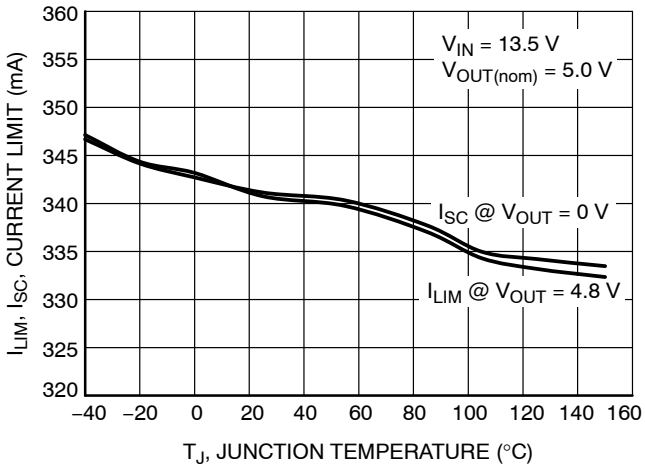


Figure 7. Output Current Limit vs. Junction Temperature

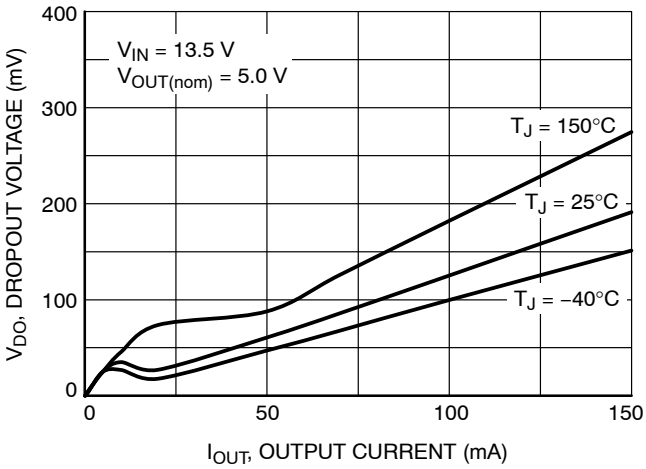


Figure 8. Dropout Voltage vs. Output Current

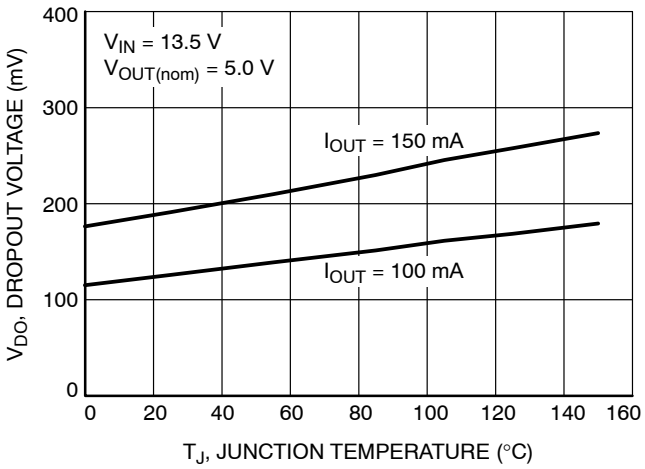


Figure 9. Dropout Voltage vs. Junction Temperature

CHARACTERISTICS CURVES – 5.0 V Option

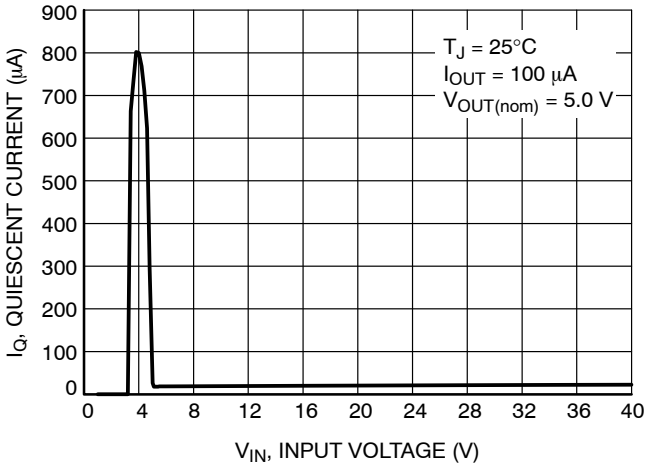


Figure 10. Quiescent Current vs. Input Voltage

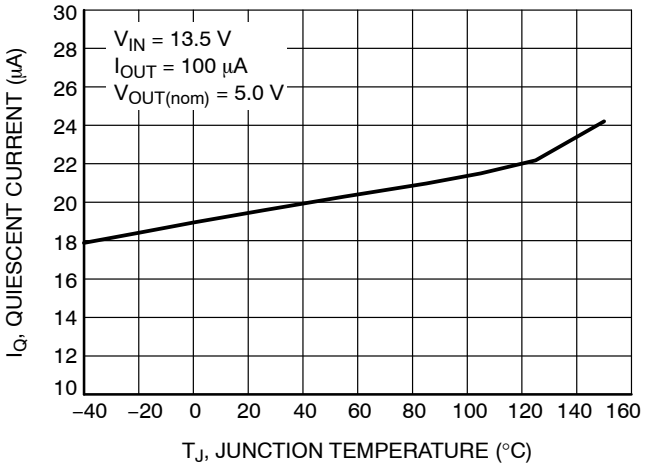


Figure 11. Quiescent Current vs. Junction Temperature

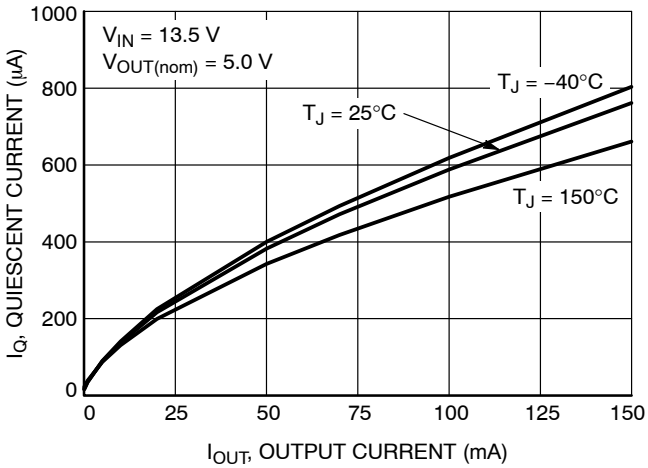


Figure 12. Quiescent Current vs. Output Current

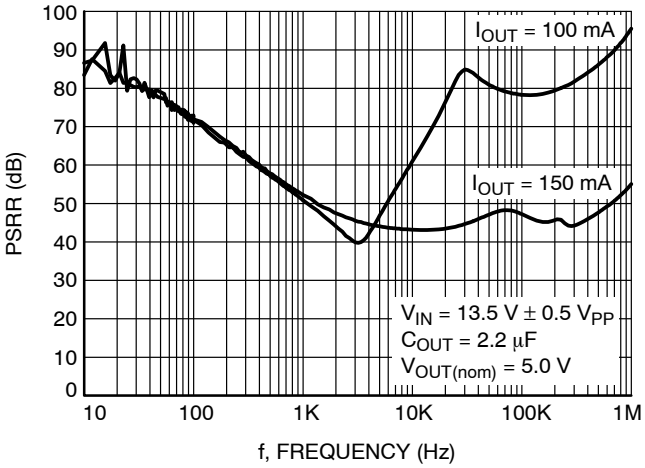


Figure 13. PSRR vs. Frequency

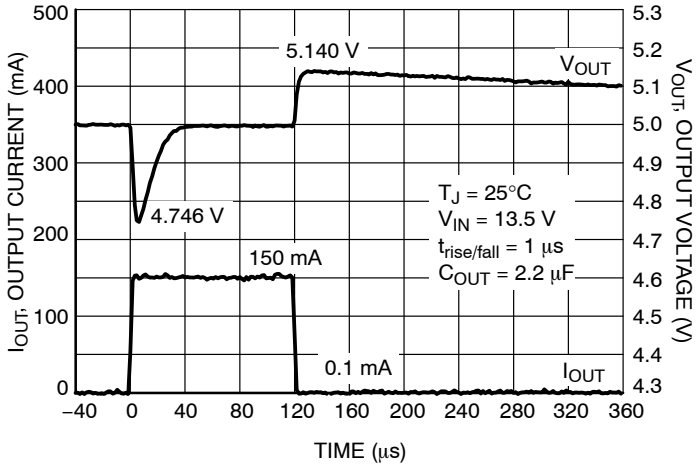


Figure 14. Load Transients

CHARACTERISTICS CURVES – 5.0 V Option

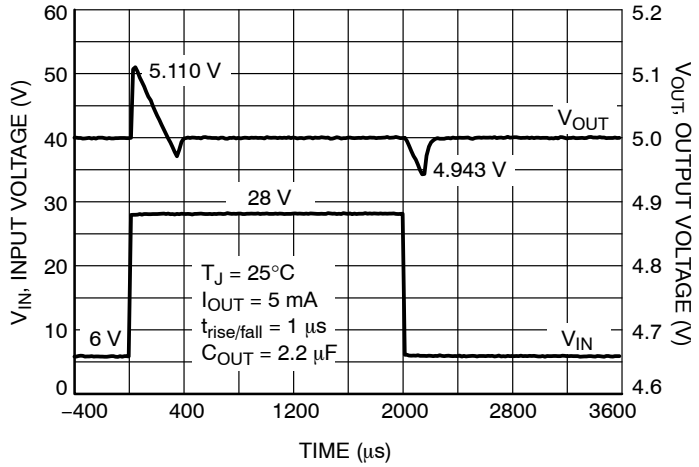


Figure 15. Line Transients

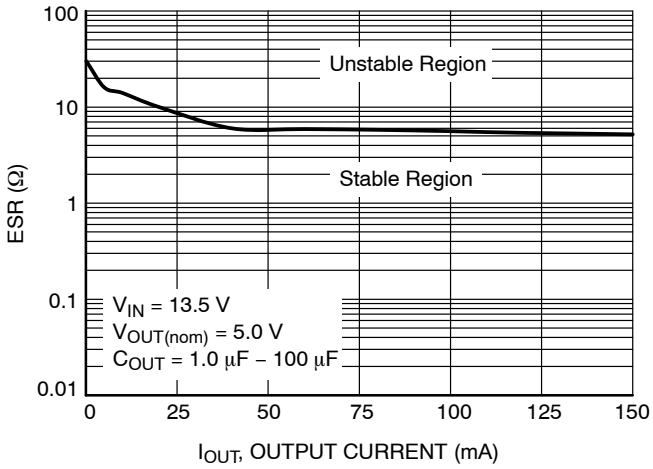


Figure 16. Output Stability with Output Capacitor ESR

CHARACTERISTICS CURVES – 3.3 V Option

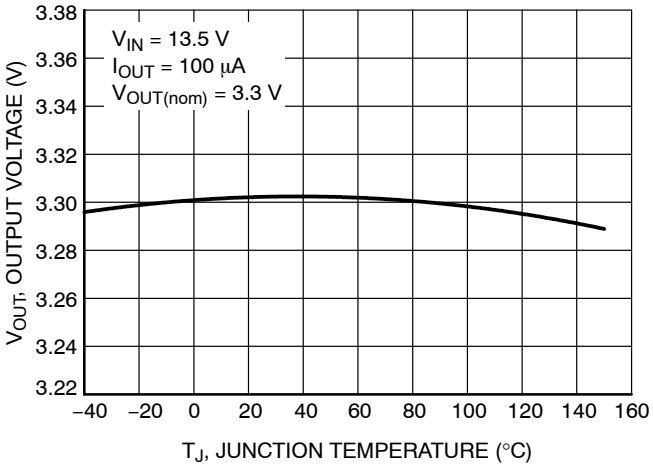


Figure 17. Output Voltage vs. Junction Temperature

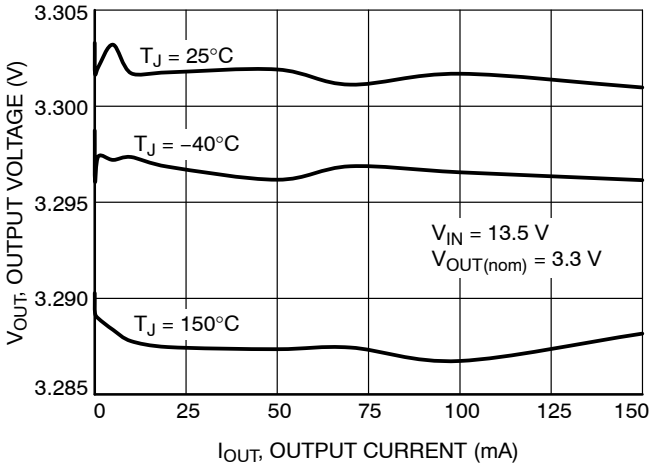


Figure 18. Output Voltage vs. Output Current

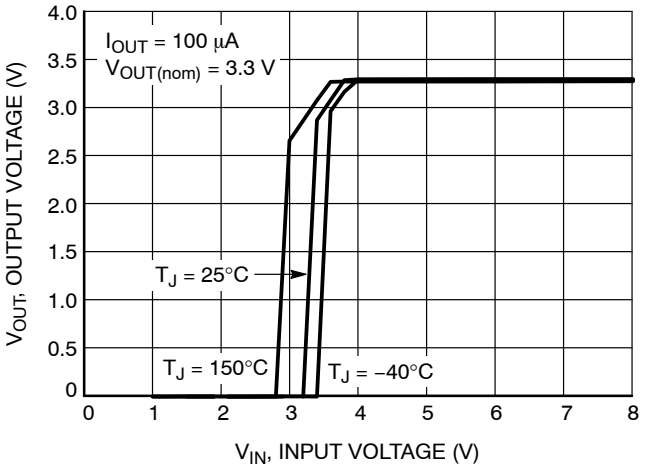


Figure 19. Output Voltage vs. Input Voltage

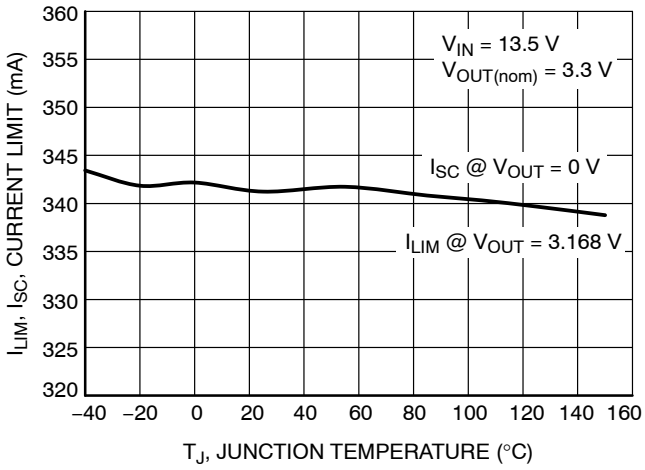


Figure 20. Output Current Limit vs. Junction Temperature

CHARACTERISTICS CURVES – 3.3 V Option

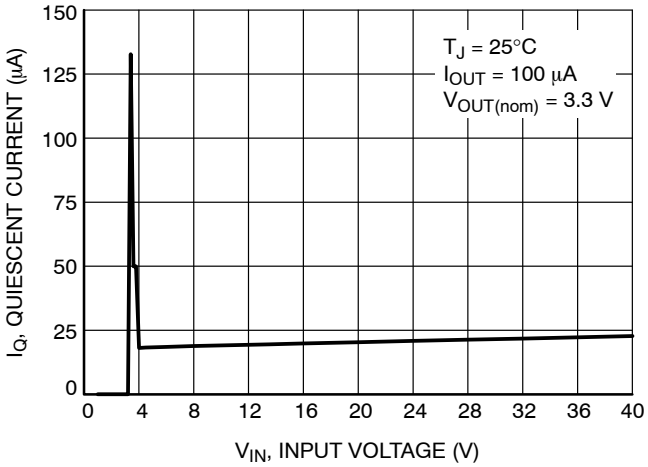


Figure 21. Quiescent Current vs. Input Voltage

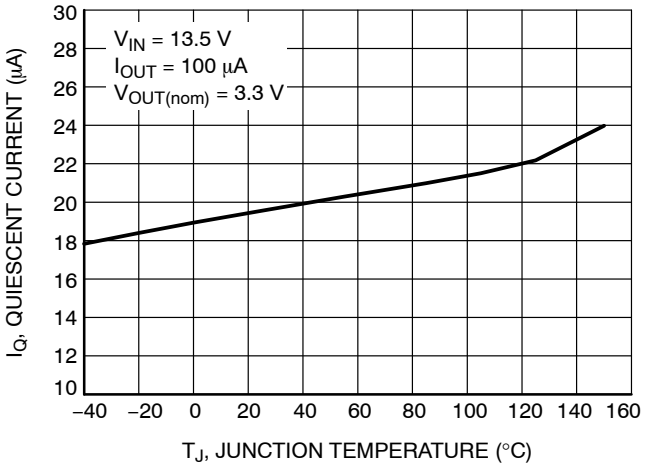


Figure 22. Quiescent Current vs. Junction Temperature

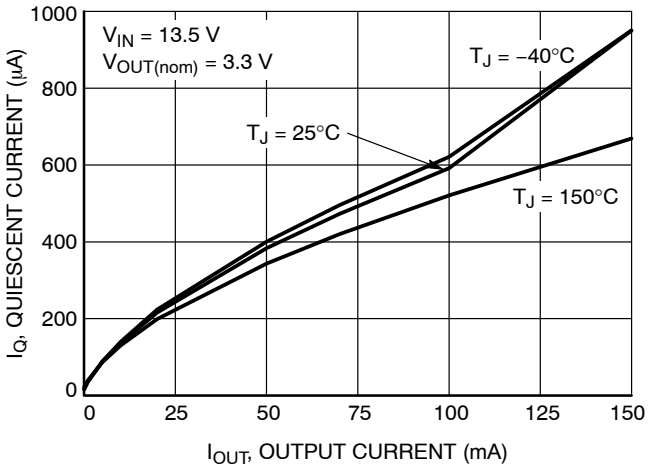


Figure 23. Quiescent Current vs. Output Current

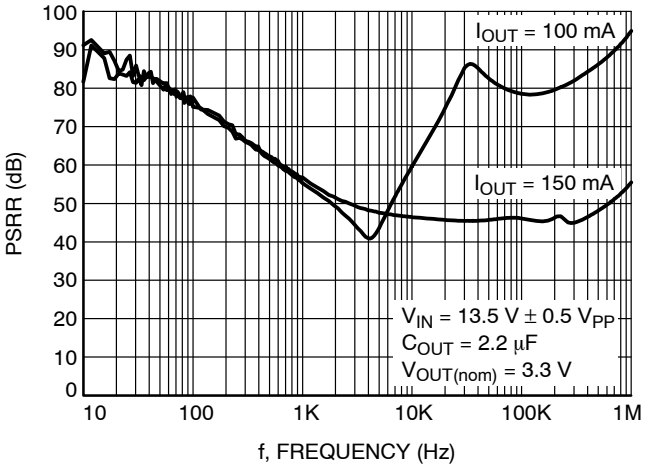


Figure 24. PSRR vs. Frequency

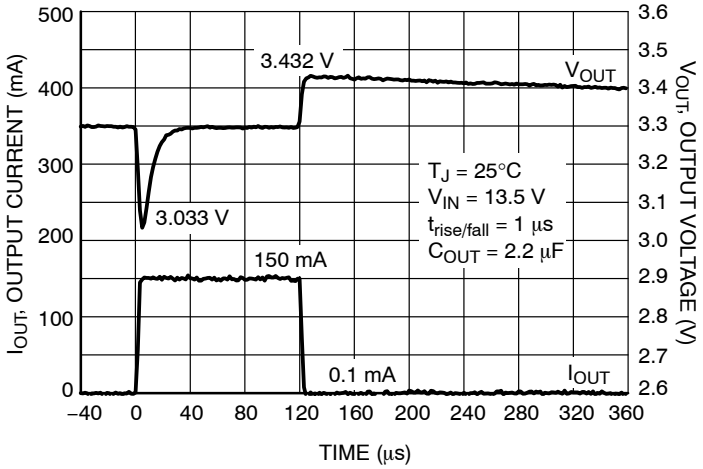


Figure 25. Load Transients

CHARACTERISTICS CURVES – 3.3 V Option

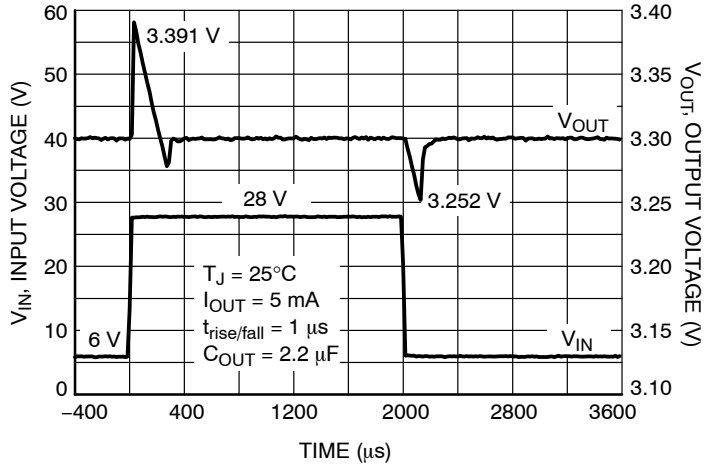


Figure 26. Line Transients

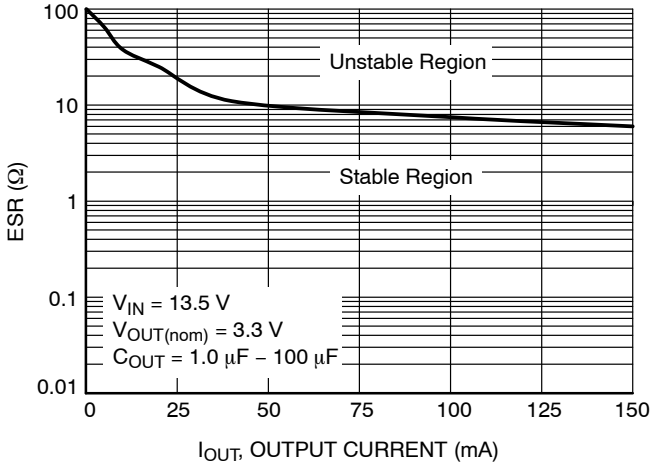


Figure 27. Output Stability with Output Capacitor ESR

DETAILED OPERATING DESCRIPTION

General

The NCV8760C is a 5 V and 3.3 V linear regulator providing low drop−out voltage for 150 mA at low quiescent current levels. Also featured in this part is a reset output with selectable delay times. Delay times are selectable via part selection and control through the Delay Time Select (DT) pin. A ceramic or tantalum 0.1 μF capacitor is recommended and should be connected to V_{IN} to GND close to the NCV8760C package. If extremely fast input voltage transients are expected with slew rate in excess of 4 V/μs then appropriate input filter must be used. Thermal shutdown functionality protects the IC from damage caused from excessively high temperatures appearing on the IC.

Output Voltage

Output voltage stability is determined by the output capacitor selection. The NCV8760C has been designed to work with low ESR (equivalent series resistance) ceramic capacitors. The NCV8760C is stable using any capacitor 1 μF and above with ESR below 5 Ω. Stable region of ESR in Figure 16 shows ESR values at which the LDO output voltage does not have any permanent oscillations at any dynamic changes of output load current. Marginal ESR is the value at which the output voltage waving is fully damped during four periods after the load change and no oscillation is further observable. ESR characteristics were measured with ceramic capacitors and additional series resistors to emulate ESR. Low duty cycle pulse load current technique has been used to maintain junction temperature close to ambient temperature.

Larger values improve noise rejection and load regulation transient response.

Current Limit

Current limit is provided on V_{OUT} to protect the IC. The minimum specification is 205 mA. Current limit is specified under two conditions (V_{OUT} = 96% x V_{OUT_NOM}) and (V_{OUT} = 0 V). No fold−back circuitry exists. Any measured differences can be attributed to change in die temperature. The part may be operated up to 205 mA provided thermal die temperature is considered and is kept below 150°C. A reset (RO) will not occur with a load less than 205 mA.

Reset Output

A reset signal is provided on the Reset Output (RO) pin to provide feedback to the microprocessor of an out of regulation condition. This is in the form of a logic signal on RO. Output (V_{OUT}) voltage conditions below the RESET threshold cause RO to go low. The RO integrity is maintained down to V_{OUT} = 1.0 V.

The NCV8670C contains an internal 30 kΩ pull up resistor. In case of RO function the external pull up resistor is optional to use (Figure 1).

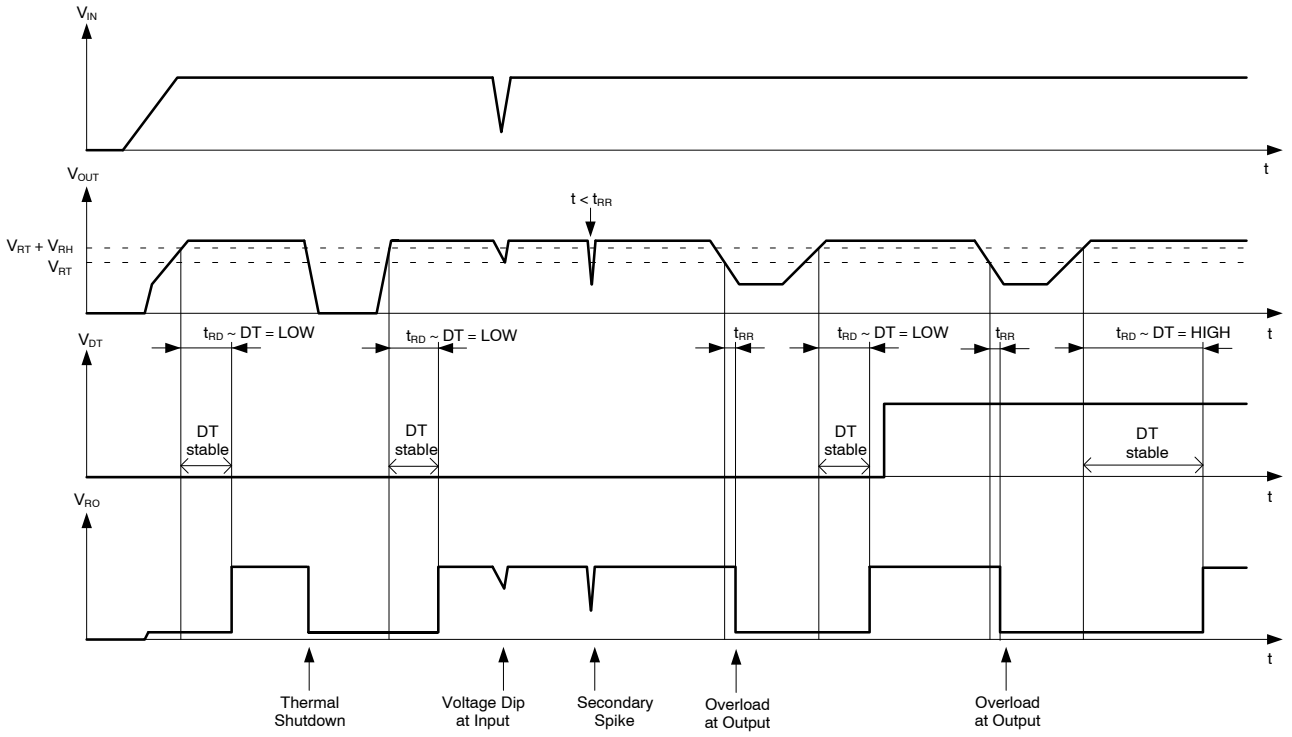


Figure 28. Reset Timing

During power−up (or restoring V_{OUT} voltage from a reset event), the V_{OUT} voltage must be maintained above the Reset threshold for the Reset Delay time before RO goes high. The time for Reset Delay is determined by the choice of IC and the state of the DT pin.

Reset Delay Time Select

Selection of the NCV8760C device and the state of the DT pin determines the available Reset Delay times. The part is designed for use with DT tied to ground or V_{OUT}, but may be controlled by any logic signal which provides a threshold between 0.8 V and 2 V. The default condition for an open DT pin is the faster Reset time (DT = GND condition). Times are in pairs and are highlighted in the table below. Consult factory for availability.

Marking − 760yCxG	DT=GND	DT=OUT
y = Reset Time	Reset Time	Reset Time
1	8 ms	128 ms
2	8 ms	32 ms
3	16 ms	64 ms
4	32 ms	128 ms

NOTE: The timing values can be selected from the following list: 8, 16, 32, 64, 128 ms. Contact factory for options not included in ORDERING INFORMATION table on page 13.

Note the DT pin is sampled within 24 μs period after V_{OUT} rises above V_{RT} + V_{RH} voltage. It is not recommended to change DT logic level during “DT stable” time window. Example of reset delay time selection is shown in Figure 28.

Thermal Shutdown

When the die temperature exceeds the Thermal Shutdown threshold, a Thermal Shutdown event is detected, V_{OUT} is turned off and RO goes low. The IC will remain in this state until the die temperature decreases below the shutdown threshold (175°C typical) minus the hysteresis factor (10°C typical). Then the output turns on and RO goes high after the RESET Delay time.

Hints

V_{IN} and GND printed circuit board traces should be as wide as possible. When the impedance of these traces is high, there is a chance to pick up noise or cause the regulator to malfunction. Place external components, especially the output capacitor, as close as possible to the device to improve EMC performance.

The NCV8760C is not developed in compliance with ISO26262 standard. If application is safety critical then the below application example diagram shown in Figure 29 can be used.

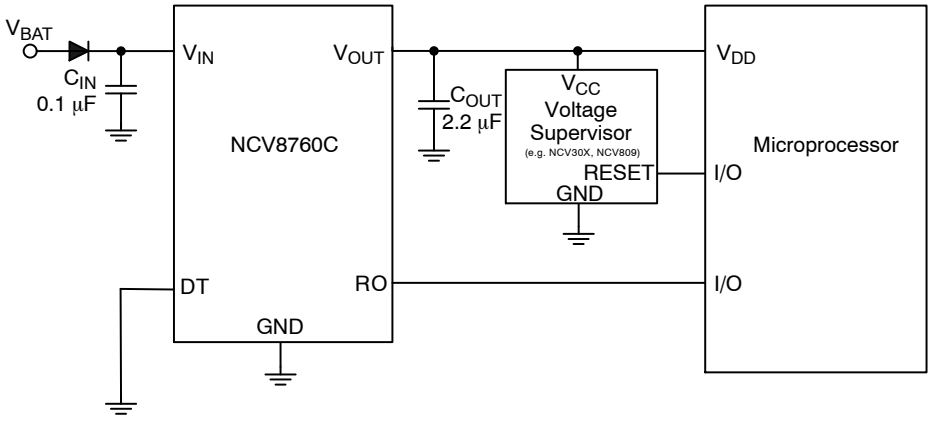


Figure 29. NCV8760C Application Diagram

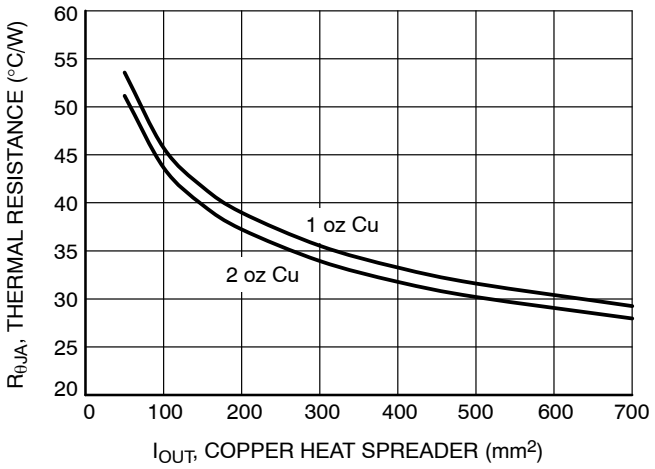


Figure 30. $R_{\theta JA}$ vs. PCB Copper Area (DPAK)

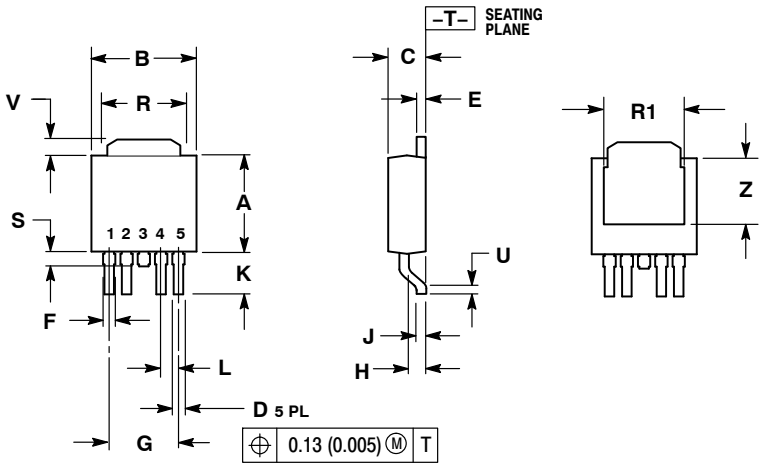
ORDERING INFORMATION

Device	Output Voltage	Reset Delay Time, DT to GND	Reset Delay Time, DT to OUT	Package	Shipping†
NCV8760CDT501RKG	5.0 V	8 ms	128 ms	DPAK (Pb−Free)	2500 / Tape & Reel
NCV8760CDT332RKG	3.3 V	8 ms	32 ms	DPAK (Pb−Free)	2500 / Tape & Reel
NCV8760CDT333RKG		16 ms	64 ms		

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specification Brochure, BRD8011/D.

PACKAGE DIMENSIONS

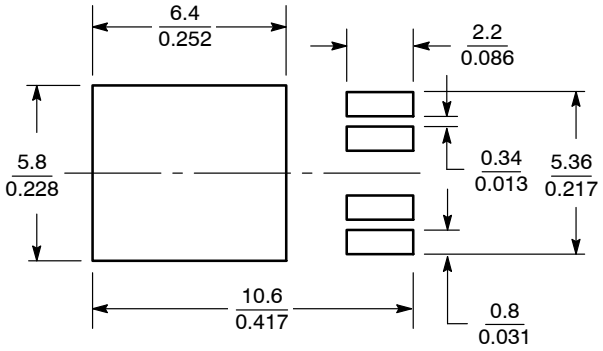
DPAK 5, CENTER LEAD CROP
DT SUFFIX
CASE 175AA
ISSUE B



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	0.235	0.245	5.97	6.22
B	0.250	0.265	6.35	6.73
C	0.086	0.094	2.19	2.38
D	0.020	0.028	0.51	0.71
E	0.018	0.023	0.46	0.58
F	0.024	0.032	0.61	0.81
G	0.180 BSC		4.56 BSC	
H	0.034	0.040	0.87	1.01
J	0.018	0.023	0.46	0.58
K	0.102	0.114	2.60	2.89
L	0.045 BSC		1.14 BSC	
R	0.170	0.190	4.32	4.83
R1	0.185	0.210	4.70	5.33
S	0.025	0.040	0.63	1.01
U	0.020	---	0.51	---
V	0.035	0.050	0.89	1.27
Z	0.155	0.170	3.93	4.32

SOLDERING FOOTPRINT*



SCALE 4:1 (mm / inches)

*For additional information on our Pb–Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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