# MOSFET – Power, N-Channel, DPAK/IPAK

## 9.0 A, 60 V

# NTD3055-150, NVD3055-150

Designed for low voltage, high speed switching applications in power supplies, converters and power motor controls and bridge circuits.

### Features

- NVD Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC-Q101 Qualified and PPAP Capable
- These Devices are Pb-Free and are RoHS Compliant

### Typical Applications

- Power Supplies
- Converters
- Power Motor Controls
- Bridge Circuits

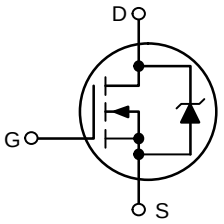
**MAXIMUM RATINGS** ($T_J$ = 25 °C unless otherwise noted)

| Rating | Symbol | Value | Unit |
|---|---|---|---|
| Drain-to-Source Voltage | $V_{DSS}$ | 60 | Vdc |
| Drain-to-Gate Voltage ($R_{GS}$ = 10 MΩ) | $V_{DGR}$ | 60 | Vdc |
| Gate-to-Source Voltage<br>− Continuous<br>− Non-repetitive ($t_p \le 10$ ms) | <br>$V_{GS}$<br>$V_{GS}$ | <br>±20<br>±30 | Vdc |
| Drain Current<br>− Continuous @ $T_A$ = 25 °C<br>− Continuous @ $T_A$ = 100 °C<br>− Single Pulse ($t_p \le 10$ μs) | <br>$I_D$<br>$I_D$<br>$I_{DM}$ | <br>9.0<br>3.0<br>27 | Adc<br><br><br>Apk |
| Total Power Dissipation @ $T_A$ = 25 °C<br>Derate above 25 °C<br>Total Power Dissipation @ $T_A$ = 25 °C (Note 1)<br>Total Power Dissipation @ $T_A$ = 25 °C (Note 2) | $P_D$ | 28.8<br>0.19<br>2.1<br>1.5 | W<br>W/°C<br>W<br>W |
| Operating and Storage Temperature Range | $T_J$, $T_{stg}$ | −55 to 175 | °C |
| Single Pulse Drain-to-Source Avalanche Energy − Starting $T_J$ = 25 °C ($V_{DD}$ = 25 Vdc, $V_{GS}$ = 10 Vdc, L = 1.0 mH, $I_L$(pk) = 7.75 A, $V_{DS}$ = 60 Vdc) | $E_{AS}$ | 30 | mJ |
| Thermal Resistance<br>− Junction-to-Case<br>− Junction-to-Ambient (Note 1)<br>− Junction-to-Ambient (Note 2) | <br>$R_{\theta JC}$<br>$R_{\theta JA}$<br>$R_{\theta JA}$ | <br>5.2<br>71.4<br>100 | °C/W |
| Maximum Lead Temperature for Soldering Purposes, 1/8″ from case for 10 seconds | $T_L$ | 260 | °C |

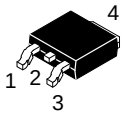
Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. When surface mounted to an FR4 board using 0.5 sq in pad size.
2. When surface mounted to an FR4 board using minimum recommended pad size.

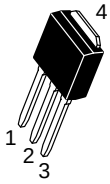
**9.0 AMPERES, 60 VOLTS**
**$R_{DS(on)}$ = 122 mΩ (Typ)**




N-Channel

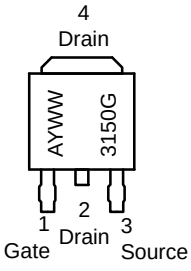


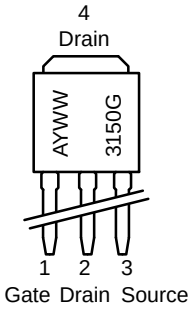

**DPAK**
**CASE 369C**
**(SURFACE MOUNT)**
**STYLE 2**




**IPAK**
**CASE 369D**
**(STRAIGHT LEAD)**
**STYLE 2**

**MARKING DIAGRAMS & PIN ASSIGNMENTS**




| | |
|---|---|
| A | = Assembly Location* |
| 3150 | = Device Code |
| Y | = Year |
| WW | = Work Week |
| G | = Pb-Free Package |

* The Assembly Location code (A) is front side optional. In cases where the Assembly Location is stamped in the package, the front side assembly code may be blank.

### ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 5 of this data sheet.

NOTE: Some of the devices on this data sheet have been **DISCONTINUED**. Please refer to the table on page 5.

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**ELECTRICAL CHARACTERISTICS** ($T_J$ = 25 °C unless otherwise noted)

| Characteristic | | Symbol | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| **OFF CHARACTERISTICS** | | | | | | |
| Drain-to-Source Breakdown Voltage (Note 3)<br>($V_{GS}$ = 0 Vdc, $I_D$ = 250 μAdc)<br>Temperature Coefficient (Positive) | | $V_{(BR)DSS}$ | <br>60<br>– | <br>–<br>70.2 | <br>–<br>– | Vdc<br><br>mV/°C |
| Zero Gate Voltage Drain Current<br>($V_{DS}$ = 60 Vdc, $V_{GS}$ = 0 Vdc)<br>($V_{DS}$ = 60 Vdc, $V_{GS}$ = 0 Vdc, $T_J$ = 150 °C) | | $I_{DSS}$ | <br>–<br>– | <br>–<br>– | <br>1.0<br>10 | μAdc |
| Gate-Body Leakage Current ($V_{GS}$ = ±20 Vdc, $V_{DS}$ = 0 Vdc) | | $I_{GSS}$ | – | – | ±100 | nAdc |
| **ON CHARACTERISTICS** (Note 3) | | | | | | |
| Gate Threshold Voltage (Note 3)<br>($V_{DS}$ = $V_{GS}$, $I_D$ = 250 μAdc)<br>Threshold Temperature Coefficient (Negative) | | $V_{GS(th)}$ | <br>2.0<br>– | <br>3.0<br>6.4 | <br>4.0<br>– | Vdc<br><br>mV/°C |
| Static Drain-to-Source On-Resistance (Note 3)<br>($V_{GS}$ = 10 Vdc, $I_D$ = 4.5 Adc) | | $R_{DS(on)}$ | – | 122 | 150 | mΩ |
| Static Drain-to-Source On-Voltage (Note 3)<br>($V_{GS}$ = 10 Vdc, $I_D$ = 9.0 Adc)<br>($V_{GS}$ = 10 Vdc, $I_D$ = 4.5 Adc, $T_J$ = 150 °C) | | $V_{DS(on)}$ | <br>–<br>– | <br>1.4<br>1.1 | <br>1.9<br>– | Vdc |
| Forward Transconductance (Note 3) ($V_{DS}$ = 7.0 Vdc, $I_D$ = 6.0 Adc) | | $g_{FS}$ | – | 5.4 | – | mhos |
| **DYNAMIC CHARACTERISTICS** | | | | | | |
| Input Capacitance | ($V_{DS}$ = 25 Vdc, $V_{GS}$ = 0 Vdc, f = 1.0 MHz) | $C_{iss}$ | – | 200 | 280 | pF |
| Output Capacitance | | $C_{oss}$ | – | 70 | 100 | |
| Transfer Capacitance | | $C_{rss}$ | – | 26 | 40 | |
| **SWITCHING CHARACTERISTICS** (Note 4) | | | | | | |
| Turn-On Delay Time | ($V_{DD}$ = 48 Vdc, $I_D$ = 9.0 Adc, $V_{GS}$ = 10 Vdc, $R_G$ = 9.1 Ω) (Note 3) | $t_{d(on)}$ | – | 11.2 | 25 | ns |
| Rise Time | | $t_r$ | – | 37.1 | 80 | |
| Turn-Off Delay Time | | $t_{d(off)}$ | – | 12.2 | 25 | |
| Fall Time | | $t_f$ | – | 23 | 50 | |
| Gate Charge | ($V_{DS}$ = 48 Vdc, $I_D$ = 9.0 Adc, $V_{GS}$ = 10 Vdc) (Note 3) | $Q_T$ | – | 7.1 | 15 | nC |
| | | $Q_1$ | – | 1.7 | – | |
| | | $Q_2$ | – | 3.5 | – | |
| **SOURCE-DRAIN DIODE CHARACTERISTICS** | | | | | | |
| Forward On-Voltage | ($I_S$ = 9.0 Adc, $V_{GS}$ = 0 Vdc) (Note 3)<br>($I_S$ = 19 Adc, $V_{GS}$ = 0 Vdc, $T_J$ = 150 °C) | $V_{SD}$ | <br>– | <br>0.98<br>0.86 | <br>1.20<br>– | Vdc |
| Reverse Recovery Time | ($I_S$ = 9.0 Adc, $V_{GS}$ = 0 Vdc, $dI_S/dt$ = 100 A/μs) (Note 3) | $t_{rr}$ | – | 28.9 | – | ns |
| | | $t_a$ | – | 21.6 | – | |
| | | $t_b$ | – | 7.3 | – | |
| Reverse Recovery Stored Charge | | $Q_{RR}$ | – | 0.036 | – | μC |

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

3. Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2%.
4. Switching characteristics are independent of operating junction temperatures.



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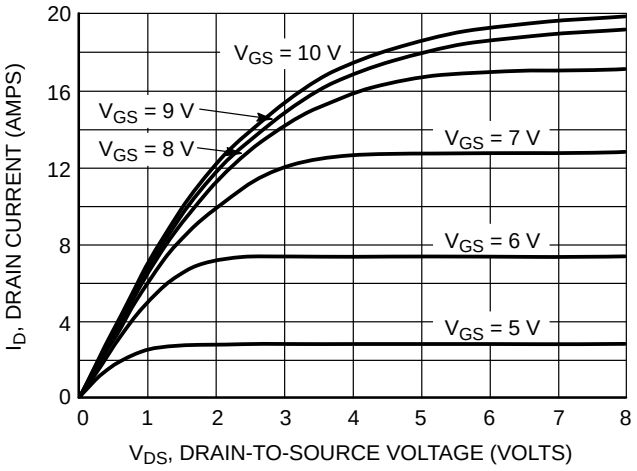



**Figure 1. On-Region Characteristics**

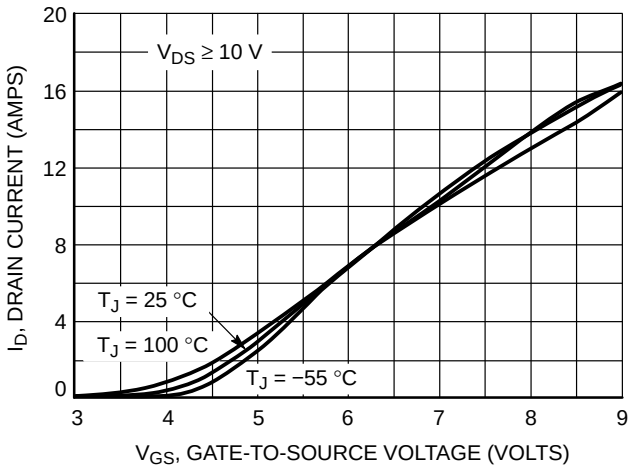



**Figure 2. Transfer Characteristics**

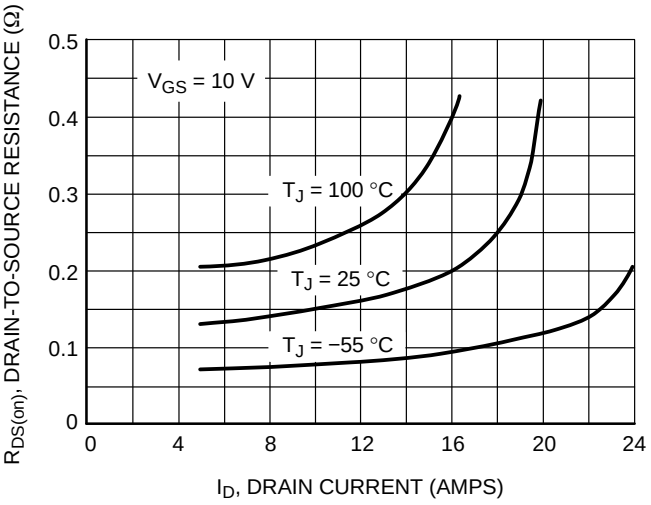



**Figure 3. On-Resistance versus Gate-To-Source Voltage**

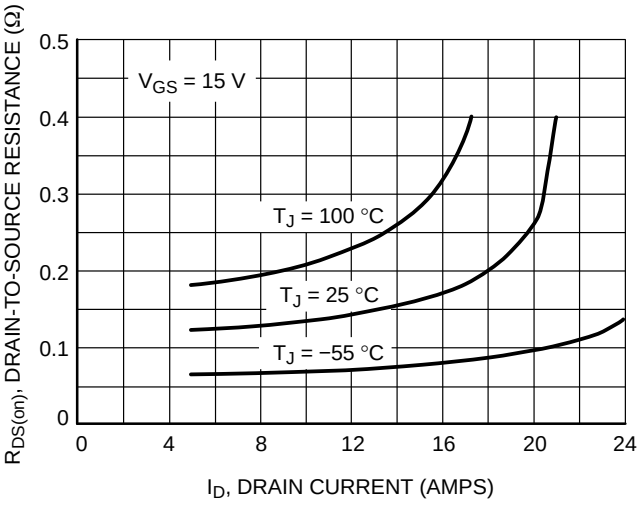



**Figure 4. On-Resistance versus Drain Current and Gate Voltage**

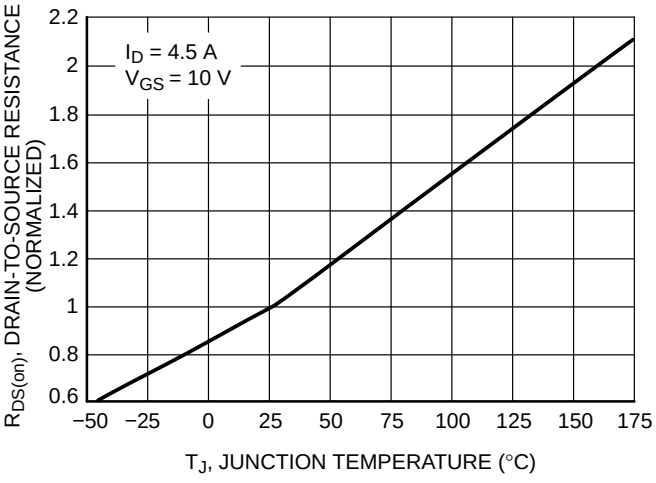



**Figure 5. On-Resistance Variation with Temperature**

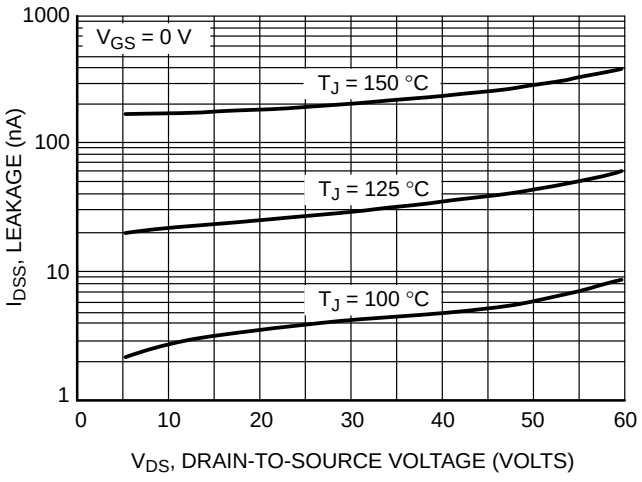



**Figure 6. Drain-To-Source Leakage Current versus Voltage**



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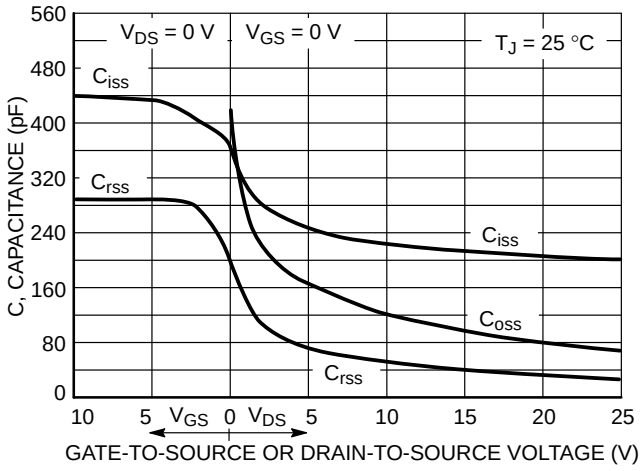



**Figure 7. Capacitance Variation**

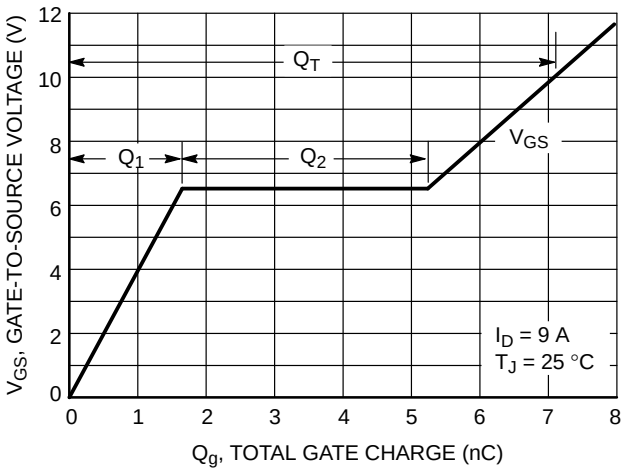



**Figure 8. Gate-to-Source and Drain-to-Source Voltage versus Total Charge**

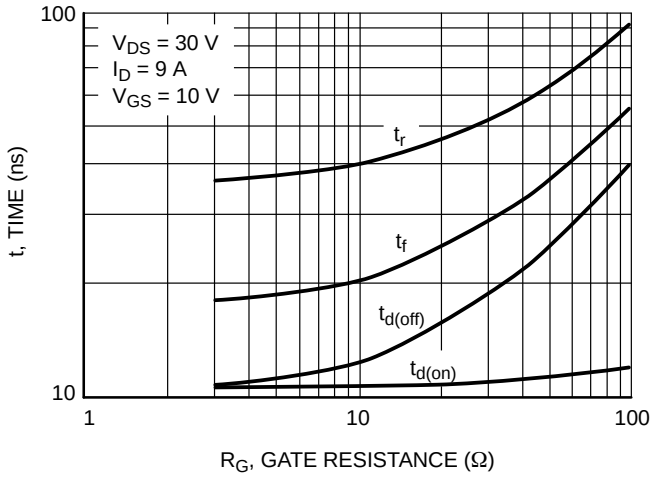



**Figure 9. Resistive Switching Time Variation versus Gate Resistance**

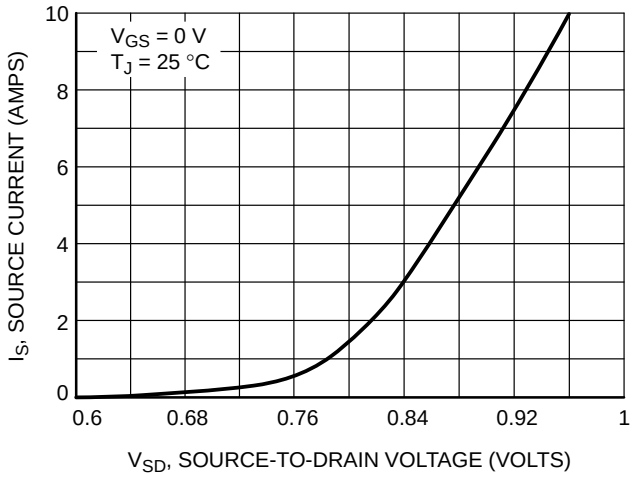



**Figure 10. Diode Forward Voltage versus Current**

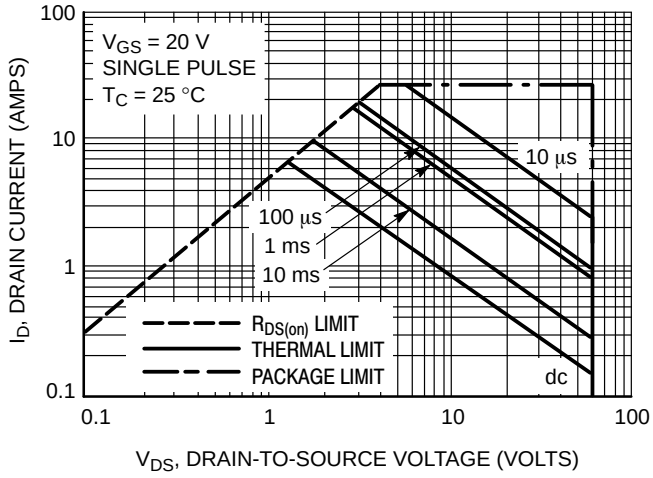



**Figure 11. Maximum Rated Forward Biased Safe Operating Area**

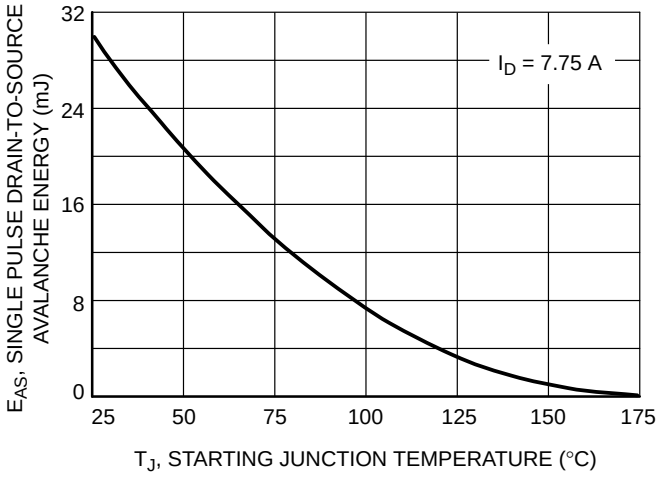



**Figure 12. Maximum Avalanche Energy versus Starting Junction Temperature**



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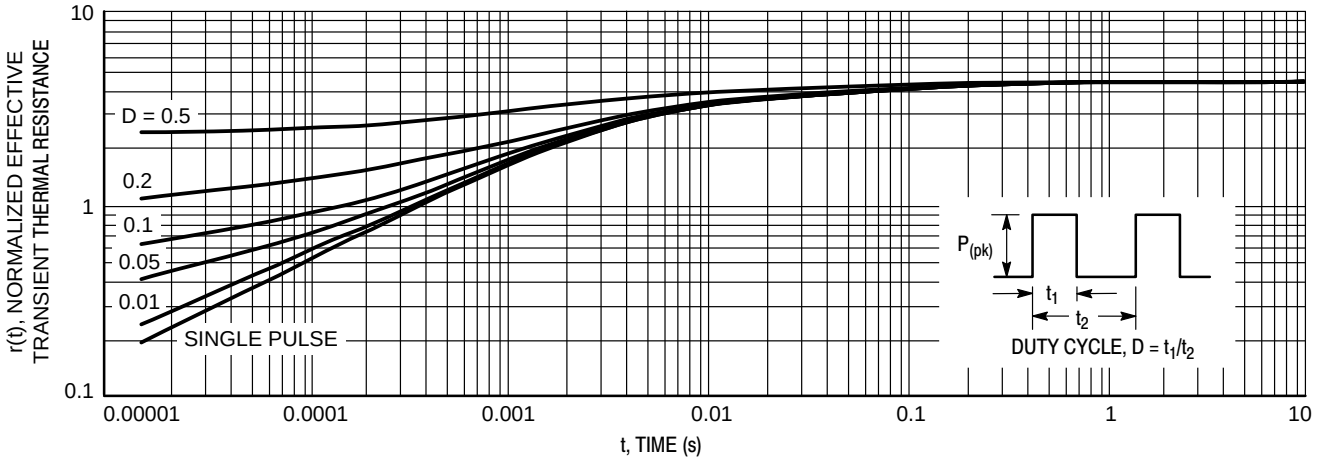



**Figure 13. Thermal Response**

## ORDERING INFORMATION

| Device | Package | Shipping† |
|---|---|---|
| NTD3055-150T4G | DPAK (Pb-Free) | 2500 / Tape & Reel |
| NVD3055-150T4G-VF01 | DPAK (Pb-Free) | 2500 / Tape & Reel |

**DISCONTINUED** (Note 5)

| | | |
|---|---|---|
| NTD3055-150G | DPAK (Pb-Free) | 75 Units / Rail |
| NTD3055-150-1G | IPAK (Pb-Free) | 75 Units / Rail |
| NTD3055-150T4H | DPAK (Halide-Free) | 2500 / Tape & Reel |
| NVD3055-150T4G* | DPAK (Pb-Free) | 2500 / Tape & Reel |

† For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

* NVD Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC-Q101 Qualified and PPAP Capable.

5. **DISCONTINUED:** These devices are not available. Please contact your **onsemi** representative for information. The most current information on these devices may be available on www.onsemi.com.



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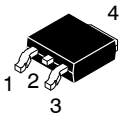
## REVISION HISTORY

| Revision | Description of Changes | Date |
|---|---|---|
| 8 | Rebranded the document to **onsemi** format. NTD3055-150G, NTD3055-150-1G, NTD3055-150T4H, NVD3055-150T4G OPNs marked as Discontinued. | 2/16/2026 |

This document has undergone updates prior to the inclusion of this revision history table. The changes tracked here only reflect updates made on the noted approval dates.



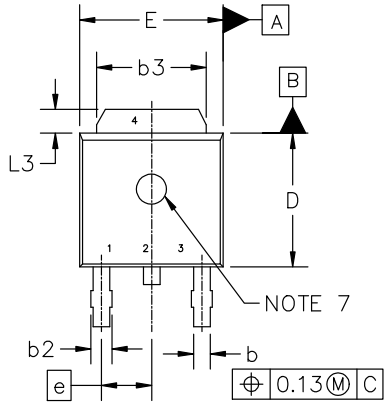
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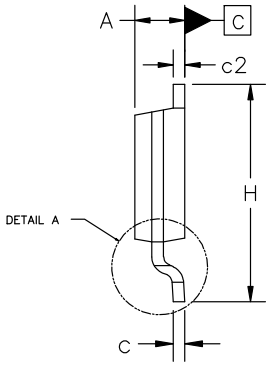

**SCALE 1:1**

**DPAK−3 6.10x6.54x2.28, 2.29P**
CASE 369C
ISSUE L

DATE 24 AUG 2026

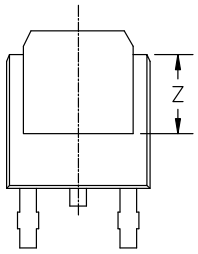



TOP VIEW

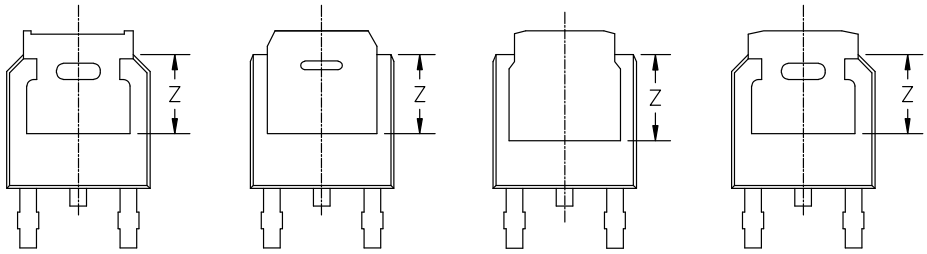



SIDE VIEW

| MILLIMETERS | | | |
|---|---|---|---|
| DIM | MIN | NOM | MAX |
| A | 2.18 | 2.28 | 2.38 |
| A1 | 0.00 | −−− | 0.13 |
| b | 0.63 | 0.76 | 0.89 |
| b2 | 0.72 | 0.93 | 1.14 |
| b3 | 4.57 | 5.02 | 5.46 |
| c | 0.46 | 0.54 | 0.61 |
| c2 | 0.46 | 0.54 | 0.61 |
| D | 5.97 | 6.10 | 6.22 |
| E | 6.35 | 6.54 | 6.73 |
| e | 2.29 BSC | | |
| H | 9.40 | 9.91 | 10.41 |
| L | 1.40 | 1.59 | 1.78 |
| L1 | 2.90 REF | | |
| L2 | 0.51 BSC | | |
| L3 | 0.89 | −−− | 1.27 |
| L4 | −−− | −−− | 1.01 |
| Z | 3.93 | −−− | −−− |



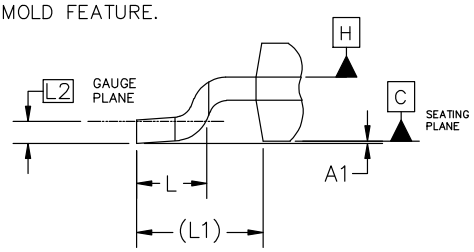

BOTTOM VIEW



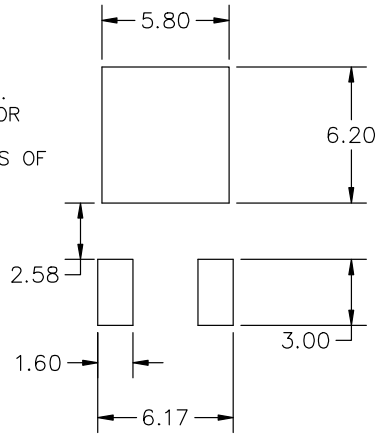

ALTERNATE CONSTRUCTIONS

NOTES:

1. DIMENSIONING AND TOLERANCING ASME Y14.5M, 2018.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. THERMAL PAD CONTOUR OPTIONAL WITHIN DIMENSIONS b3, L3, AND Z.
4. DIMENSIONS D AND E DO NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR BURRS.
5. DIMENSIONS D AND E ARE DETERMINED AT THE OUTERMOST EXTREMES OF THE PLASTIC BODY.
6. DATUMS A AND B ARE DETERMINED AT DATUM PLANE H.
7. OPTIONAL MOLD FEATURE.




DETAIL A
ROTATED 90° CW




RECOMMENDED MOUNTING FOOTPRINT*
*For additional information on our Pb−Free strategy and soldering details, please download the onsemi Soldering and Mounting Techniques reference manual, SOLDERRM/D.

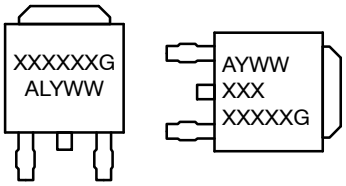
| | | |
|---|---|---|
| **DOCUMENT NUMBER:** | **98AON10527D** | Electronic versions are uncontrolled except when accessed directly from the Document Repository. Printed versions are uncontrolled except when stamped "CONTROLLED COPY" in red. |
| **DESCRIPTION:** | **DPAK−3 6.10x6.54x2.28, 2.29P** | **PAGE 1 OF 2** |

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**DPAK−3 6.10x6.54x2.28, 2.29P**
CASE 369C
ISSUE L

DATE 24 AUG 2026

## GENERIC MARKING DIAGRAM*




**IC** **Discrete**

| | |
|---|---|
| XXXXXX | = Device Code |
| A | = Assembly Location |
| L | = Wafer Lot |
| Y | = Year |
| WW | = Work Week |
| G | = Pb−Free Package |

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, “G” or microdot “▪”, may or may not be present. Some products may not follow the Generic Marking.

STYLE 1:
PIN 1. BASE
2. COLLECTOR
3. EMITTER
4. COLLECTOR

STYLE 2:
PIN 1. GATE
2. DRAIN
3. SOURCE
4. DRAIN

STYLE 3:
PIN 1. ANODE
2. CATHODE
3. ANODE
4. CATHODE

STYLE 4:
PIN 1. CATHODE
2. ANODE
3. GATE
4. ANODE

STYLE 5:
PIN 1. GATE
2. ANODE
3. CATHODE
4. ANODE

STYLE 6:
PIN 1. MT1
2. MT2
3. GATE
4. MT2

STYLE 7:
PIN 1. GATE
2. COLLECTOR
3. EMITTER
4. COLLECTOR

STYLE 8:
PIN 1. N/C
2. CATHODE
3. ANODE
4. CATHODE

STYLE 9:
PIN 1. ANODE
2. CATHODE
3. RESISTOR ADJUST
4. CATHODE

STYLE 10:
PIN 1. CATHODE
2. ANODE
3. CATHODE
4. ANODE




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