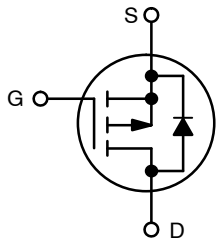
MOSFET - Power, P-Channel, SOT-223

-10 A, -20 V

NTF6P02, NVF6P02

-10 AMPERES
-20 VOLTS
$R_{DS(on)}$ = 44 mΩ (Typ.)



P−Channel MOSFET

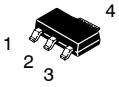
Features

- Low $R_{DS(on)}$
- Logic Level Gate Drive
- Diode Exhibits High Speed, Soft Recovery
- Avalanche Energy Specified
- NVF Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC-Q101 Qualified and PPAP Capable*
- These Devices are Pb-Free and are RoHS Compliant

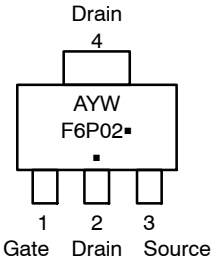
Typical Applications

- Power Management in Portables and Battery-Powered Products, i.e.: Cellular and Cordless Telephones and PCMCIA Cards

MARKING DIAGRAM & PIN ASSIGNMENT



SOT-223
CASE 318E
STYLE 3



A = Assembly Location
Y = Year
W = Work Week
F6P02 = Specific Device Code
▪ = Pb-Free Package

(Note: Microdot may be in either location)

MAXIMUM RATINGS (T_J = 25 °C unless otherwise noted)

Rating	Symbol	Value	Unit
Drain-to-Source Voltage	V_{DSS}	−20	Vdc
Gate-to-Source Voltage	V_{GS}	±8.0	Vdc
Drain Current (Note 1) – Continuous @ T_A = 25 °C – Continuous @ T_A = 70 °C – Single Pulse (t_p = 10 μs)	 I_D I_D I_{DM}	 −10 −8.4 −35	 Adc Apk
Total Power Dissipation @ T_A = 25 °C	P_D	8.3	W
Operating and Storage Temperature Range	T_J, T_{stg}	−55 to +150	°C
Single Pulse Drain-to-Source Avalanche Energy – Starting T_J = 25 °C (V_{DD} = −20 Vdc, V_{GS} = −5.0 Vdc, $I_{L(pk)}$ = −10 A, L = 3.0 mH, R_G = 25Ω)	E_{AS}	150	mJ
Thermal Resistance – Junction to Lead (Note 1) – Junction to Ambient (Note 2) – Junction to Ambient (Note 3)	 $R_{θJL}$ $R_{θJA}$ $R_{θJA}$	 15 71.4 160	°C/W
Maximum Lead Temperature for Soldering Purposes, 1/8″ from case for 10 seconds	T_L	260	°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. Steady State.
2. When surface mounted to an FR4 board using 1” pad size, (Cu. Area 1.127 sq in), Steady State.
3. When surface mounted to an FR4 board using minimum recommended pad size, (Cu. Area 0.412 sq in), Steady State.

ORDERING INFORMATION

Device	Package	Shipping†
NTF6P02T3G	SOT-223 (Pb-Free)	4000 / Tape & Reel
NVF6P02T3G*	SOT-223 (Pb-Free)	4000 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specification Brochure, BRD8011/D.

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ELECTRICAL CHARACTERISTICS (T_J = 25 °C unless otherwise noted)

Characteristic		Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS						
Drain-to-Source Breakdown Voltage (Note 4) (V_{GS} = 0 Vdc, I_D = −250 μAdc) Temperature Coefficient (Positive)		$V_{(BR)DSS}$	−20 –	−25 −11	– –	Vdc mV/°C
Zero Gate Voltage Drain Current (V_{DS} = −20 Vdc, V_{GS} = 0 Vdc) (V_{DS} = −20 Vdc, V_{GS} = 0 Vdc, T_J = 125 °C)		I_{DSS}	– –	– –	−1.0 −10	μAdc
Gate-Body Leakage Current (V_{GS} = ±8.0 Vdc, V_{DS} = 0 Vdc)		I_{GSS}	–	–	±100	nAdc
ON CHARACTERISTICS (Note 4)						
Gate Threshold Voltage (Note 4) (V_{DS} = V_{GS}, I_D = −250 μAdc) Threshold Temperature Coefficient (Negative)		$V_{GS(th)}$	−0.4 –	−0.7 2.6	−1.0 –	Vdc mV/°C
Static Drain-to-Source On-Resistance (Note 4) (V_{GS} = −4.5 Vdc, I_D = −6.0 Adc) (V_{GS} = −2.5 Vdc, I_D = −4.0 Adc) (V_{GS} = −2.5 Vdc, I_D = −3.0 Adc)		$R_{DS(on)}$	– – –	44 57 57	50 70 –	mΩ
Forward Transconductance (Note 4) (V_{DS} = −10 Vdc, I_D = −6.0 Adc)		g_{fs}	–	12	–	Mhos
DYNAMIC CHARACTERISTICS						
Input Capacitance	(V_{DS} = −16 Vdc, V_{GS} = 0 V, f = 1.0 MHz)	C_{iss}	–	900	1200	pF
Output Capacitance		C_{oss}	–	350	500	
Transfer Capacitance		C_{rss}	–	90	150	
Input Capacitance	(V_{DS} = −10 Vdc, V_{GS} = 0 V, f = 1.0 MHz)	C_{iss}	–	940	–	pF
Output Capacitance		C_{oss}	–	410	–	
Transfer Capacitance		C_{rss}	–	110	–	
SWITCHING CHARACTERISTICS (Note 5)						
Turn-On Delay Time	(V_{DD} = −5.0 Vdc, I_D = −1.0 Adc, V_{GS} = −4.5 Vdc, R_G = 6.0 Ω)	$t_{d(on)}$	–	7.0	12	ns
Rise Time		t_r	–	25	45	
Turn-Off Delay Time		$t_{d(off)}$	–	75	125	
Fall Time		t_f	–	50	85	
Turn-On Delay Time	(V_{DD} = −16 Vdc, I_D = −6.0 Adc, V_{GS} = −4.5 Vdc, R_G = 2.5 Ω)	$t_{d(on)}$	–	8.0	–	ns
Rise Time		t_r	–	30	–	
Turn-Off Delay Time		$t_{d(off)}$	–	60	–	
Fall Time		t_f	–	60	–	
Gate Charge	(V_{DS} = −16 Vdc, I_D = −6.0 Adc, V_{GS} = −4.5 Vdc) (Note 4)	Q_T	–	15	20	nC
		Q_{gs}	–	1.7	–	
		Q_{gd}	–	6.0	–	
SOURCE-DRAIN DIODE CHARACTERISTICS						
Forward On-Voltage	(I_S = −3.0 Adc, V_{GS} = 0 Vdc) (Note 4) (I_S = −2.1 Adc, V_{GS} = 0 Vdc) (I_S = −3.0 Adc, V_{GS} = 0 Vdc, T_J = 125 °C)	V_{SD}	– – –	−0.82 −0.74 −0.68	−1.2 – –	Vdc

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ELECTRICAL CHARACTERISTICS (T_J = 25 °C unless otherwise noted)

Characteristic		Symbol	Min	Typ	Max	Unit
SOURCE-DRAIN DIODE CHARACTERISTICS						
Reverse Recovery Time	(I_S = −3.0 Adc, V_{GS} = 0 Vdc, dI_S/dt = 100 A/μs) (Note 4)	t_{rr}	–	42	–	ns
		t_a	–	17	–	
		t_b	–	25	–	
Reverse Recovery Stored Charge		Q_{RR}	–	0.036	–	μC

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

4. Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2.0%.
5. Switching characteristics are independent of operating junction temperatures.

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TYPICAL ELECTRICAL CHARACTERISTICS

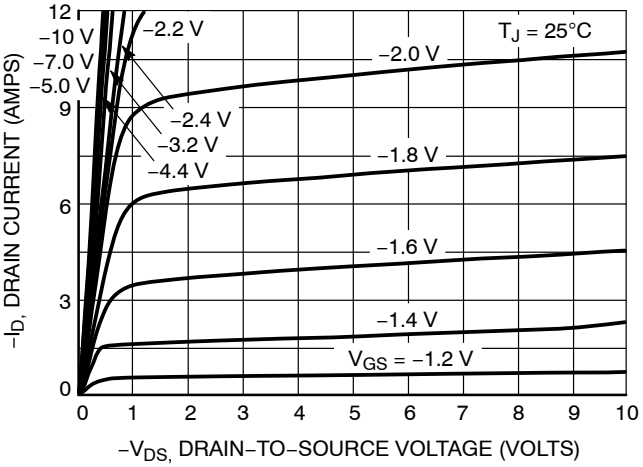


Figure 1. On−Region Characteristics

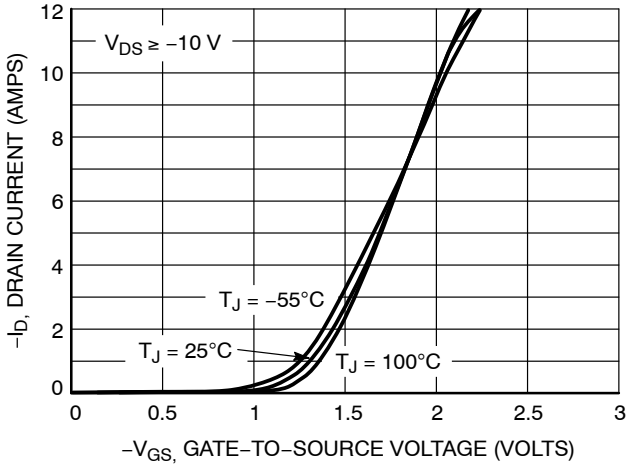


Figure 2. Transfer Characteristics

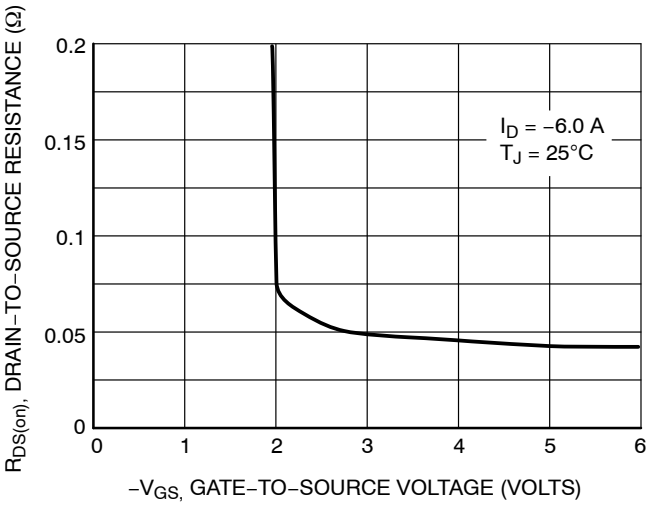


Figure 3. On−Resistance versus Gate−to−Source Voltage

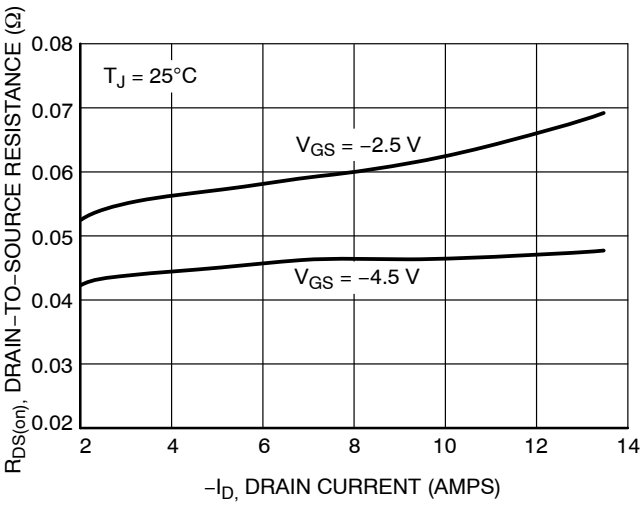


Figure 4. On−Resistance versus Drain Current and Gate Voltage

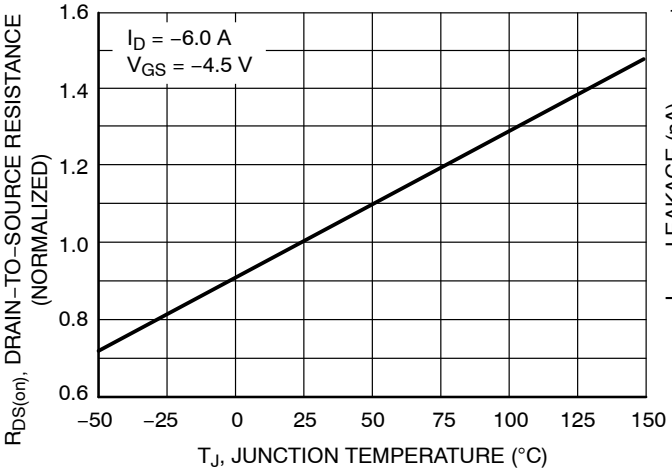


Figure 5. On−Resistance Variation with Temperature

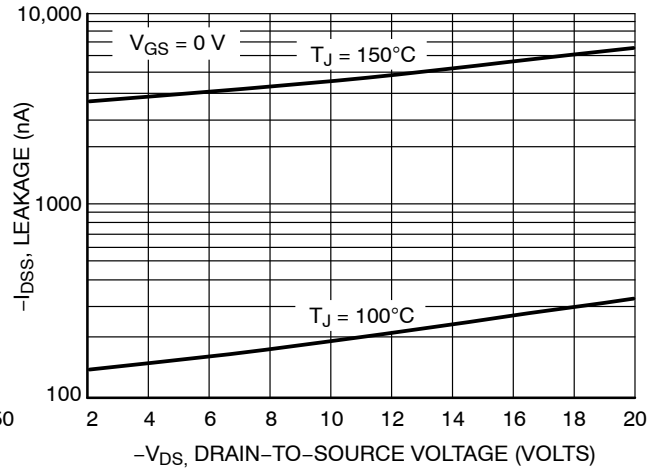


Figure 6. Drain−to−Source Leakage Current versus Voltage

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TYPICAL ELECTRICAL CHARACTERISTICS

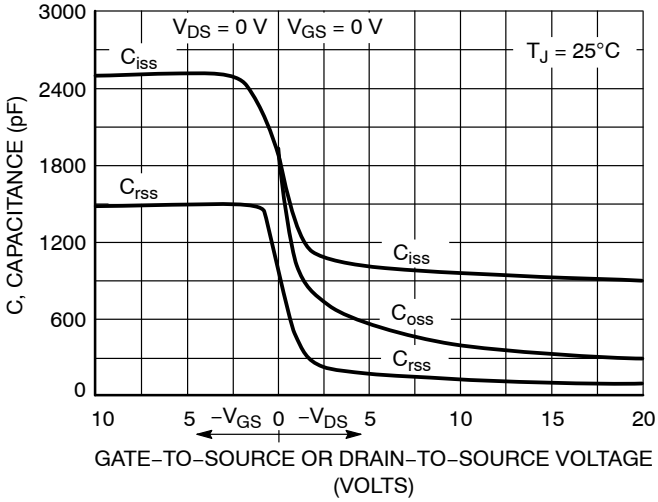


Figure 7. Capacitance Variation

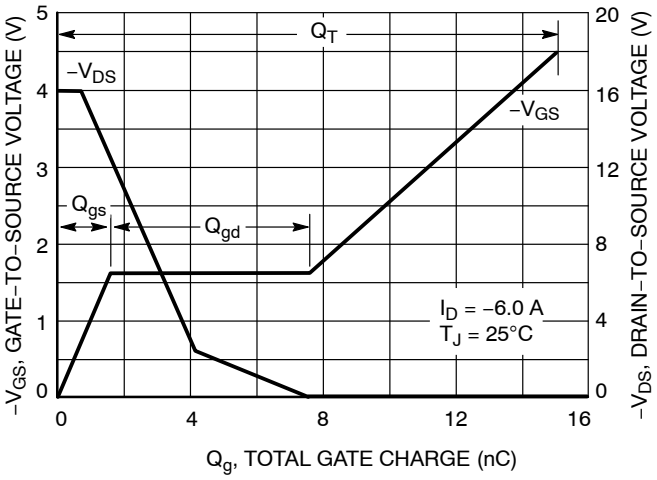


Figure 8. Gate−to−Source and Drain−to−Source Voltage versus Total Charge

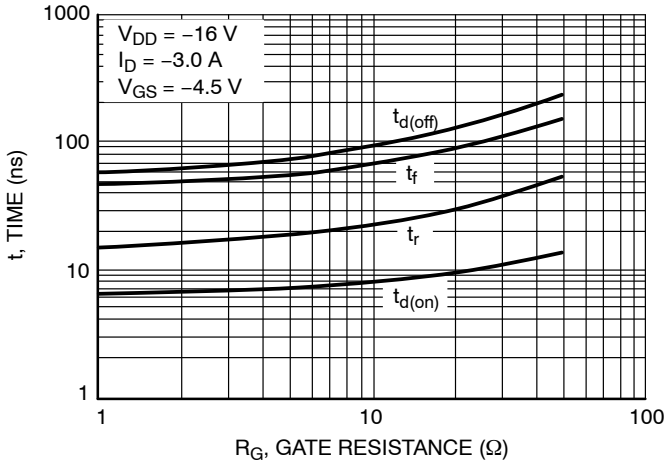


Figure 9. Resistive Switching Time Variation versus Gate Resistance

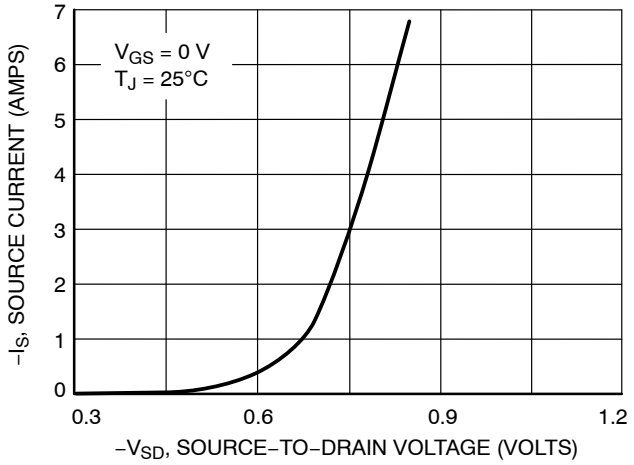


Figure 10. Diode Forward Voltage versus Current

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TYPICAL ELECTRICAL CHARACTERISTICS

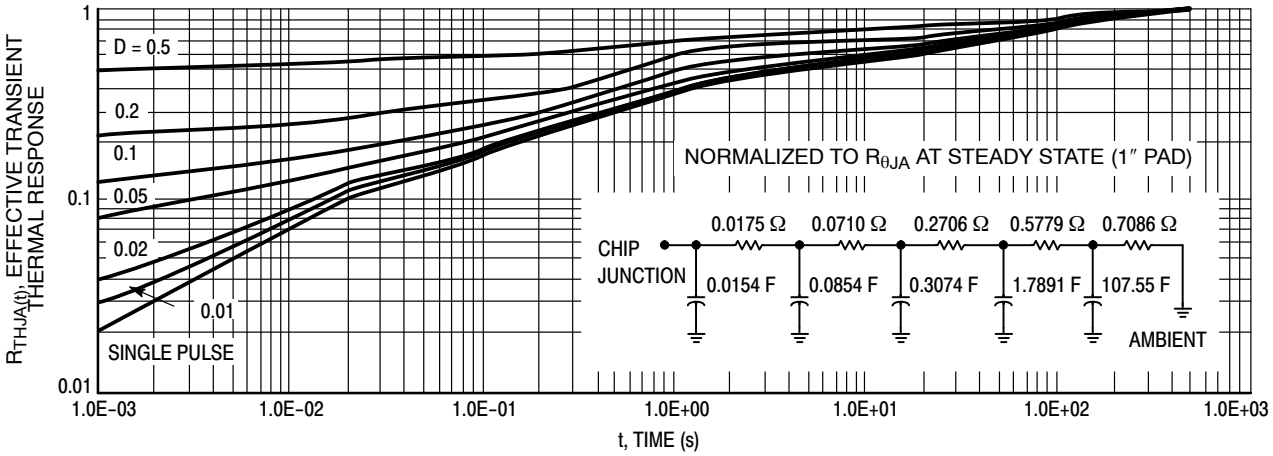


Figure 11. FET Thermal Response

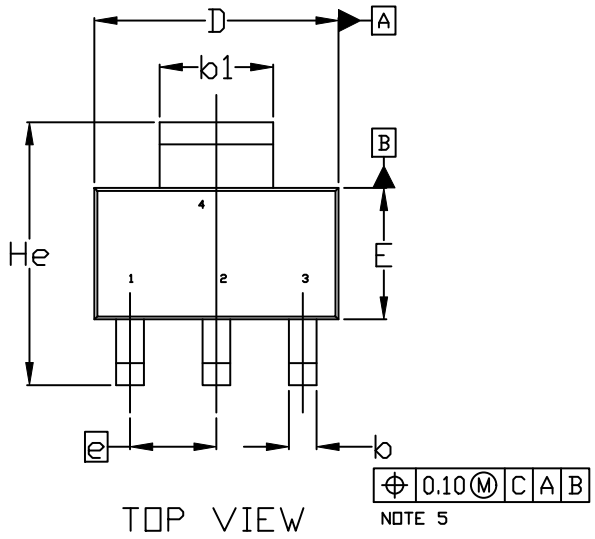
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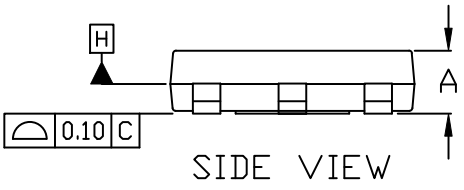


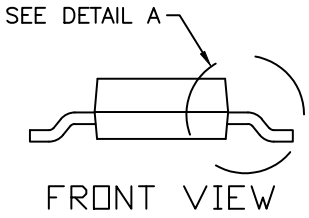
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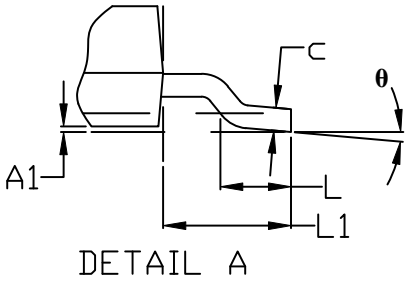
SOT−223 (TO−261)
CASE 318E−04
ISSUE R

DATE 02 OCT 2018



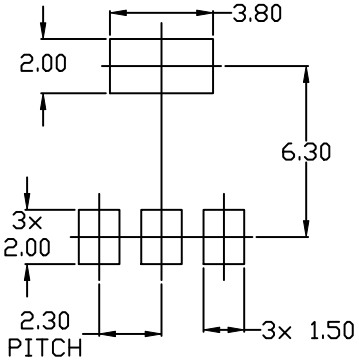






NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS
3. DIMENSIONS D & E DO NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH, PROTRUSIONS OR GATE BURRS SHALL NOT EXCEED 0.200MM PER SIDE.
4. DATUMS A AND B ARE DETERMINED AT DATUM H.
5. A1 IS DEFINED AS THE VERTICAL DISTANCE FROM THE SEATING PLANE TO THE LOWEST POINT OF THE PACKAGE BODY.
6. POSITIONAL TOLERANCE APPLIES TO DIMENSIONS b AND b1.

	MILLIMETERS		
DIM	MIN.	NOM.	MAX.
A	1.50	1.63	1.75
A1	0.02	0.06	0.10
b	0.60	0.75	0.89
b1	2.90	3.06	3.20
c	0.24	0.29	0.35
D	6.30	6.50	6.70
E	3.30	3.50	3.70
e	2.30 BSC		
L	0.20	---	---
L1	1.50	1.75	2.00
He	6.70	7.00	7.30
θ	0°	---	10°



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SOT−223 (TO−261)
CASE 318E−04
ISSUE R

DATE 02 OCT 2018

STYLE 1:
PIN 1. BASE
2. COLLECTOR
3. EMITTER
4. COLLECTOR

STYLE 2:
PIN 1. ANODE
2. CATHODE
3. NC
4. CATHODE

STYLE 3:
PIN 1. GATE
2. DRAIN
3. SOURCE
4. DRAIN

STYLE 4:
PIN 1. SOURCE
2. DRAIN
3. GATE
4. DRAIN

STYLE 5:
PIN 1. DRAIN
2. GATE
3. SOURCE
4. GATE

STYLE 6:
PIN 1. RETURN
2. INPUT
3. OUTPUT
4. INPUT

STYLE 7:
PIN 1. ANODE 1
2. CATHODE
3. ANODE 2
4. CATHODE

STYLE 8:
CANCELLED

STYLE 9:
PIN 1. INPUT
2. GROUND
3. LOGIC
4. GROUND

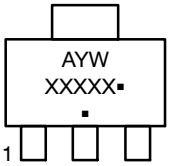
STYLE 10:
PIN 1. CATHODE
2. ANODE
3. GATE
4. ANODE

STYLE 11:
PIN 1. MT 1
2. MT 2
3. GATE
4. MT 2

STYLE 12:
PIN 1. INPUT
2. OUTPUT
3. NC
4. OUTPUT

STYLE 13:
PIN 1. GATE
2. COLLECTOR
3. EMITTER
4. COLLECTOR

GENERIC MARKING DIAGRAM*



A = Assembly Location
Y = Year
W = Work Week
XXXXX = Specific Device Code
▪ = Pb−Free Package

(Note: Microdot may be in either location)

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, “G” or microdot “▪”, may or may not be present. Some products may not follow the Generic Marking.

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