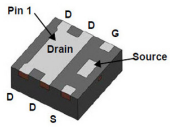
MOSFET – Power, Single P-Channel, WDFN6

-30 V

Preliminary Document

NTLJS17D0P03P8Z

$V_{(BR)DSS}$	$R_{DS(on)}$ MAX	I_D MAX
−30 V	11.3 mΩ @ −10 V	−11.7 A
	21.3 mΩ @ −4.5 V	



WDFN6 (2.05x2.05)
CASE 483AV

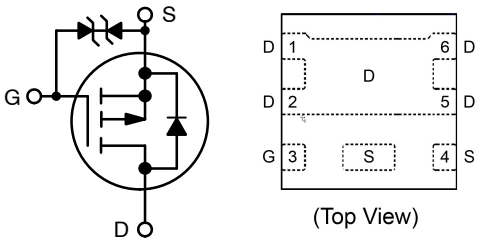
Features

- Small Footprint (4 mm^2) for Compact Design
- Low $R_{DS(on)}$ to Minimize Conduction Losses
- These Devices are Pb-Free, Halogen-Free/BFR-Free and are RoHS Compliant

Applications

- Battery Management
- Protection
- Power Load Switch

ELECTRICAL CONNECTION



P−CHANNEL MOSFET

(Top View)

MARKING DIAGRAM



YW = Date Code
ZZ = Assembly Lot Code
A = Assembly Site Code
17D = Specific Device Code

ORDERING INFORMATION

See detailed ordering, marking and shipping information in the package dimensions section on page 4 of this data sheet.

MAXIMUM RATINGS (T_J = 25 °C unless otherwise noted)

Symbol	Parameter			Value	Unit
V_{DSS}	Drain-to-Source Voltage			−30	V
V_{GS}	Gate-to−Source Voltage			±25	V
I_D	Continuous Drain Current $R_{\theta JA}$ (Notes 1, 3)	Steady State	T_A = 25 °C	−11.7	A
			T_A = 85 °C	−8.4	
P_D	Power Dissipation $R_{\theta JA}$ (Notes 1, 3)		T_A = 25 °C	2.40	W
I_D	Continuous Drain Current $R_{\theta JA}$ (Notes 2, 3)	Steady State	T_A = 25 °C	−7.0	A
			T_A = 85 °C	−5.1	
P_D	Power Dissipation $R_{\theta JA}$ (Notes 2, 3)		T_A = 25 °C	0.86	W
I_{DM}	Pulsed Drain Current	T_A = 25 °C, t_p = 10 μs		47	A
T_J, T_{stg}	Operating Junction and Storage Temperature			−55 to +150	°C
T_L	Lead Temperature for Soldering Purposes (1/8″ from case for 10 s)			260	°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

THERMAL RESISTANCE MAXIMUM RATINGS (Note 1)

Symbol	Parameter	Value	Unit
$R_{\theta JA}$	Junction-to-Ambient - Steady State (Note 1)	52	°C/W
$R_{\theta JA}$	Junction-to-Ambient - Steady State (Note 2)	145	

1. Surface-mounted on FR4 board using 1 in^2 pad size, 2 oz. Cu pad.
2. Surface-mounted on FR4 board using minimum pad size, 2 oz. Cu pad.
3. The entire application environment impacts the thermal resistance values shown, they are not constants and are only valid for the particular conditions noted. Actual continuous current will be limited by thermal & electro-mechanical application board design. $R_{\theta CA}$ is determined by the user's board design.

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ELECTRICAL CHARACTERISTICS (T_J = 25 °C unless otherwise noted)

Symbol	Parameter	Test Condition		Min	Typ	Max	Unit
OFF CHARACTERISTICS							
$V_{(BR)DSS}$	Drain-to-Source Breakdown Voltage	V_{GS} = 0 V, I_D = −250 μA		−30	–	–	V
$V_{(BR)DSS}/T_J$	Drain-to-Source Breakdown Voltage Temperature Coefficient	I_D = −250 μA, ref to 25 °C		–	12.7	–	mV/°C
I_{DSS}	Zero Gate Voltage Drain Current	V_{GS} = 0 V, V_{DS} = −24 V	T_J = 25 °C	–	–	−1	μA
			T_J = 125 °C	–	–	−10	
I_{GSS}	Gate-to-Source Leakage Current	V_{DS} = 0 V, V_{GS} = ±25 V		–	–	±10	μA
ON CHARACTERISTICS (Note 4)							
$V_{GS(TH)}$	Gate Threshold Voltage	V_{GS} = V_{DS}, I_D = −250 μA		−1.0	–	−3.0	V
V_{GS}/T_J	Threshold Temperature Coefficient	I_D = −250 μA, ref to 25 °C		–	−5.9	–	mV/°C
$R_{DS(on)}$	Drain-to-Source On Resistance	V_{GS} = −10 V, I_D = −10 A		–	8.6	11.3	mΩ
		V_{GS} = −4.5 V, I_D = −10 A		–	14.3	21.3	
g_{FS}	Forward Transconductance	V_{DS} = −5 V, I_D = −10 A		–	34	–	S
CHARGES AND CAPACITANCES							
C_{iss}	Input Capacitance	V_{GS} = 0 V, V_{DS} = −15 V, f = 1.0 MHz		–	1600	–	pF
C_{oss}	Output Capacitance			–	550	–	
C_{rss}	Reverse Transfer Capacitance			–	530	–	
$Q_{G(TOT)}$	Total Gate Charge	V_{GS} = −4.5 V, V_{DS} = −15 V, I_D = −10 A		–	23	–	nC
$Q_{G(TH)}$	Threshold Gate Charge			–	3.0	–	nC
Q_{GS}	Gate-to-Source Charge			–	4.6	–	
Q_{GD}	Gate-to-Drain Charge			–	14.2	–	
$Q_{G(TOT)}$	Total Gate Charge	V_{GS} = −10 V, V_{DS} = −15 V, I_D = −10 A		–	38	–	nC
SWITCHING CHARACTERISTICS, V_{GS} = 4.5 V (Note 5)							
$t_{d(on)}$	Turn-On Delay Time	V_{GS} = −4.5 V, V_{DD} = −15 V, I_D = −10 A, R_G = 6 Ω		–	18	–	ns
t_r	Rise Time			–	106	–	
$t_{d(off)}$	Turn-Off Delay Time			–	40	–	
t_f	Fall Time			–	72	–	
SWITCHING CHARACTERISTICS, V_{GS} = 10 V (Note 5)							
$t_{d(on)}$	Turn-On Delay Time	V_{GS} = −10 V, V_{DD} = −15 V, I_D = −10 A, R_G = 6 Ω		–	9	–	ns
t_r	Rise Time			–	18	–	
$t_{d(off)}$	Turn-Off Delay Time			–	85	–	
t_f	Fall Time			–	70	–	
DRAIN-SOURCE DIODE CHARACTERISTICS							
V_{SD}	Forward Diode Voltage	V_{GS} = 0 V, I_S = −10 A	T_J = 25 °C	–	0.83	1.3	V
			T_J = 125 °C	–	0.7	–	
t_{RR}	Reverse Recovery Time	V_{GS} = 0 V, dI_S/dt = −100 A/μs, I_S = −10 A		–	32	–	ns
Q_{RR}	Reverse Recovery Charge			–	10	–	nC

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

4. Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2%.
5. Switching characteristics are independent of operating junction temperatures.

TYPICAL CHARACTERISTICS

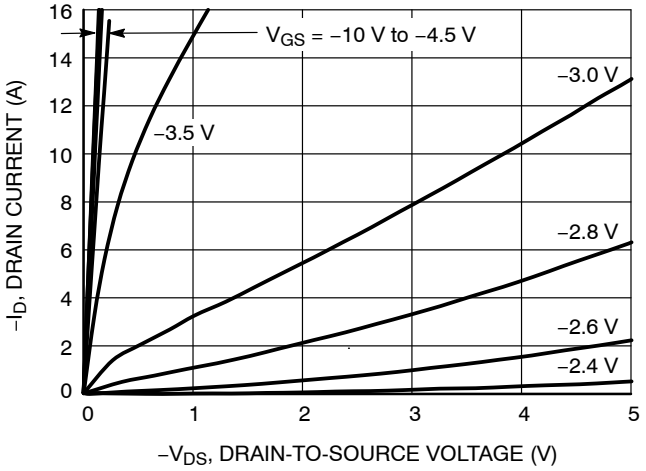


Figure 1. On-Region Characteristics

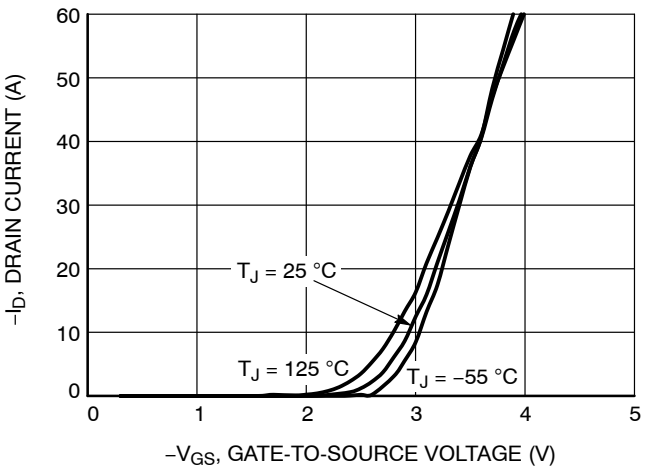


Figure 2. Transfer Characteristics

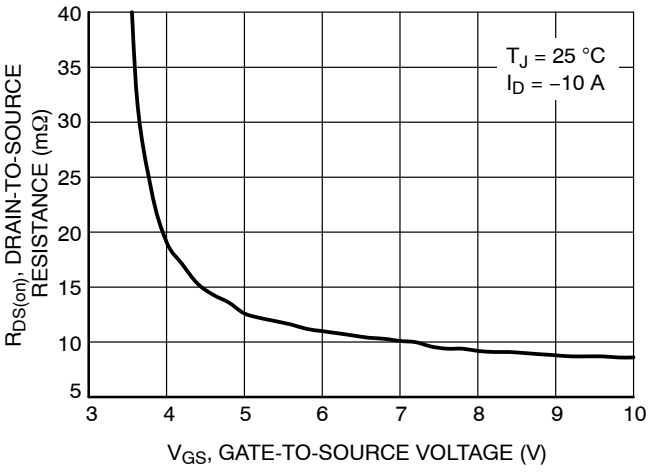


Figure 3. On-Resistance vs. Gate-to-Source Voltage (V)

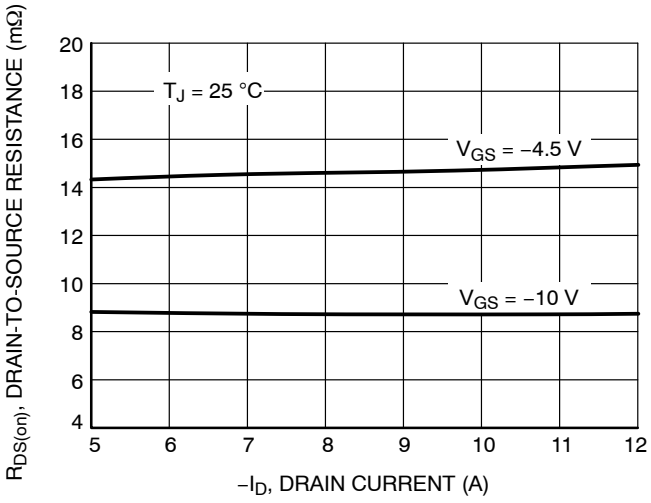


Figure 4. On-Resistance vs. Drain Current and Gate Voltage

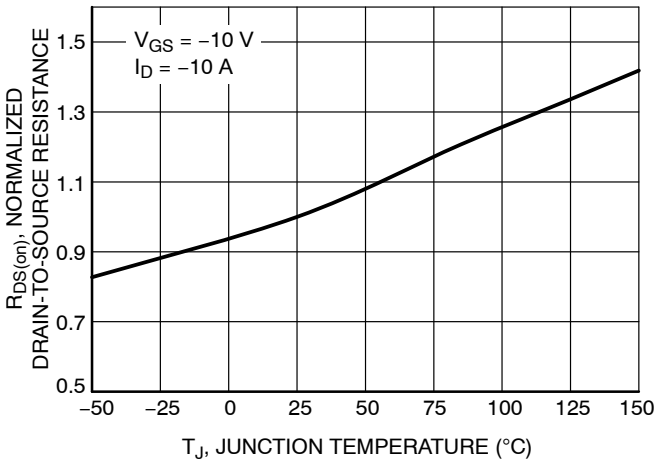


Figure 5. On-Resistance Variation with Temperature

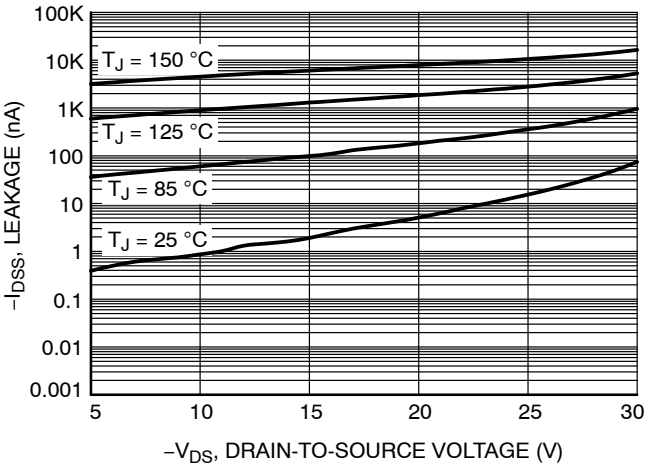


Figure 6. Drain-to-Source Leakage Current vs. Voltage

TYPICAL CHARACTERISTICS (continued)

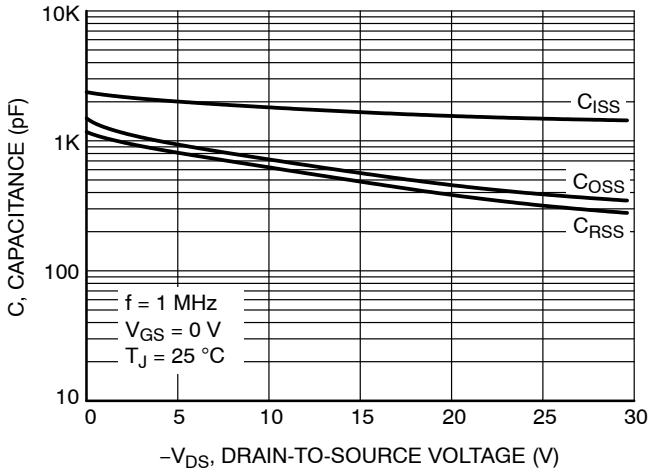


Figure 7. Capacitance Variation

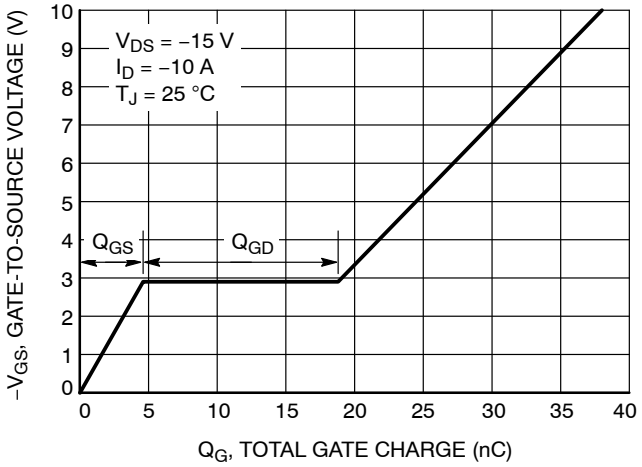


Figure 8. Gate-to-Source vs. Total Charge

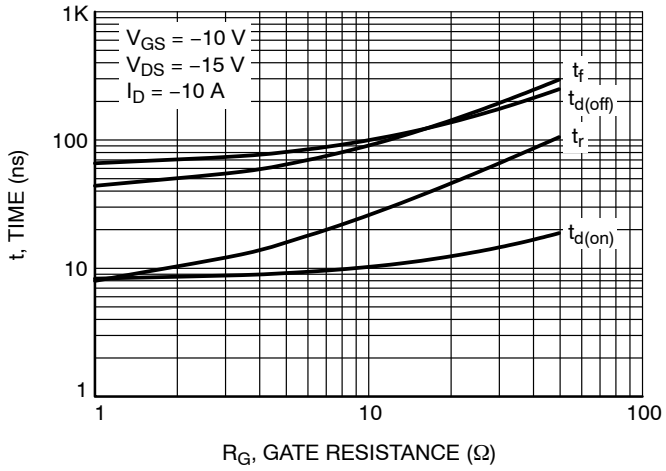


Figure 9. Resistive Switching Time Variation vs. Gate Resistance

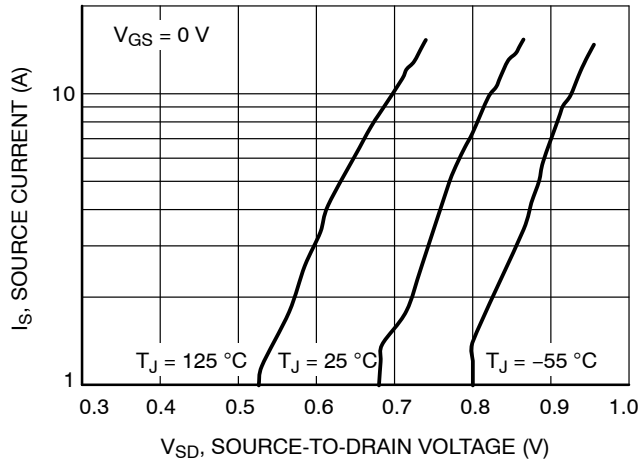


Figure 10. Diode Forward Voltage vs. Current

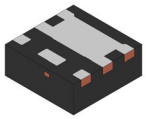
DEVICE ORDERING INFORMATION

Device	Package	Shipping†
NTLJS17D0P03P8ZTAG	WDFN6 (Pb-Free)	3,000 / Tape & Reel

† For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

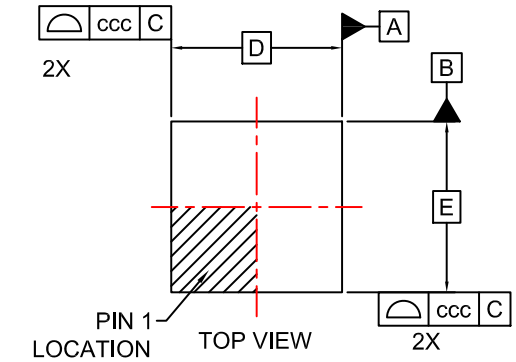
REVISION HISTORY

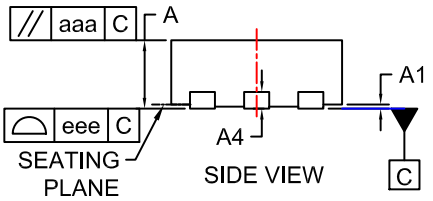
Revision	Description of Changes	Date
P5	Rebranded the Data Sheet to **onsemi** format.	02/23/2026

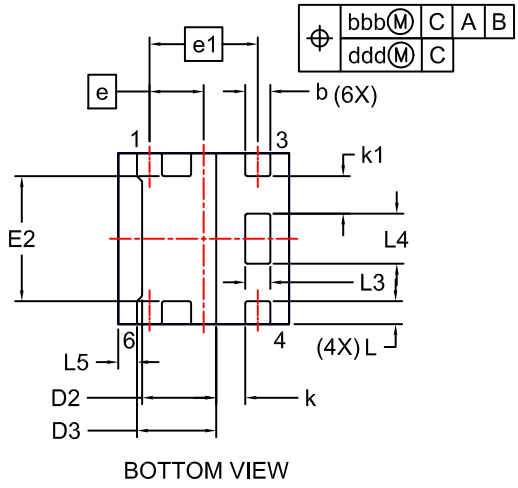


WDFN6 2.05X2.05, 0.65P
CASE 483AV
ISSUE A

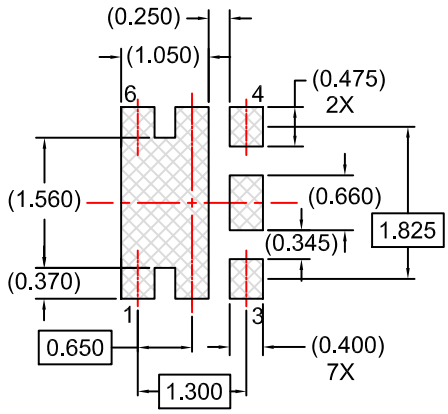
DATE 02 APR 2019







LAND PATTERN
RECOMMENDATION



NOTES:

1. CONTROLLING DIMENSION: MILLIMETERS.
2. COPLANARITY APPLIES TO THE EXPOSED PADS AS WELL AS THE TERMINALS.
3. DIMENSIONS D AND E DO NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS.
4. SEATING PLANE IS DEFINED BY THE TERMINALS. "A1" IS DEFINED AS THE DISTANCE FROM THE SEATING PLANE TO THE LOWEST POINT ON THE PACKAGE BODY.

DIM	MILLIMETERS		
	MIN.	NOM.	MAX.
A	0.60	0.70	0.80
A1	0.00	-	0.05
A4		(0.20)	
b	0.25	0.30	0.35
D	1.95	2.05	2.15
D2	0.84	0.89	0.94
D3		(0.95)	
E	1.95	2.05	2.15
E2	1.45	1.50	1.55
e		0.65 BSC	
e1		1.30 BSC	
k		(0.35)	
k1		(0.45)	
L	0.18	0.28	0.38
L3	0.25	0.30	0.35
L4	0.55	0.60	0.65
L5		(0.23)	
aaa		0.10	
bbb		0.10	
ccc		0.05	
ddd		0.05	
eee		0.05	

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DESCRIPTION:	**WDFN6 2.05X2.05, 0.65P**		**PAGE 1 OF 1**

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Üretici parça numarasını yazın; stok ve fiyatı hemen görün.

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Toplu alım ve teklif

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Teklif isteyin

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