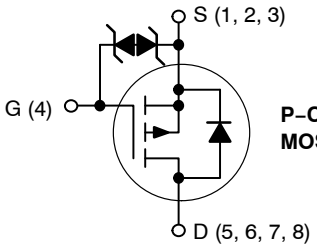
MOSFET - Power, Single P-Channel, SO8-FL
-30 V, 1.4 mΩ, -263 A

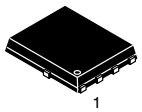
NTMFS002P03P8Z

$V_{(BR)DSS}$	$R_{DS(on)}$	I_D
−30 V	1.4 mΩ @ −10 V	−263 A
	2.3 mΩ @ −4.5 V	



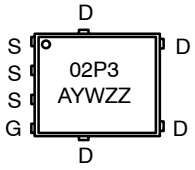
Features
- Ultra Low $R_{DS(on)}$ to Improve System Efficiency
- Advanced Package Technology in 5x6mm for Space Saving and Excellent Thermal Conduction
- These Devices are Pb−Free, Halogen Free/BFR Free and are RoHS Compliant

Typical Applications
- Power Load Switch
- Protection: Reverse Current, Over Voltage, and Reverse Negative Voltage
- Battery Management



SO−8 FLAT LEAD
CASE 506EZ

MARKING DIAGRAM



A = Assembly Location
Y = Year
W = Work Week
ZZ = Lot Traceability

MAXIMUM RATINGS (T_J = 25°C unless otherwise noted)

Parameter			Symbol	Value	Unit
Drain−to−Source Voltage			V_{DSS}	−30	V
Gate−to−Source Voltage			V_{GS}	±25	V
Continuous Drain Current $R_{\theta JC}$ (Notes 1, 2)	Steady State	T_C = 25°C	I_D	−263	A
		T_C = 85°C		−189	
Power Dissipation $R_{\theta JC}$ (Notes 1, 2)		T_C = 25°C	P_D	138.9	W
Continuous Drain Current $R_{\theta JA}$ (Notes 1, 2)	Steady State	T_A = 25°C	I_D	−40.2	A
		T_A = 85°C		−29	
Power Dissipation $R_{\theta JA}$ (Notes 1, 2)		T_A = 25°C	P_D	3.3	W
Pulsed Drain Current	T_A = 25°C, t_p = 10 μs		I_{DM}	−648	A
Single Pulse Drain−to−Source Avalanche Energy (I_L=65.16 A)			E_{AS}	212.3	mJ
Operating Junction and Storage Temperature Range			T_J, T_{stg}	−55 to +150	°C
Lead Temperature for Soldering Purposes (1/8″ from case for 10 s)			T_L	260	°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

THERMAL RESISTANCE MAXIMUM RATINGS

Parameter	Symbol	Value	Unit
Junction−to−Case − Steady State (Drain) (Note 2)	$R_{\theta JC}$	0.9	°C/W
Junction−to−Ambient − Steady State (Note 2)	$R_{\theta JA}$	38.3	°C/W

1. The entire application environment impacts the thermal resistance values shown, they are not constants and are only valid for the particular conditions noted.
2. Surface−mounted on FR4 board using a 1 in^2, 2 oz. Cu pad. Assuming a 76 mm x 76 mm x 1.6 mm board.

ORDERING INFORMATION

Device	Package	Shipping†
NTMFS002P03P8ZT1G	SO8−FL (Pb−Free)	1500 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specification Brochure, BRD8011/D.

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ELECTRICAL CHARACTERISTICS (T_J = 25°C unless otherwise noted)

Parameter	Symbol	Test Condition		Min	Typ	Max	Unit
OFF CHARACTERISTICS							
Drain−to−Source Breakdown Voltage	$V_{(BR)DSS}$	V_{GS} = 0 V, I_D = −250 μA		−30			V
Drain−to−Source Breakdown Voltage Temperature Coefficient	$V_{(BR)DSS}/T_J$	I_D = −250 μA, ref to 25°C			−3.3		mV/°C
Zero Gate Voltage Drain Current	I_{DSS}	V_{GS} = 0 V, V_{DS} = −24 V	T_J = 25°C			−1.0	μA
Gate−to−Source Leakage Current	I_{GSS}	V_{DS} = 0 V, V_{GS} = ±25 V				±10	μA
ON CHARACTERISTICS (Note 3)							
Gate Threshold Voltage	$V_{GS(TH)}$	V_{GS} = V_{DS}, I_D = −250 μA		−1.0		−3.0	V
Threshold Temperature Coefficient	$V_{GS(TH)}/T_J$	I_D = −250 μA, ref to 25°C			5.7		mV/°C
Drain−to−Source On Resistance	$R_{DS(on)}$	V_{GS} = −10 V, I_D = −23 A			0.9	1.4	mΩ
		V_{GS} = −4.5 V, I_D = −20 A			1.5	2.3	
Froward Transconductance	g_{FS}	V_{DS} = −5 V, I_D = −20 A			129		S
CHARGES AND CAPACITANCES							
Input Capacitance	C_{iss}	V_{GS} = 0 V, f = 1.0 MHz, V_{DS} = −15 V			14950		pF
Output Capacitance	C_{oss}				5280		
Reverse Transfer Capacitance	C_{rss}				4870		
Total Gate Charge	$Q_{G(TOT)}$	V_{GS} = −4.5 V, V_{DS} = −15 V, I_D = −23 A			217		nC
Threshold Gate Charge	$Q_{G(TH)}$				13		
Gate−to−Source Charge	Q_{GS}				35		
Gate−to−Drain Charge	Q_{GD}				145		
Total Gate Charge	$Q_{G(TOT)}$	V_{GS} = −10 V, V_{DS} = −15 V, I_D = −23 A			365		
SWITCHING CHARACTERISTICS, V_{GS} = 4.5 V (Note 3)							
Turn−On Delay Time	$t_{d(on)}$	V_{GS} = −4.5 V, V_{DS} = −15 V, I_D = −23 A, R_G = 6 Ω			68		ns
Rise Time	t_r				375		
Turn−Off Delay Time	$t_{d(off)}$				160		
Fall Time	t_f				317		
SWITCHING CHARACTERISTICS, V_{GS} = 10 V (Note 3)							
Turn−On Delay Time	$t_{d(on)}$	V_{GS} = −10 V, V_{DS} = −15 V, I_D = −23 A, R_G = 6 Ω			27		ns
Rise Time	t_r				78		
Turn−Off Delay Time	$t_{d(off)}$				280		
Fall Time	t_f				295		
DRAIN−SOURCE DIODE CHARACTERISTICS							
Forward Diode Voltage	V_{SD}	V_{GS} = 0 V, I_S = −23 A	T_J = 25°C		−0.65	−1.3	V
			T_J = 125°C		−0.48		
Reverse Recovery Time	t_{RR}	V_{GS} = 0 V, dI_S/dt = 100 A/μs, I_S = −23 A			82		ns
Charge Time	t_a				47		
Discharge Time	t_b				36		
Reverse Recovery Charge	Q_{RR}				180		nC

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

3. Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2%.

TYPICAL CHARACTERISTICS

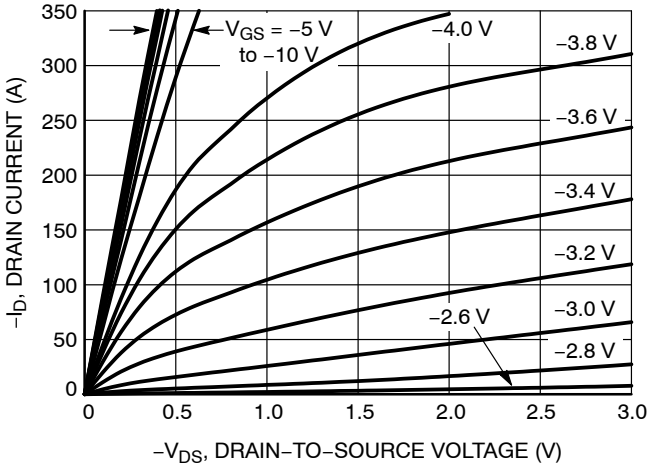


Figure 1. On−Region Characteristics

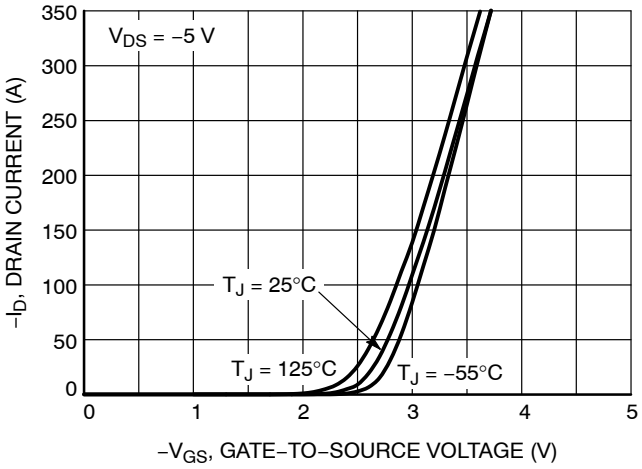


Figure 2. Transfer Characteristics

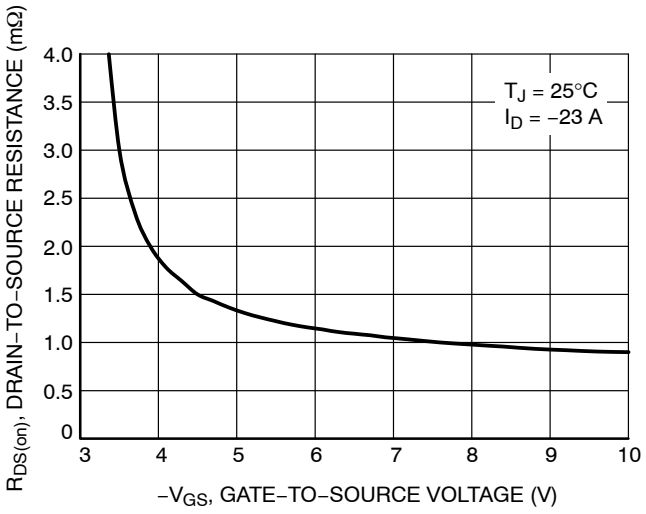


Figure 3. On−Resistance vs. Gate−to−Source Voltage

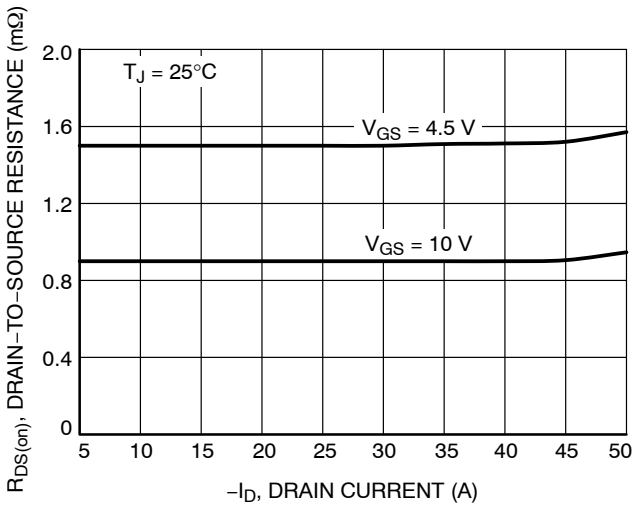


Figure 4. On−Resistance vs. Drain Current and Gate Voltage

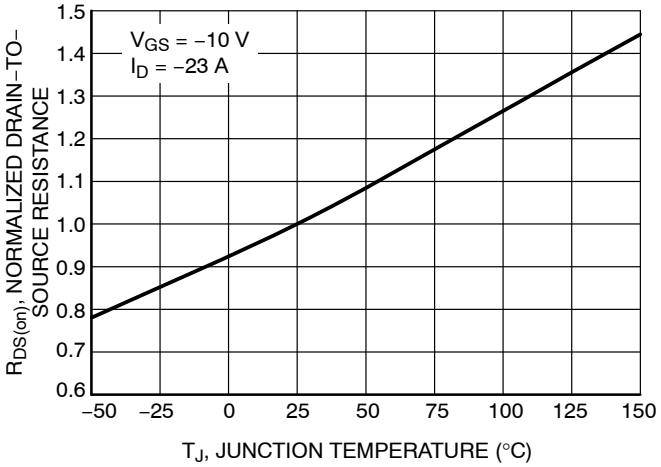


Figure 5. On−Resistance Variation with Temperature

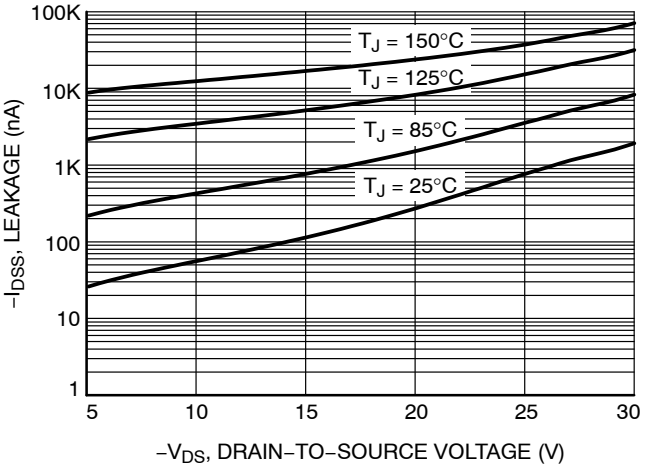


Figure 6. Drain−to−Source Leakage Current vs. Voltage

TYPICAL CHARACTERISTICS

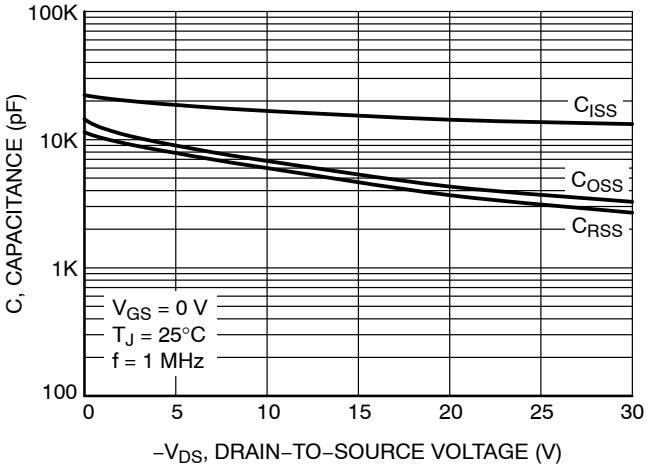


Figure 7. Capacitance Variation

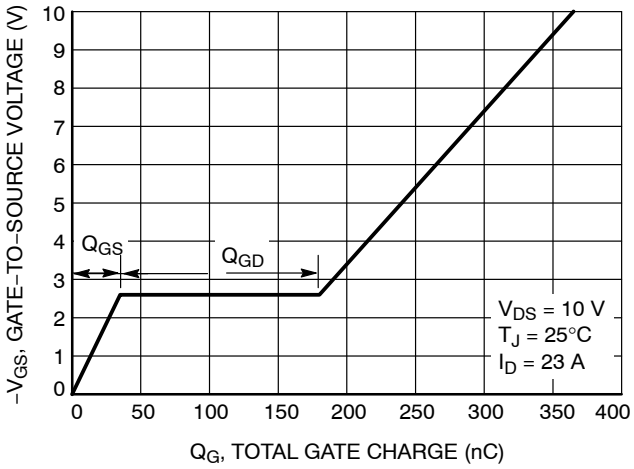


Figure 8. Gate−to−Source Voltage vs. Total Charge

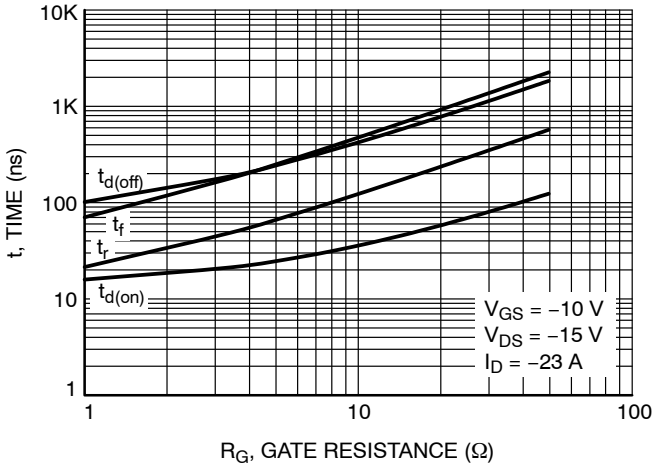


Figure 9. Resistive Switching Time Variation vs. Gate Resistance

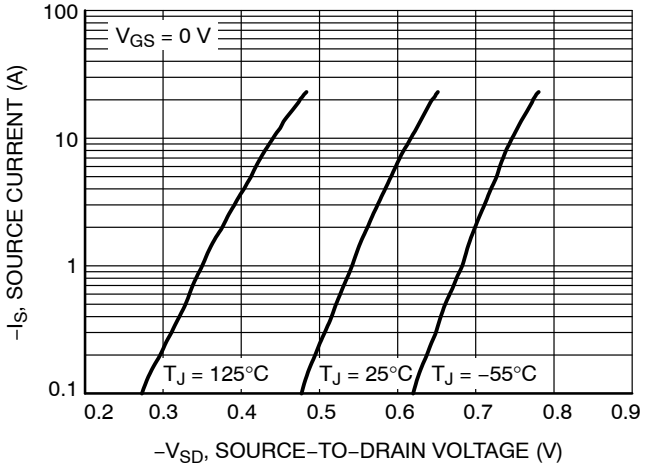


Figure 10. Diode Forward Voltage vs. Current

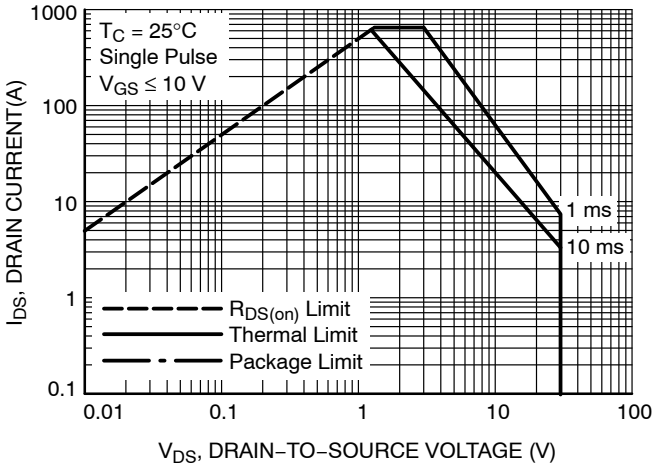


Figure 11. Maximum Rated Forward Biased Safe Operating Area

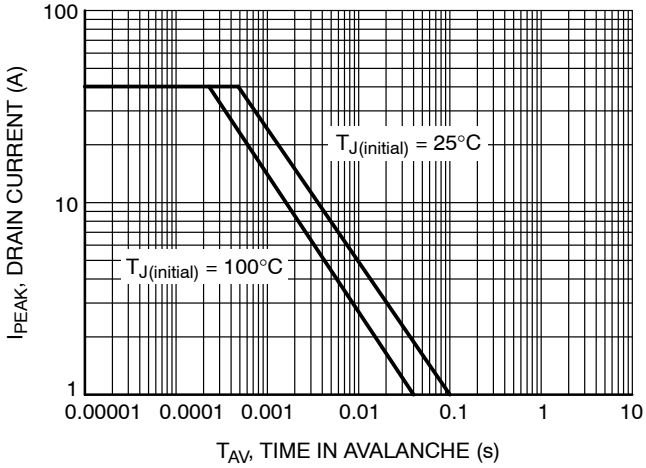


Figure 12. I_{PEAK} vs. Time in Avalanche

TYPICAL CHARACTERISTICS

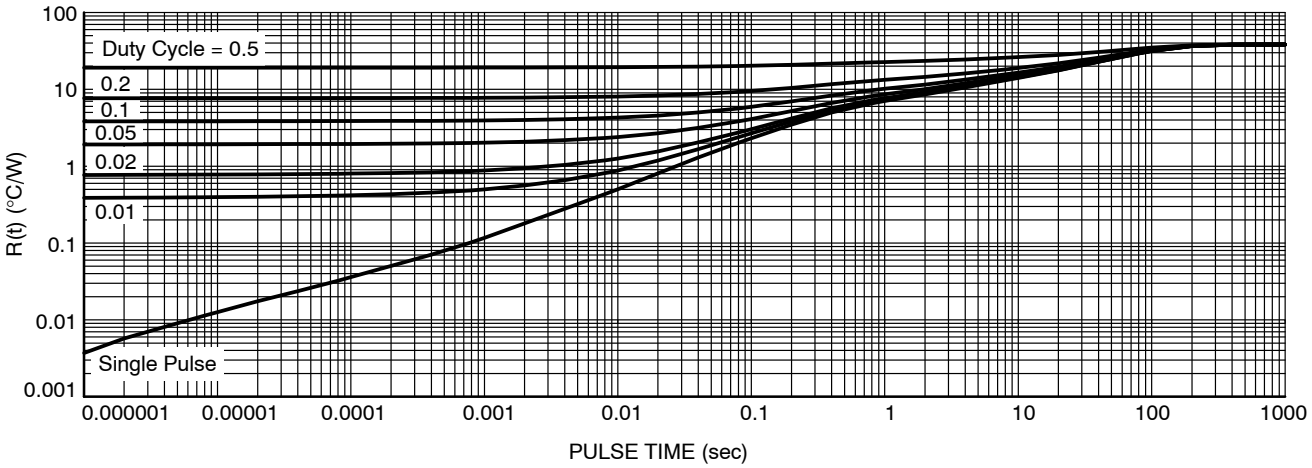
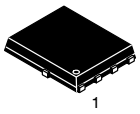


Figure 13. Thermal Characteristics

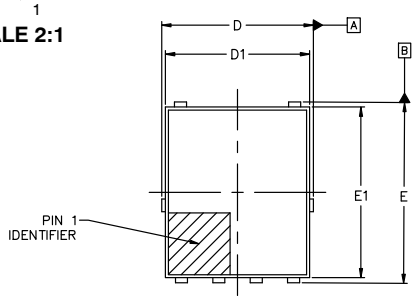


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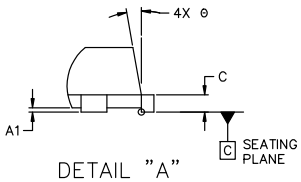
DFN−5, 4.90x5.90x1.00, 1.27P
CASE 506EZ
ISSUE C

DATE 18 JUN 2026

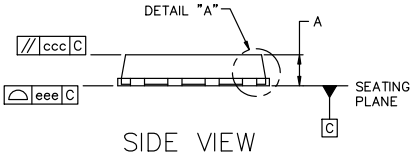
NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 2018.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSIONS D1 AND E1 DO NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR GATE BURRS.



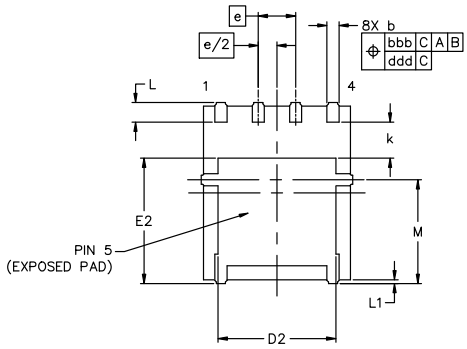
TOP VIEW



DETAIL "A"
SCALED 2:1



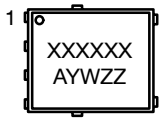
SIDE VIEW



BOTTOM VIEW

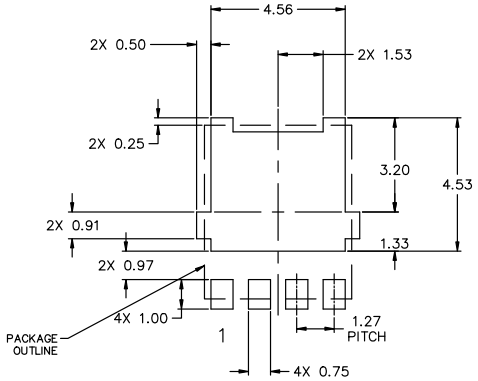
MILLIMETERS			
DIM	MIN	NOM	MAX
A	0.90	1.00	1.10
A1	0.00	−−−	0.05
b	0.33	0.41	0.51
c	0.23	0.28	0.33
D	5.00	5.15	5.30
D1	4.70	4.90	5.10
D2	3.80	4.00	4.20
E	6.00	6.15	6.30
E1	5.70	5.90	6.10
E2	3.45	3.80	3.85
e	1.27 BSC		
G	0.51	0.575	0.71
k	1.10	1.20	1.40
L	0.51	0.575	0.71
L1	0.125 REF		
M	3.00	3.40	3.80
θ	0°	−−−	12°
TOLERANCE FORM & POSITION			
bbb	0.10		
ccc	0.10		
ddd	0.05		
eee	0.10		

GENERIC MARKING DIAGRAM*



XXXXXX = Specific Device Code
A = Assembly Location
Y = Year
W = Work Week
ZZ = Lot Traceability

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, "G" or microdot " ▪", may or may not be present. Some products may not follow the Generic Marking.



RECOMMENDED MOUNTING FOOTPRINT

*For additional information on our Pb−Free strategy and soldering details, please download the onsemi Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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