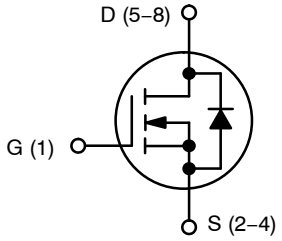
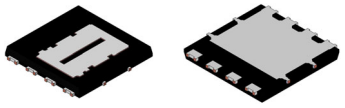
MOSFET - Power, Single N-Channel
100 V, 1.7 mΩ, 267 A

NTMTSC1D6N10MC

$V_{(BR)DSS}$	$R_{DS(ON)}$ MAX	I_D MAX
100 V	1.7 mΩ @ 10 V	267 A



N–CHANNEL MOSFET



TDFNW8
CASE 507AS

Features

- Small Footprint (8x8 mm) for Compact Design
- Low $R_{DS(on)}$ to Minimize Conduction Losses
- Low Q_G and Capacitance to Minimize Driver Losses
- New Power 88 Dual Cool Package
- These Devices are Pb–Free and are RoHS Compliant

MAXIMUM RATINGS (T_J = 25°C unless otherwise noted)

Parameter			Symbol	Value	Unit
Drain–to–Source Voltage			V_{DSS}	100	V
Gate–to–Source Voltage			V_{GS}	±20	V
Continuous Drain Current $R_{\theta JC}$ (Notes 1, 3)	Steady State	T_C = 25°C	I_D	267	A
		T_C = 100°C		189	
Power Dissipation $R_{\theta JC}$ (Note 1)		T_C = 25°C	P_D	291	W
		T_C = 100°C		145	
Continuous Drain Current $R_{\theta JA}$ (Notes 1, 2, 3)	Steady State	T_A = 25°C	I_D	30	A
		T_A = 100°C		21	
Power Dissipation $R_{\theta JA}$ (Notes 1, 2)		T_A = 25°C	P_D	3.9	W
		T_A = 100°C		1.9	
Pulsed Drain Current	T_A = 25°C, t_p = 10 μs		I_{DM}	900	A
Operating Junction and Storage Temperature Range			T_J, T_{stg}	−55 to +175	°C
Source Current (Body Diode)			I_S	243	A
Single Pulse Drain–to–Source Avalanche Energy ($I_{L(pk)}$ = 22.3 A)			E_{AS}	1550	mJ
Lead Temperature for Soldering Purposes (1/8″ from case for 10 s)			T_L	260	°C

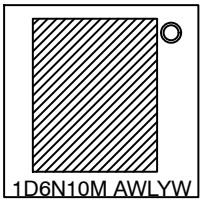
Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

THERMAL RESISTANCE MAXIMUM RATINGS

Parameter	Symbol	Value	Unit
Junction–to–Case – Bottom – Steady State	$R_{\theta JCB}$	0.5	°C/W
Junction–to–Case – Top – Steady State	$R_{\theta JCT}$	0.8	
Junction–to–Ambient – Steady State (Note 2)	$R_{\theta JA}$	38	

1. The entire application environment impacts the thermal resistance values shown, they are not constants and are only valid for the particular conditions noted.
2. Surface–mounted on FR4 board using a 650 mm^2, 2 oz. Cu pad.
3. Maximum current for pulses as long as 1 second is higher but is dependent on pulse duration and duty cycle.

MARKING DIAGRAM



1D6N10M = Specific Device Code
A = Assembly Location
WL = Wafer Lot Code
Y = Year Code
W = Work Week Code

ORDERING INFORMATION

See detailed ordering, marking and shipping information in the package dimensions section on page 5 of this data sheet.

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ELECTRICAL CHARACTERISTICS (T_J = 25°C unless otherwise specified)

Parameter	Symbol	Test Condition		Min	Typ	Max	Unit
OFF CHARACTERISTICS							
Drain−to−Source Breakdown Voltage	$V_{(BR)DSS}$	V_{GS} = 0 V, I_D = 250 μA		100			V
Drain−to−Source Breakdown Voltage Temperature Coefficient	$V_{(BR)DSS}/T_J$				64.5		mV/°C
Zero Gate Voltage Drain Current	I_{DSS}	V_{GS} = 0 V, V_{DS} = 100 V	T_J = 25 °C			5	μA
			T_J = 125°C			10	
Gate−to−Source Leakage Current	I_{GSS}	V_{DS} = 0 V, V_{GS} = 20 V				100	nA
ON CHARACTERISTICS (Note 4)							
Gate Threshold Voltage	$V_{GS(TH)}$	V_{GS} = V_{DS}, I_D = 650 μA		2.0		4.0	V
Threshold Temperature Coefficient	$V_{GS(TH)}/T_J$				−10		mV/°C
Drain−to−Source On Resistance	$R_{DS(on)}$	V_{GS} = 10 V	I_D = 90 A		1.42	1.7	mΩ
		V_{GS} = 6 V	I_D = 58 A			4.3	
Forward Transconductance	g_{FS}	V_{DS} =5 V, I_D = 100 A			233		S
CHARGES, CAPACITANCES & GATE RESISTANCE							
Input Capacitance	C_{ISS}	V_{GS} = 0 V, f = 100 KHz, V_{DS} = 50 V			7630		pF
Output Capacitance	C_{OSS}				4260		
Reverse Transfer Capacitance	C_{RSS}				80		
Total Gate Charge	$Q_{G(TOT)}$	V_{GS} = 10 V, V_{DS} = 50 V; I_D = 116 A			106		nC
Threshold Gate Charge	$Q_{G(TH)}$	V_{GS} = 10 V, V_{DS} = 50 V; I_D = 116 A			20		
Gate−to−Source Charge	Q_{GS}				35		
Gate−to−Drain Charge	Q_{GD}				22		
Plateau Voltage	V_{GP}				5		V
SWITCHING CHARACTERISTICS (Note 5)							
Turn−On Delay Time	$t_{d(ON)}$	V_{GS} = 10 V, V_{DS} = 50 V, I_D = 116 A, R_G = 6 Ω			34		ns
Rise Time	t_r				24		
Turn−Off Delay Time	$t_{d(OFF)}$				69		
Fall Time	t_f				29		
DRAIN−SOURCE DIODE CHARACTERISTICS							
Forward Diode Voltage	V_{SD}	V_{GS} = 0 V, I_S = 90 A	T_J = 25°C		0.83	1.2	V
			T_J = 125°C		0.7		
Reverse Recovery Time	t_{RR}	V_{GS} = 0 V, dIS/dt = 100 A/μs, I_S = 58 A			82		ns
Charge Time	t_a				55		
Discharge Time	t_b				27		
Reverse Recovery Charge	Q_{RR}				147		nC
Reverse Recovery Time	t_{RR}	V_{GS} = 0 V, dIS/dt = 1000 A/μs, I_S = 58 A			43		ns
Charge Time	t_a				23		
Discharge Time	t_b				19		
Reverse Recovery Charge	Q_{RR}				385		nC

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

4. Pulse Test: pulse width ≤ 300 μs, duty cycle ≤ 2%.
5. Switching characteristics are independent of operating junction temperatures.

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TYPICAL CHARACTERISTICS

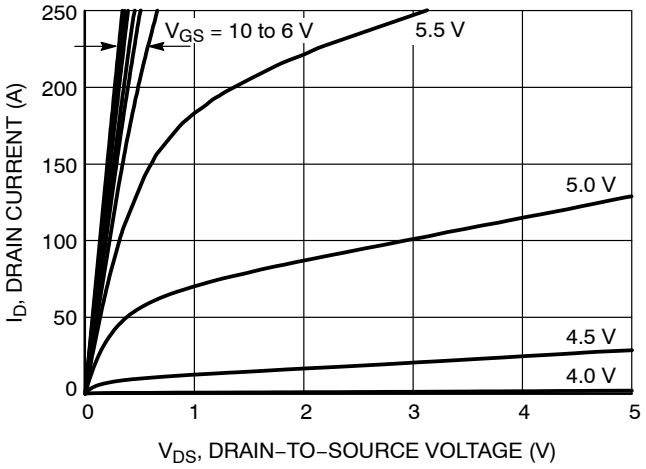


Figure 1. On−Region Characteristics

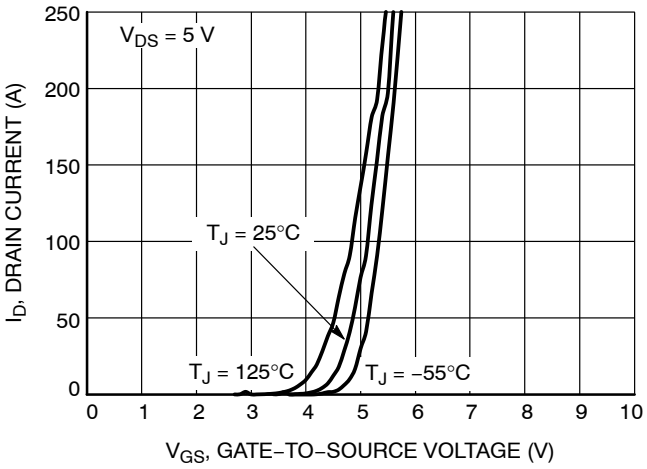


Figure 2. Transfer Characteristics

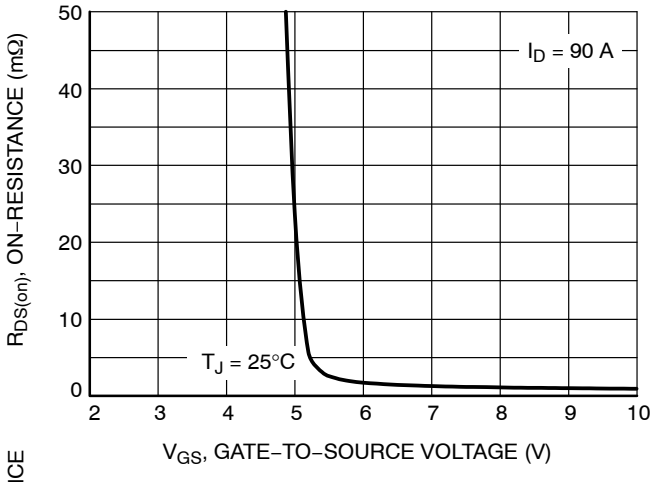


Figure 3. On−Resistance vs. Gate−to−Source Voltage

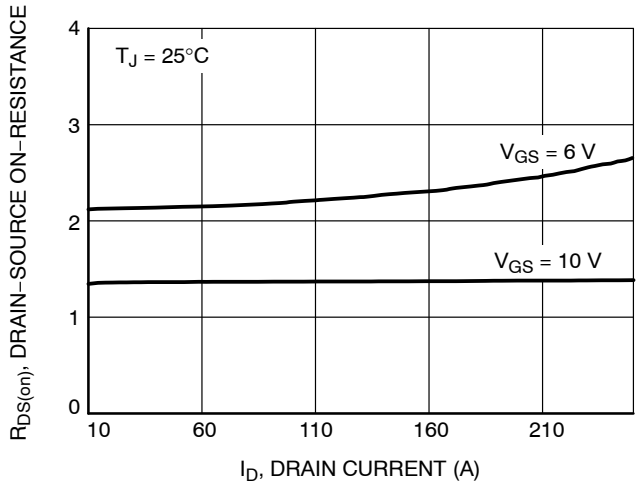


Figure 4. On−Resistance vs. Drain Current

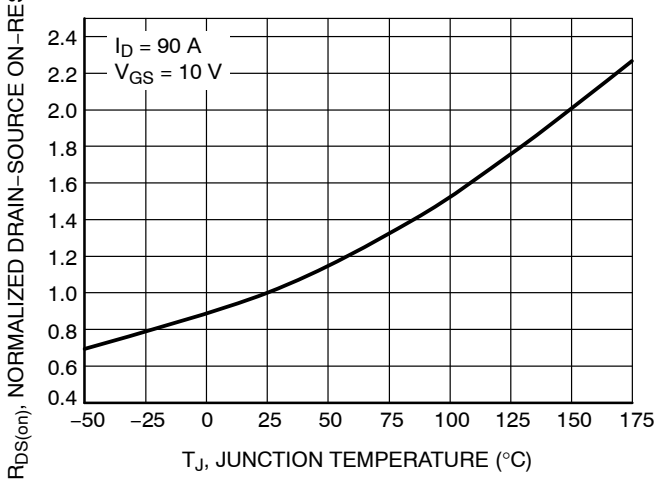


Figure 5. On−Resistance Variation with Temperature

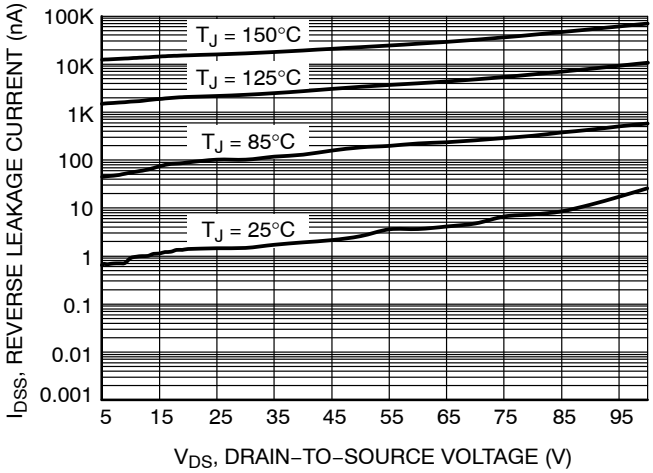


Figure 6. Drain−to−Source Leakage Current vs. Voltage

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TYPICAL CHARACTERISTICS

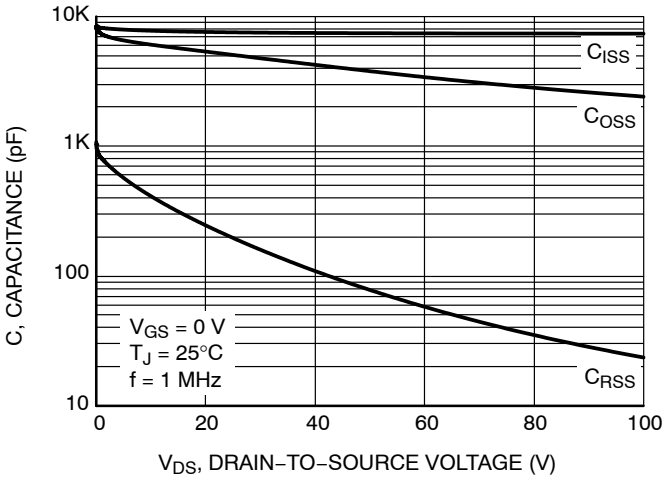


Figure 7. Capacitance Variation

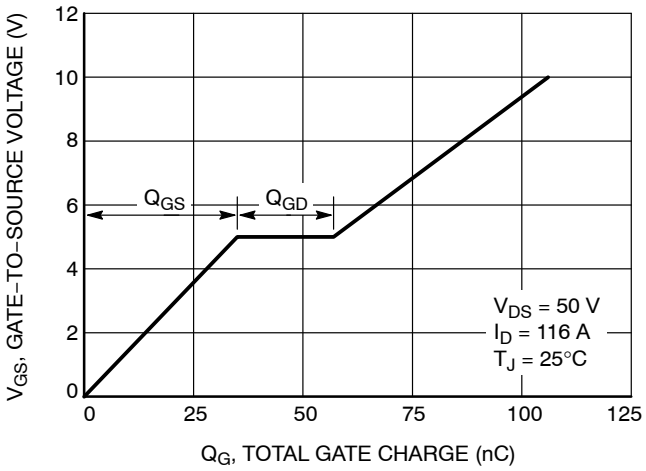


Figure 8. Gate−to−Source Voltage vs. Total Charge

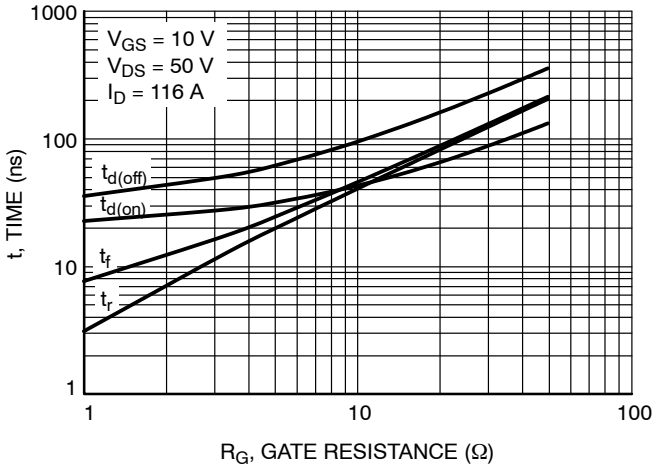


Figure 9. Resistive Switching Time Variation vs. Gate Resistance

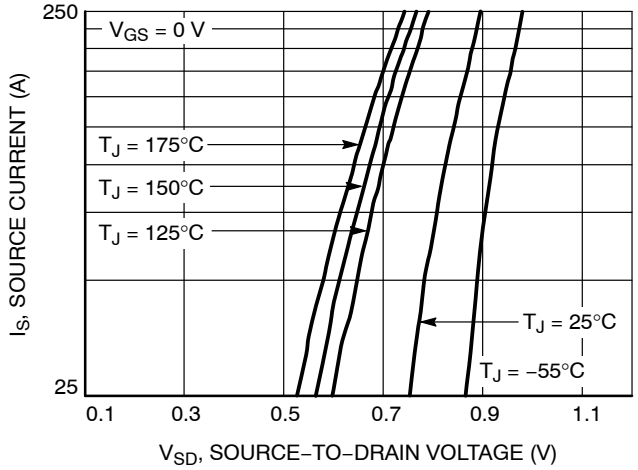


Figure 10. Diode Forward Voltage vs. Current

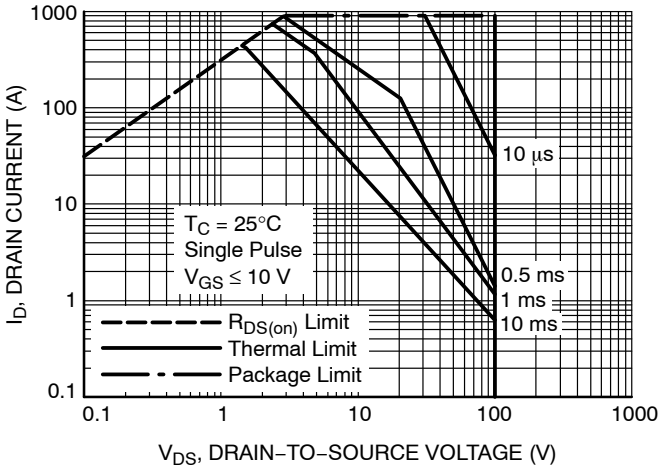


Figure 11. Safe Operating Area

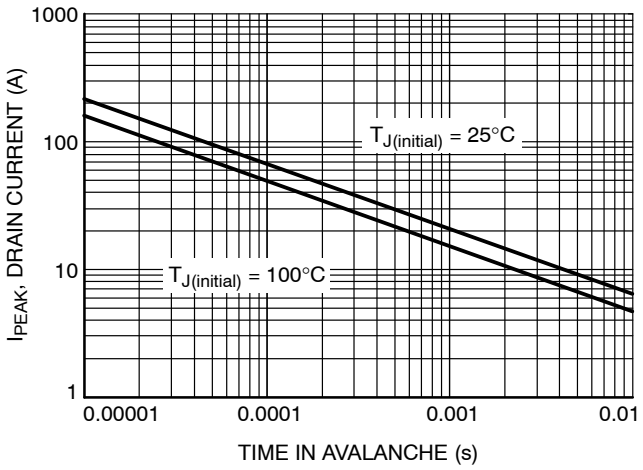


Figure 12. Maximum Drain Current vs. Time in Avalanche

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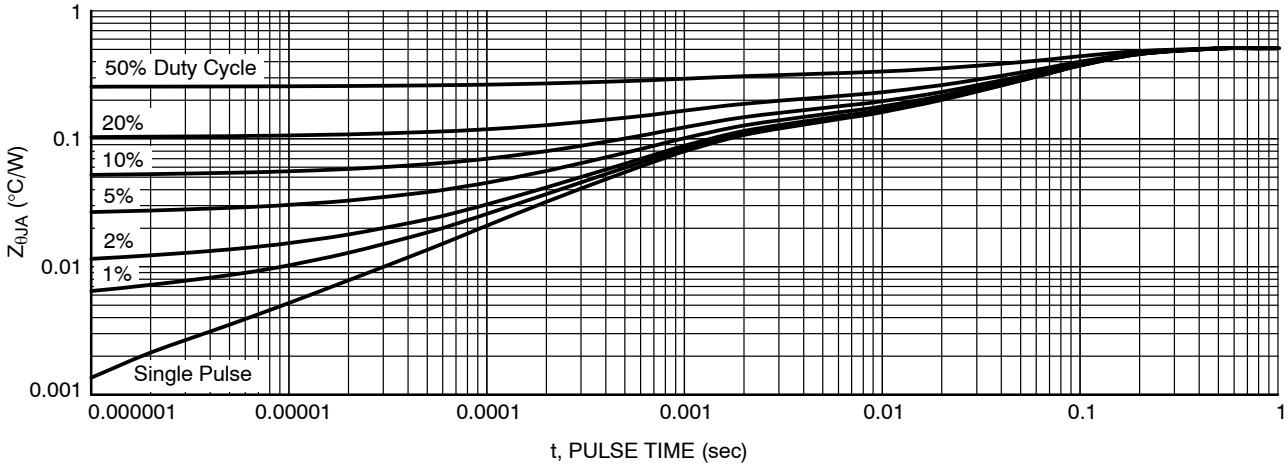


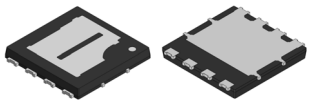
Figure 13. Junction−to−Ambient Transient Thermal Response

DEVICE ORDERING INFORMATION

Device	Marking	Package	Shipping†
NTMTSC1D6N10MCTXG	1D6N10M	TDFNW8 (Pb−Free)	3,000 / Tape & Reel

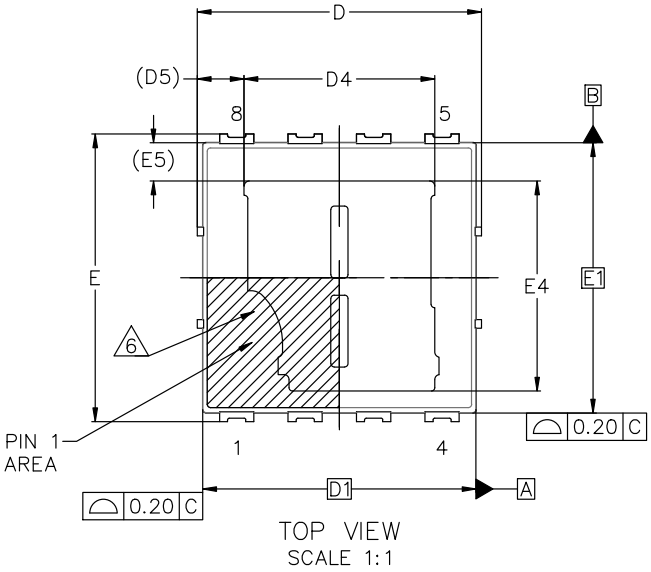
†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

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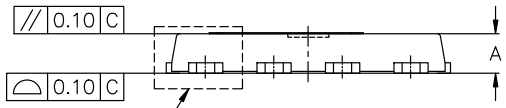


TDFNW−8 8.30x8.40x0.92, 2.00P
CASE 507AS
ISSUE D

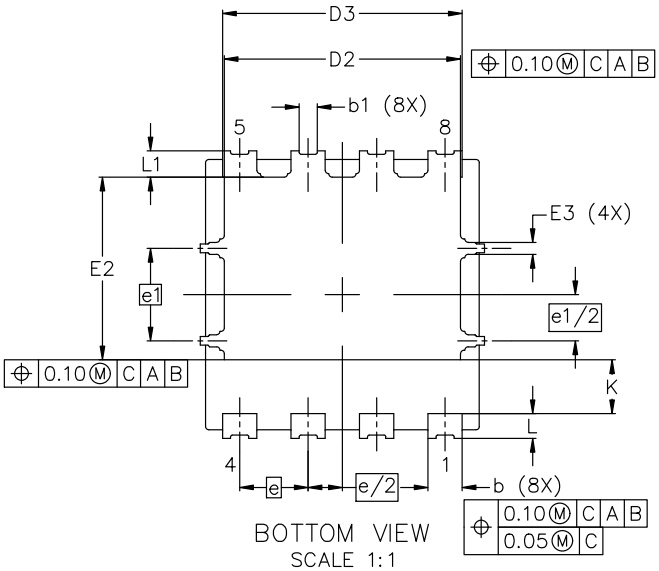
DATE 26 OCT 2026



TOP VIEW
SCALE 1:1

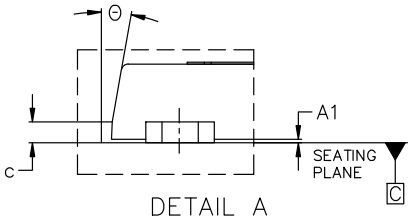


FRONT VIEW
SCALE 1:1



BOTTOM VIEW
SCALE 1:1

NOTES:
1. DIMENSIONING & TOLERANCING PER ASME Y14.5M, 2009.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. COPLANARITY APPLIES TO THE EXPOSED PADS AS WELL AS THE TERMINALS.
4. DIMENSIONS D1 AND E1 DO NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR GATE BURRS.
5. SEATING PLANE IS DEFINED BY THE TERMINALS. "A1" IS DEFINED AS THE DISTANCE FROM THE SEATING PLANE TO THE LOWEST POINT ON THE PACKAGE BODY.
6. SLOT PARTITION IS OPTIONAL.



DETAIL A
SCALE 2:1

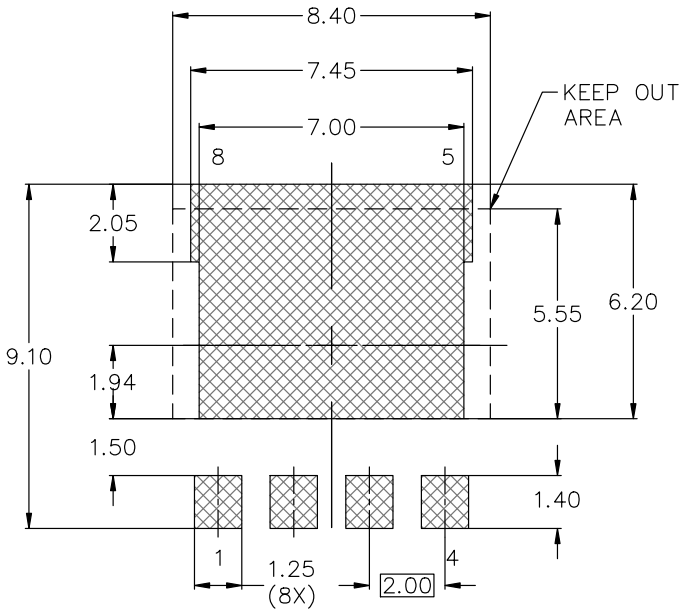
DIM	MILLIMETERS		
	MIN.	NOM.	MAX.
A	0.82	0.92	1.02
A1	0.00	0.02	0.05
b	0.90	1.00	1.10
b1	0.35	0.45	0.55
c	0.23	0.28	0.33
D	8.20	8.30	8.40
D1		8.00 BSC	
D2	6.80	6.90	7.00
D3	6.90	7.00	7.10
D4	5.52	5.67	5.82
D5		1.16 REF.	
E	8.30	8.40	8.50
E1		7.90 BSC	
E2	5.24	5.34	5.44
E3	0.25	0.35	0.45
E4	6.08	6.23	6.38
E5		1.13 REF.	
e		2.00 BSC	
e/2		1.00 BSC	
e1		2.70 BSC	
e1/2		1.35 BSC	
K	1.50	1.57	1.70
L	0.64	0.74	0.84
L1	0.67	0.77	0.87
Θ	0°	−−−	12°

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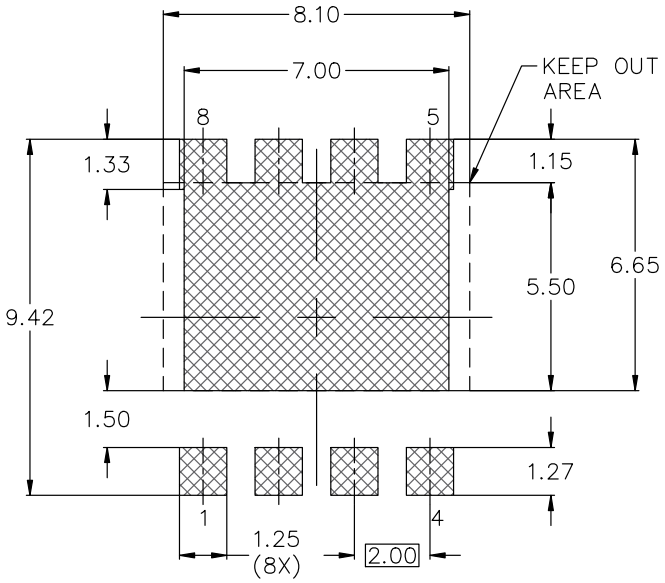
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CASE 507AS
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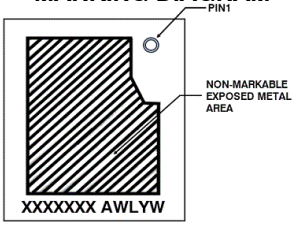


UNIVERSAL LAND PATTERN



RECOMMENDED MOUNTING FOOTPRINT
*FOR ADDITIONAL INFORMATION ON OUR Pb−FREE STRATEGY AND SOLDERING DETAILS, PLEASE DOWNLOAD THE onsemi SOLDERING AND MOUNTING TECHNIQUES REFERENCE MANUAL, SOLDERRM/D.

GENERIC MARKING DIAGRAM*



XXXX = Specific Device Code
A = Assembly Location
WL = Wafer Lot Code
Y = Year Code
W = Work Week Code

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, “G” or microdot “ ▪”, may or may not be present. Some products may not follow the Generic Marking.

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Üretici parça numarasını yazın; stok ve fiyatı hemen görün.

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Kategorilere göz atın

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Üreticileri görün

Toplu alım ve teklif

Listede olmayan ya da yüksek adetli parçalar için teklif isteyin.

Teklif isteyin

www.entegreci.com | **destek@entegreci.com** | **0850 305 90 34**

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