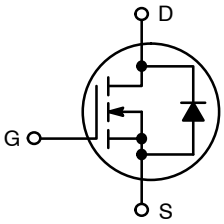
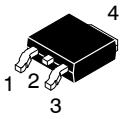
MOSFET – Power, N-Channel, SUPERFET® III, Easy Drive
650 V, 360 mΩ, 10 A

NVD360N65S3

V_{DSS}	$R_{DS(ON)}$ MAX	I_D MAX
650 V	360 mΩ @ 10 V	10 A



POWER MOSFET



DPAK
CASE 369C

Features

- Ultra Low Gate Charge & Low Effective Output Capacitance
- Lower FOM ($R_{DS(on)\ max.}$ x $Q_{g\ typ.}$ & $R_{DS(on)\ max.}$ x E_{OSS})
- 100% Avalanche Tested
- AEC−Q101 Qualified and PPAP Capable
- These Devices are Pb−Free and are RoHS Compliant

MAXIMUM RATINGS (T_C = 25°C unless otherwise noted)

Parameter	Symbol	Value	Unit
Drain−to−Source Voltage	V_{DSS}	650	V
Gate−to−Source Voltage − DC	V_{GSS}	±30	V
Gate−to−Source Voltage − AC (f > 1 Hz)	V_{GSS}	±30	V
Drain Current − Continuous (T_C = 25°C)	I_D	10	A
Drain Current − Continuous (T_C = 100°C)	I_D	6	A
Drain Current − Pulsed (Note 3)	I_{DM}	25	A
Power Dissipation (T_C = 25°C)	P_D	83	W
Power Dissipation − Derate Above 25°C	P_D	0.67	W/°C
Operating Junction and Storage Temperature Range	T_J, T_{STG}	−55 to +150	°C
Single Pulsed Avalanche Energy (Note 4)	E_{AS}	40	mJ
Repetitive Avalanche Energy (Note 3)	E_{AR}	0.83	mJ
MOSFET dv/dt	dv/dt	100	V/ns
Peak Diode Recovery dv/dt (Note 5)	dv/dt	20	V/ns
Max. Lead Temperature for Soldering Purposes (1/8″ from case for 5 s)	T_L	300	°C

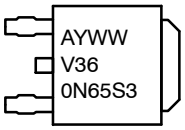
THERMAL CHARACTERISTICS

Parameter	Symbol	Value	Unit
Thermal Resistance, Junction−to−Case, Max. (Notes 1, 2)	$R_{\theta JC}$	1.5	°C/W
Thermal Resistance, Junction−to−Ambient, Max. (Notes 1, 2, 6)	$R_{\theta JA}$	52	

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. The entire application environment impacts the thermal resistance values shown. They are not constants and are only valid for the particular conditions noted.
2. Assembled to an infinite heatsink with perfect heat transfer from the case (assumes 0 K/W thermal interface).
3. Repetitive rating: pulse−width limited by maximum junction temperature.
4. I_{AS} = 2.1 A, R_G = 25 Ω, starting T_J = 25°C.
5. I_{SD} = 5 A, di/dt ≤ 200 A/μs, V_{DD} ≤ 400 V, starting T_J = 25°C.
6. Device on 1 in^2 pad 2 oz copper pad on 1.5 x 1.5 in. board of FR−4 material.

MARKING DIAGRAM



A = Assembly Location
Y = Year
WW = Work Week
V360N65S3 = Specific Device Code

ORDERING INFORMATION

Device	Package	Shipping†
NVD360N65S3	DPAK3 (Pb−Free)	2500 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specification Brochure, BRD8011/D.

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ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
OFF CHARACTERISTICS						
Drain−to−Source Breakdown Voltage	BV_{DSS}	V_{GS} = 0 V, I_D = 1 mA, T_J = 25°C	650			V
Drain−to−Source Breakdown Voltage	BV_{DSS}	V_{GS} = 0 V, I_D = 1 mA, T_J = 150°C	700			V
Breakdown Voltage Temperature Coefficient	$\Delta BV_{DSS}/\Delta T_J$	I_D = 1 mA, Referenced to 25°C		650		mV/°C
Zero Gate Voltage Drain Current	I_{DSS}	V_{GS} = 0 V, V_{DS} = 650 V			1	μA
		V_{DS} = 520 V, T_C = 125°C		0.33		
Gate−to−Body Leakage Current	I_{GSS}	V_{GS} = ±30 V, V_{DS} = 0 V			±100	nA
ON CHARACTERISTICS						
Gate Threshold Voltage	$V_{GS(th)}$	V_{GS} = V_{DS}, I_D = 0.2 mA	2.5		4.5	V
Threshold Temperature Coefficient	$\Delta V_{GS(th)}/\Delta T_J$	V_{GS} = V_{DS}, I_D = 0.2 mA		−8.8		mV/°C
Static Drain−to−Source On Resistance	$R_{DS(on)}$	V_{GS} = 10 V, I_D = 5 A		314	360	mΩ
Forward Transconductance	g_{FS}	V_{DS} = 20 V, I_D = 5 A		6		S
DYNAMIC CHARACTERISTICS						
Input Capacitance	C_{iss}	V_{GS} = 0 V, V_{DS} = 400 V, f = 1 MHz		756		pF
Output Capacitance	C_{oss}			17.4		
Reverse Transfer Capacitance	C_{rss}			1.53		
Effective Output Capacitance	$C_{oss(eff.)}$	V_{DS} = 0 V to 400 V, V_{GS} = 0 V		179		pF
Energy Related Output Capacitance	$C_{oss(er.)}$	V_{DS} = 0 V to 400 V, V_{GS} = 0 V		29.3		pF
Total Gate Charge at 10 V	$Q_{G(TOT)}$	V_{GS} = 10 V, V_{DS} = 400 V, I_D = 5 A (Note 7)		16.8		nC
Threshold Gate Charge	$Q_{G(TH)}$			2.8		
Gate−to−Source Gate Charge	Q_{GS}			4.6		
Gate−to−Drain “Miller” Charge	Q_{GD}			7		
Equivalent Series Resistance	ESR	f = 1 MHz		1		Ω
SWITCHING CHARACTERISTICS						
Turn-On Delay Time	$t_{d(on)}$	V_{GS} = 10 V, V_{DD} = 400 V, I_D = 5 A, R_g = 4.7 Ω (Note 7)		13.6		ns
Turn-On Rise Time	t_r			9.44		ns
Turn-Off Delay Time	$t_{d(off)}$			33.9		ns
Turn-Off Fall Time	t_f			11.2		ns
SOURCE−DRAIN DIODE CHARACTERISTICS						
Maximum Continuous Source−to−Drain Diode Forward Current	I_S	V_{GS} = 0 V			10	A
Maximum Pulsed Source−to−Drain Diode Forward Current	I_{SM}	V_{GS} = 0 V			25	A
Source−to−Drain Diode Forward Voltage	V_{SD}	V_{GS} = 0 V, I_{SD} = 5 A			1.2	V
Reverse Recovery Time	t_{rr}	V_{GS} = 0 V, dI_F/dt = 100 A/μs, I_{SD} = 5 A		197		ns
Charge Time	t_a			18		
Discharge Time	t_b			10		
Reverse Recovery Charge	Q_{rr}			2089		nC

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

7. Essentially independent of operating temperature typical characteristics.

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TYPICAL CHARACTERISTICS

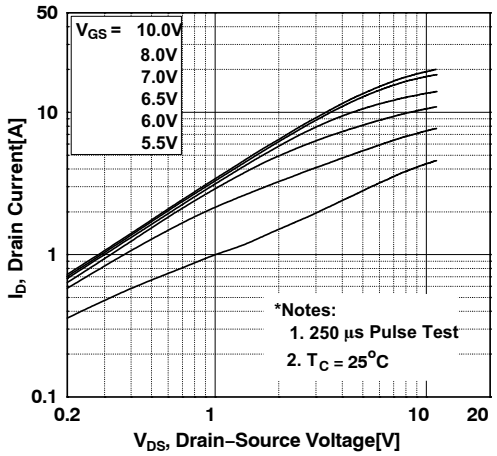


Figure 1. On−Region Characteristics 25°C

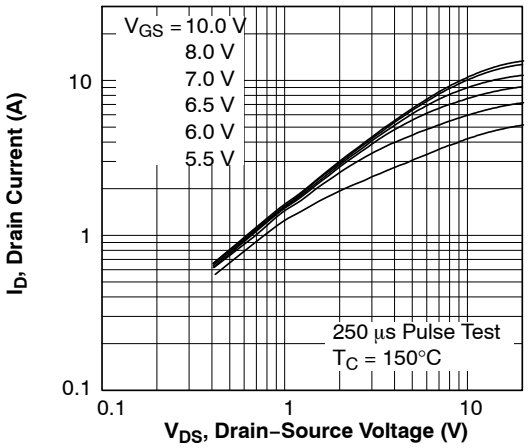


Figure 2. On−Region Characteristics 150°C

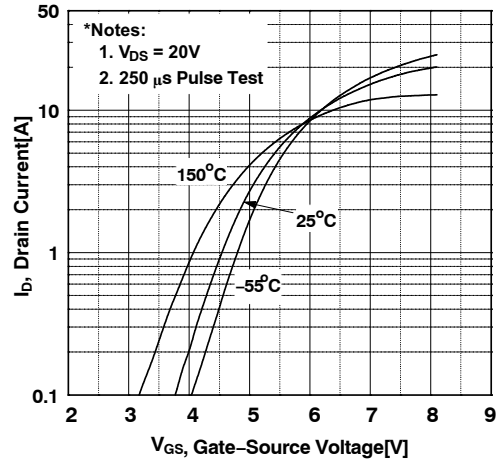


Figure 3. Transfer Characteristics

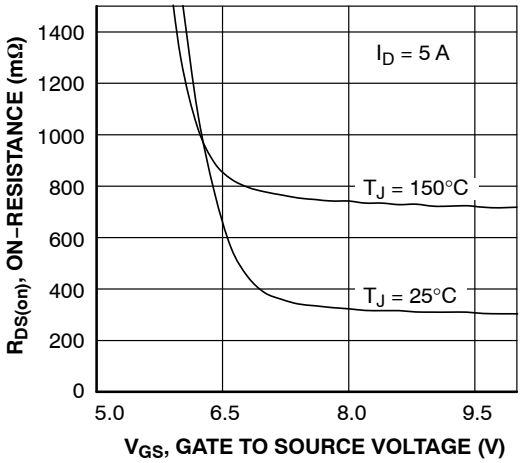


Figure 4. $R_{DS(on)}$ vs. Gate Voltage

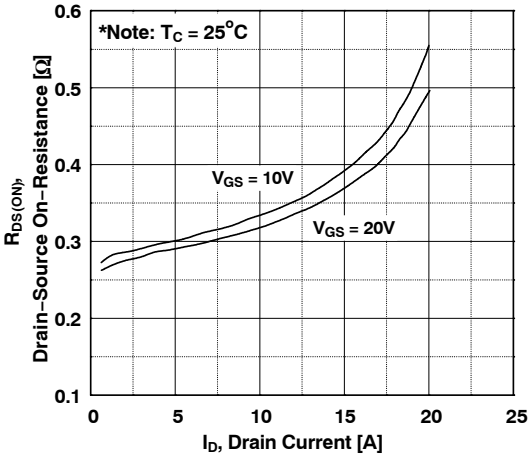


Figure 5. On−Resistance Variation vs. Drain Current and Gate Voltage

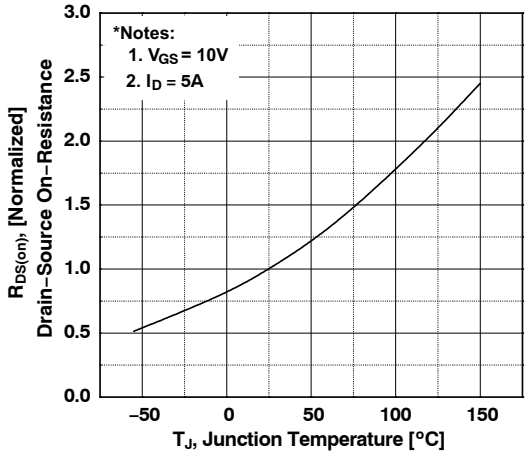


Figure 6. On−Resistance Variation vs. Temperature

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TYPICAL CHARACTERISTICS

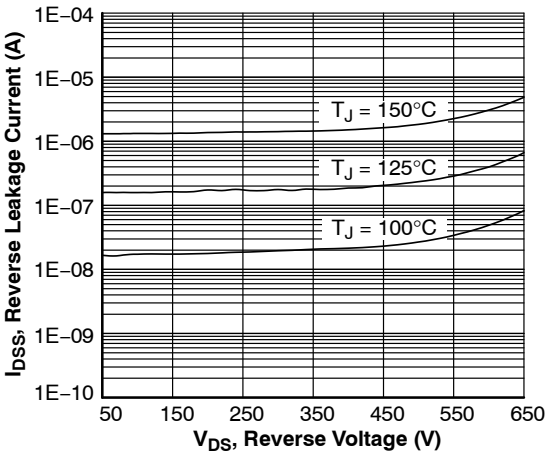


Figure 7. Drain−to−Source Leakage Current vs. Voltage

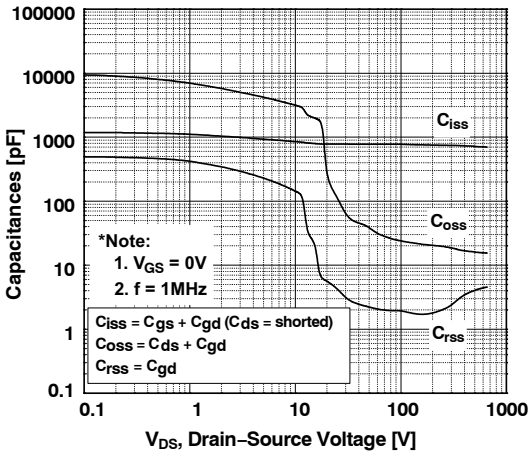


Figure 8. Capacitance Characteristics

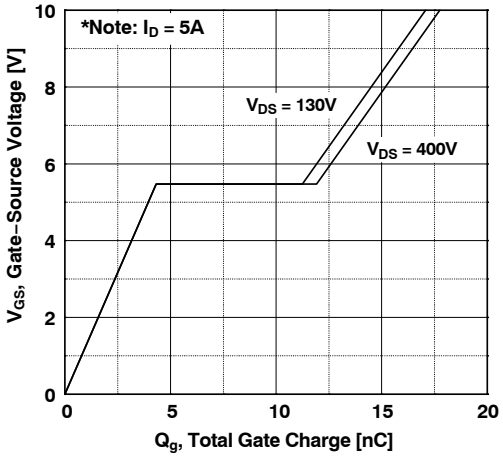


Figure 9. Gate Charge Characteristics

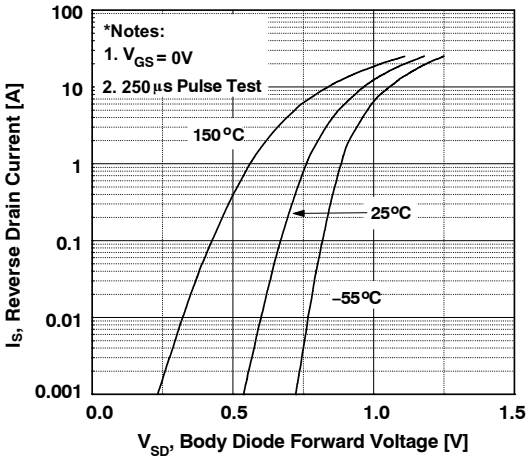


Figure 10. Body Diode Forward Voltage Variation vs. Source Current and Temperature

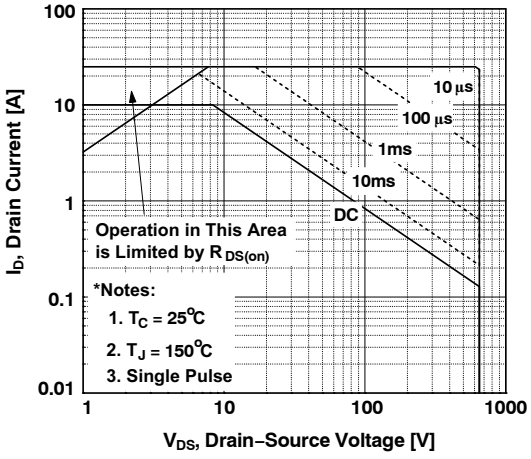


Figure 11. Maximum Safe Operating Area

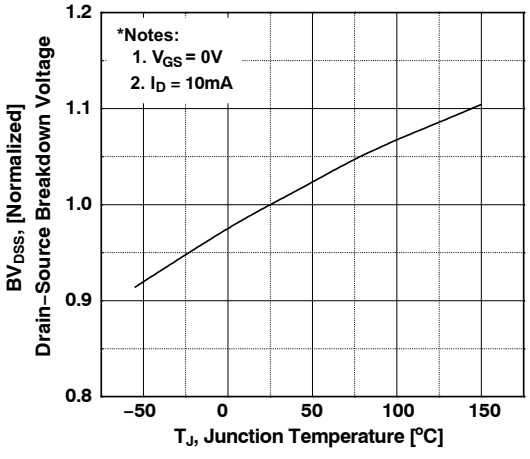


Figure 12. Breakdown Voltage Variation vs. Temperature

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TYPICAL CHARACTERISTICS

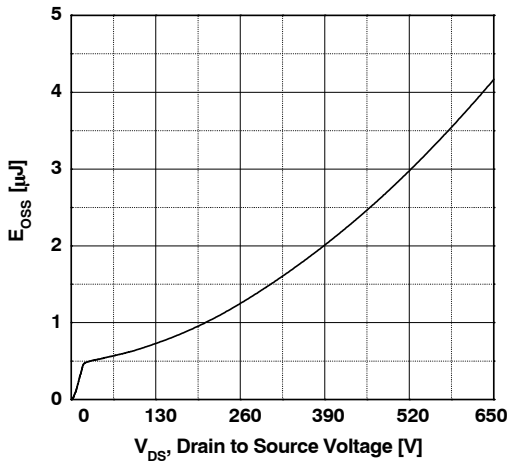


Figure 13. E_{OSS} vs. Drain to Source Voltage

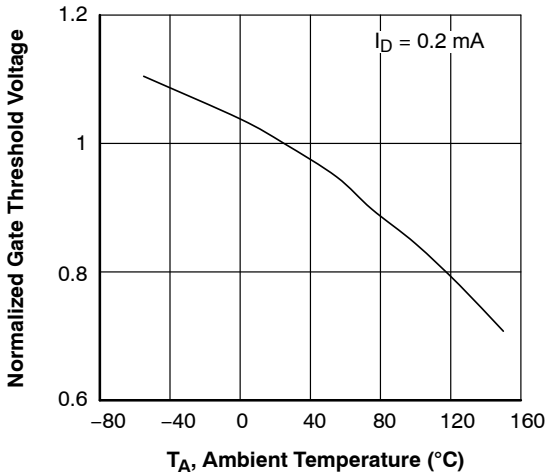


Figure 14. Normalized Gate Threshold Voltage vs. Temperature

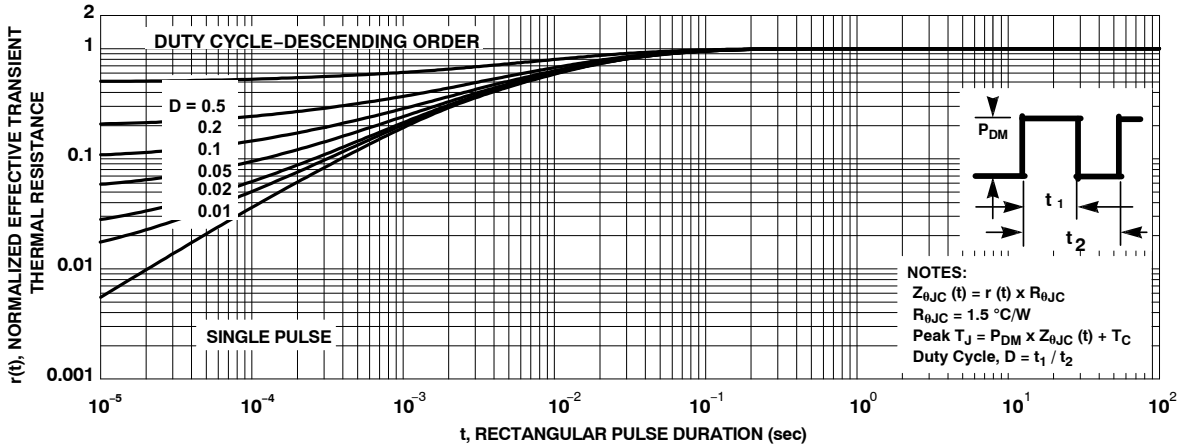


Figure 15. Transient Thermal Response Curve

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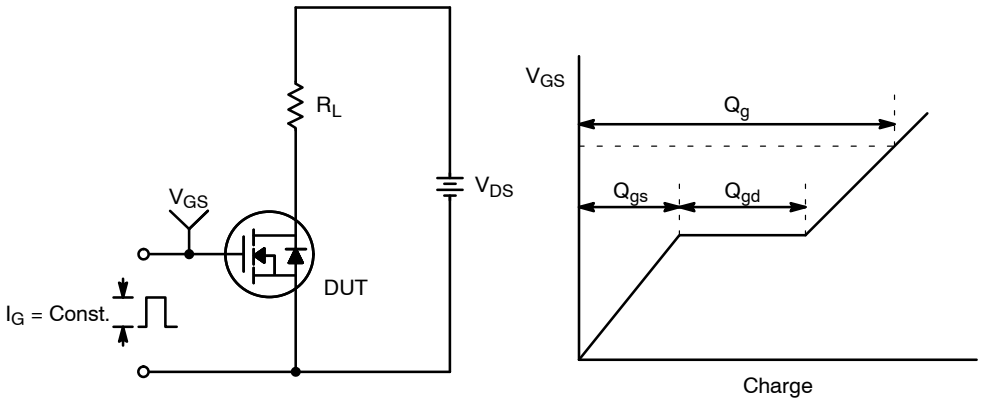


Figure 16. Gate Charge Test Circuit & Waveform

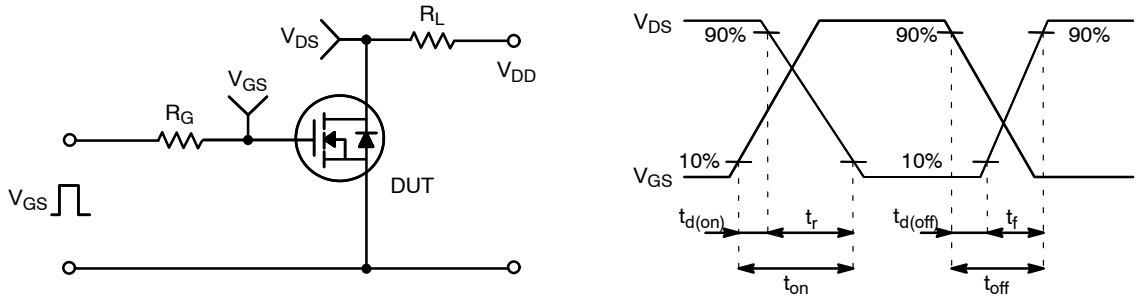


Figure 17. Resistive Switching Test Circuit & Waveforms

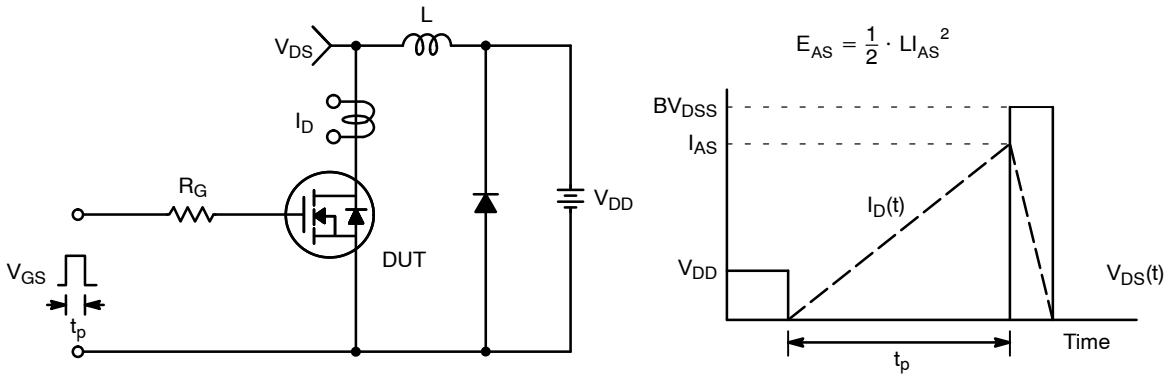


Figure 18. Unclamped Inductive Switching Test Circuit & Waveforms

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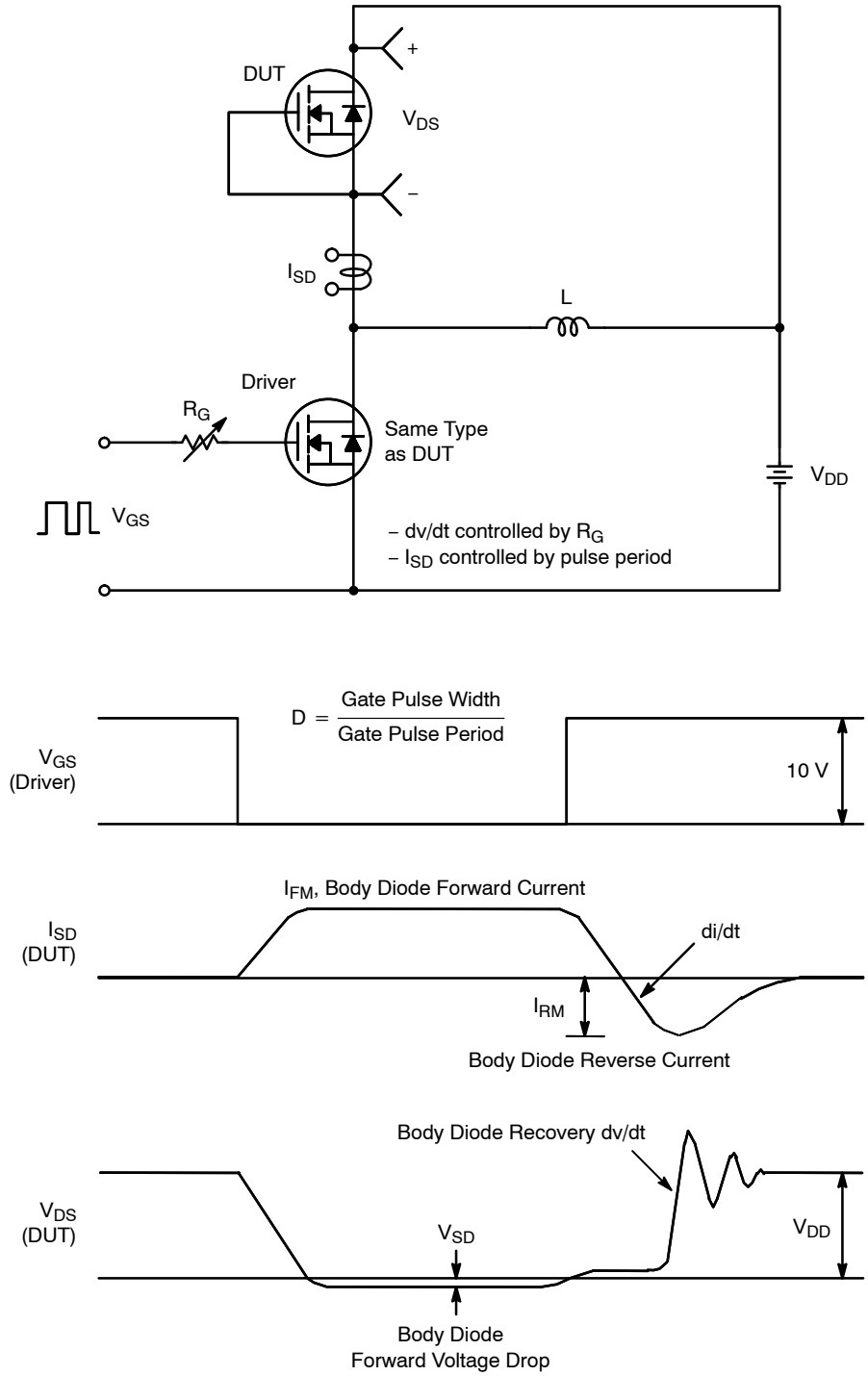
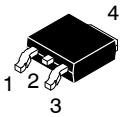


Figure 19. Peak Diode Recovery dv/dt Test Circuit & Waveforms

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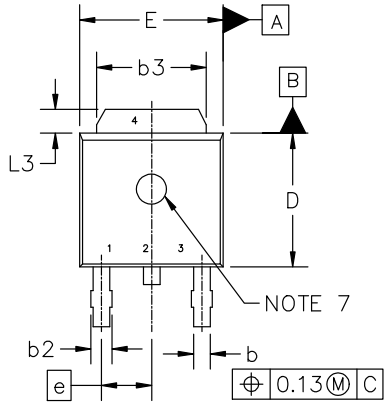
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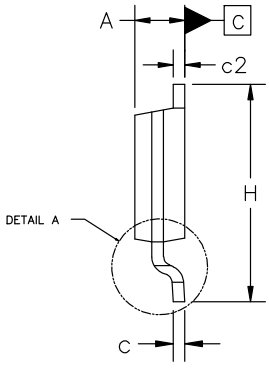
SCALE 1:1

DPAK−3 6.10x6.54x2.28, 2.29P
CASE 369C
ISSUE L

DATE 24 AUG 2026

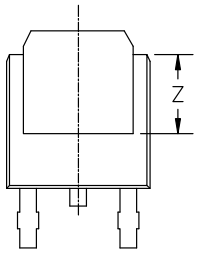


TOP VIEW

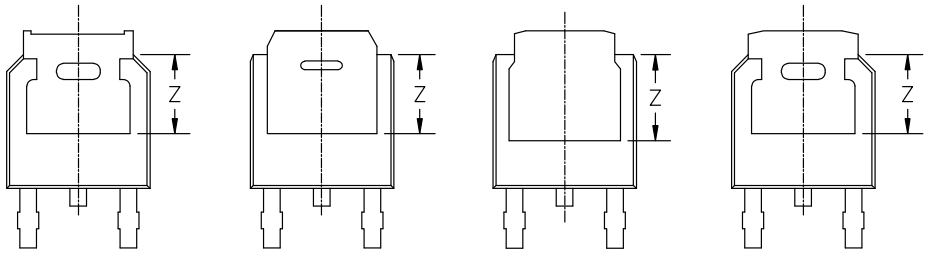


SIDE VIEW

MILLIMETERS			
DIM	MIN	NOM	MAX
A	2.18	2.28	2.38
A1	0.00	−−−	0.13
b	0.63	0.76	0.89
b2	0.72	0.93	1.14
b3	4.57	5.02	5.46
c	0.46	0.54	0.61
c2	0.46	0.54	0.61
D	5.97	6.10	6.22
E	6.35	6.54	6.73
e	2.29 BSC		
H	9.40	9.91	10.41
L	1.40	1.59	1.78
L1	2.90 REF		
L2	0.51 BSC		
L3	0.89	−−−	1.27
L4	−−−	−−−	1.01
Z	3.93	−−−	−−−



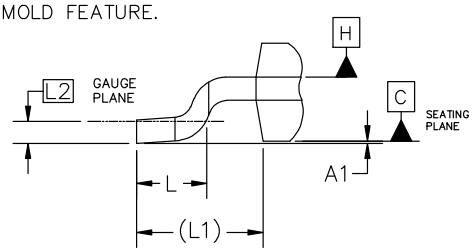
BOTTOM VIEW



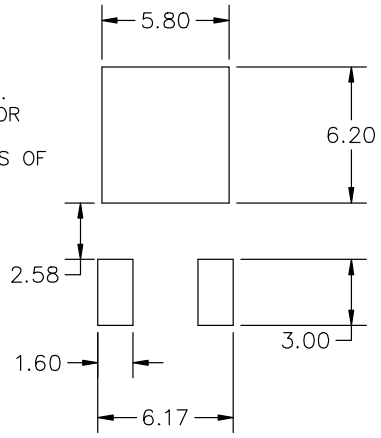
ALTERNATE CONSTRUCTIONS

NOTES:

1. DIMENSIONING AND TOLERANCING ASME Y14.5M, 2018.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. THERMAL PAD CONTOUR OPTIONAL WITHIN DIMENSIONS b3, L3, AND Z.
4. DIMENSIONS D AND E DO NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR BURRS.
5. DIMENSIONS D AND E ARE DETERMINED AT THE OUTERMOST EXTREMES OF THE PLASTIC BODY.
6. DATUMS A AND B ARE DETERMINED AT DATUM PLANE H.
7. OPTIONAL MOLD FEATURE.



DETAIL A
ROTATED 90° CW



RECOMMENDED MOUNTING FOOTPRINT*
*For additional information on our Pb−Free strategy and soldering details, please download the onsemi Soldering and Mounting Techniques reference manual, SOLDERRM/D.

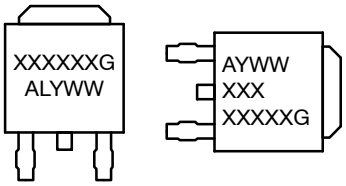
DOCUMENT NUMBER:	**98AON10527D**	Electronic versions are uncontrolled except when accessed directly from the Document Repository. Printed versions are uncontrolled except when stamped "CONTROLLED COPY" in red.
DESCRIPTION:	**DPAK−3 6.10x6.54x2.28, 2.29P**	**PAGE 1 OF 2**

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DPAK−3 6.10x6.54x2.28, 2.29P
CASE 369C
ISSUE L

DATE 24 AUG 2026

GENERIC MARKING DIAGRAM*



IC **Discrete**

XXXXXX	= Device Code
A	= Assembly Location
L	= Wafer Lot
Y	= Year
WW	= Work Week
G	= Pb−Free Package

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, “G” or microdot “▪”, may or may not be present. Some products may not follow the Generic Marking.

STYLE 1:
PIN 1. BASE
2. COLLECTOR
3. EMITTER
4. COLLECTOR

STYLE 2:
PIN 1. GATE
2. DRAIN
3. SOURCE
4. DRAIN

STYLE 3:
PIN 1. ANODE
2. CATHODE
3. ANODE
4. CATHODE

STYLE 4:
PIN 1. CATHODE
2. ANODE
3. GATE
4. ANODE

STYLE 5:
PIN 1. GATE
2. ANODE
3. CATHODE
4. ANODE

STYLE 6:
PIN 1. MT1
2. MT2
3. GATE
4. MT2

STYLE 7:
PIN 1. GATE
2. COLLECTOR
3. EMITTER
4. COLLECTOR

STYLE 8:
PIN 1. N/C
2. CATHODE
3. ANODE
4. CATHODE

STYLE 9:
PIN 1. ANODE
2. CATHODE
3. RESISTOR ADJUST
4. CATHODE

STYLE 10:
PIN 1. CATHODE
2. ANODE
3. CATHODE
4. ANODE

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