ON Semiconductor

Is Now



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MOSFET - Power, Single N-Channel, Shielded Gate, PowerTrench®

120 V, 53 mΩ, 4.8 A

NVLJS053N12MCL

ON Semiconductor®

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$V_{(BR)DSS}$	$R_{DS(on)}$ MAX	I_D MAX
120 V	53 mΩ @ 10 V	4.8 A
	70 mΩ @ 4.5 V	

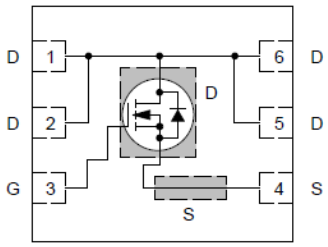
Features

- Shielded Gate MOSFET Technology
- 50% Lower Q_{rr} than Other MOSFET Suppliers
- Lowers Switching Noise/EMI
- Low Profile – 0.5 mm Maximum in MicroFET 2x2 mm
- 100% UIL Tested
- AEC−Q101 Qualified and PPAP Capable
- These Devices are Pb−Free and are RoHS Compliant

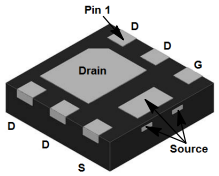
Typical Applications

- Primary DC−DC MOSFET
- Synchronous Rectifier in DC−DC and AC−DC
- Motor Drive

N−CHANNEL MOSFET



(Top View)



UDFN6
(2 X 2)
CASE 517DZ

MAXIMUM RATINGS (T_J = 25°C unless otherwise noted)

Parameter		Symbol	Value	Unit
Drain−to−Source Voltage		V_{DSS}	120	V
Gate−to−Source Voltage		V_{GS}	±20	V
Continuous Drain Current (Note 1)	T_A = 25°C	I_D	4.8	A
Power Dissipation (Note 1)	T_A = 25°C	P_D	2.3	W
Power Dissipation (Note 2)	T_A = 25°C	P_D	0.62	W
Pulsed Drain Current (Note 3)	T_A = 25°C	I_{DM}	86	A
Operating Junction and Storage Temperature Range		T_J, T_{stg}	−55 to +175	°C
Single Pulse Drain−to−Source Avalanche Energy ($I_{L(pk)}$ = 0.8 A) (Note 4)		E_{AS}	885	mJ
Maximum Lead Temperature for Soldering Purposes (1/8″ from case for 10 s)		T_L	260	°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

THERMAL CHARACTERISTICS

Parameter	Symbol	Value	Unit
Thermal Resistance Junction−to−Ambient (Note 1)	$R_{\theta JA}$	65.6	°C/W
Thermal Resistance Junction−to−Ambient (Note 2)	$R_{\theta JA}$	200	°C/W

1. Surface mounted on a FR−4 board using 1 in^2 pad of 2 oz copper.
2. Surface mounted on a FR−4 board using the minimum recommended pad of 2 oz copper.
3. Pulsed ID please refer to Figure 11 SOA graph for more details
4. E_{AS} of 886 mJ is based on starting T_J = 25°C; L = 1 mH, I_{AS} = 0.8 A, V_{DD} = 120 V, V_{GS} = 10 V.

MARKING DIAGRAM



AA = Specific Device Code
M = One Digit Date Code
▪ = Pb−Free Package

(Note: Microdot may be in either location)

ORDERING INFORMATION

See detailed ordering, marking and shipping information in the package dimensions section on page 5 of this data sheet.

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ELECTRICAL CHARACTERISTICS (T_J = 25°C unless otherwise noted)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
OFF CHARACTERISTICS						
Drain−to−Source Breakdown Voltage	$V_{(BR)DSS}$	V_{GS} = 0 V, I_D = 250 μA	120			V
Drain−to−Source Breakdown Voltage Temperature Coefficient	$V_{(BR)DSS}/T_J$	I_D = 250 μA, referenced to 25°C		55		mV/°C
Zero Gate Voltage Drain Current	I_{DSS}	V_{GS} = 0 V, V_{DS} = 120 V, T_J = 25°C			1	μA
Gate−to−Source Leakage Current	I_{GSS}	V_{GS} = ±20 V, V_{DS} = 0 V			±100	nA
ON CHARACTERISTICS (Note 5)						
Gate Threshold Voltage	$V_{GS(TH)}$	V_{GS} = V_{DS}, I_D = 30 μA	1.0	1.5	3.0	V
Gate Threshold Temperature Coefficient	$V_{GS(TH)}/T_J$	V_{GS} = V_{DS}, I_D = 30 μA		−4.4		mV/°C
Drain−to−Source On Resistance	$R_{DS(on)}$	V_{GS} = 10 V, I_D = 5.2 A, T_J = 25°C		42	53	mΩ
		V_{GS} = 4.5 V, I_D = 4.5 A, T_J = 25°C		55	70	mΩ
CHARGES, CAPACITANCES & GATE RESISTANCE						
Input Capacitance	C_{ISS}	V_{GS} = 0 V, f = 1 MHz, V_{DS} = 60 V		520		pF
Output Capacitance	C_{OSS}			190		
Reverse Transfer Capacitance	C_{RSS}			1.8		
Gate−Resistance	R_G			2.0	3.0	Ω
Total Gate Charge	$Q_{G(TOT)}$	V_{GS} = 10 V, V_{DS} = 60 V, I_D = 5.2 A		7.8		nC
4.5 V Gate Charge	$Q_{G(4.5V)}$			3.8		
Gate−to−Source Charge	Q_{GS}			1.5		
Gate−to−Drain Charge	Q_{GD}			1.0		
Output Charge	Q_{OSS}	V_{GS} = 0 V, V_{DD} = 60 V		17		nC
Total Gate Charge Sync	Q_{SYNC}	V_{DS} = 0 V, V_{GS} = 0 ~ 10 V		6.7		nC
RESISTIVE SWITCHING CHARACTERISTICS (Note 6)						
Turn−On Delay Time	$t_{d(on)}$	V_{GS} = 10 V, V_{DS} = 60 V, I_D = 5.2 A, R_G = 6 Ω		5.9		ns
Rise Time	t_r			1.6		
Turn−Off Delay Time	$t_{d(off)}$			14		
Fall Time	t_f			2.6		
DRAIN−SOURCE DIODE CHARACTERISTICS						
Forward Diode Voltage	V_{SD}	V_{GS} = 0 V, I_S = 5.2 A, T_J = 25°C		0.87	1.2	V
Reverse Recovery Time	t_{RR}	I_F = 5.2 A, dI_s/dt = 300 A/μs		25		ns
Reverse Recovery Charge	Q_{RR}			31		nC
Reverse Recovery Time	t_{RR}	I_F = 5.2 A, dI_s/dt = 1000 A/μs		15		ns
Reverse Recovery Charge	Q_{RR}			64		nC

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

5. Pulse test: pulse width ≤ 300 μs, duty ratio ≤ 2%.
6. Switching characteristics are independent of operating junction temperature

TYPICAL CHARACTERISTICS

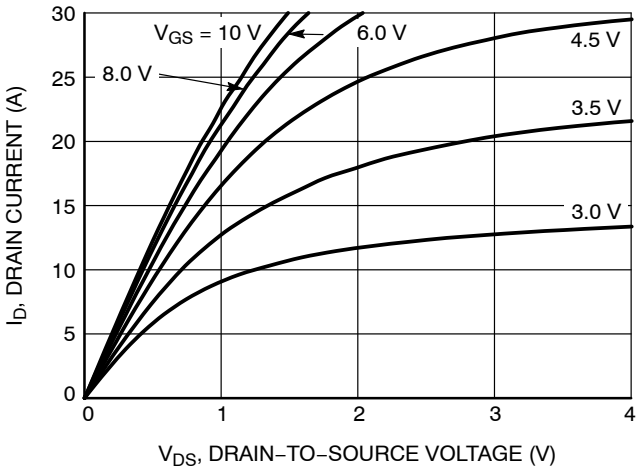


Figure 1. On−Region Characteristics

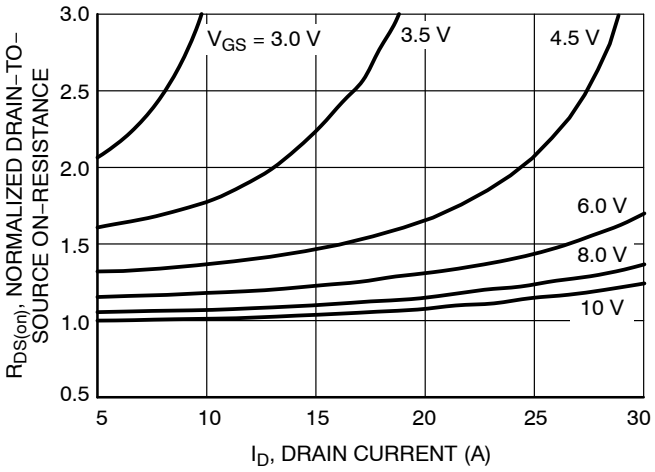


Figure 2. Normalized On−Resistance vs. Drain Current and Gate Voltage

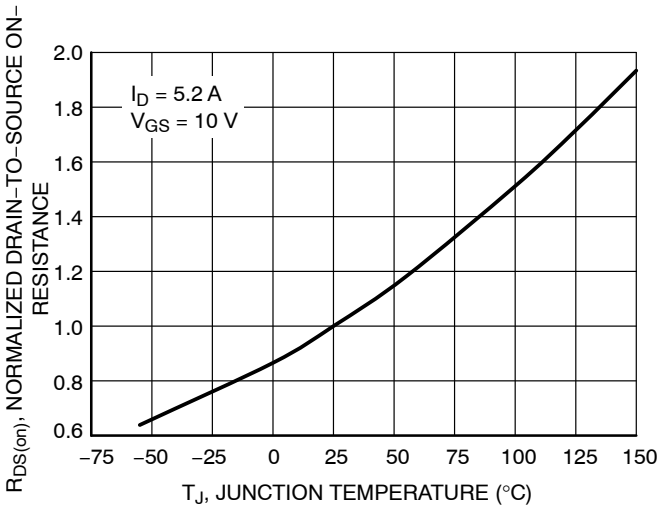


Figure 3. On−Resistance Variation with Temperature

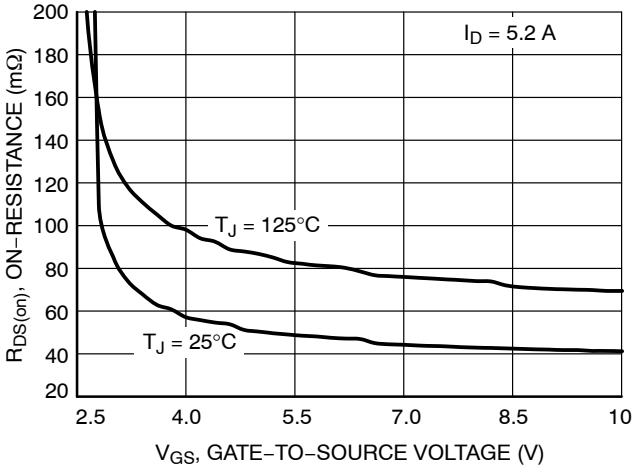


Figure 4. On−Resistance vs. Gate−to−Source Voltage

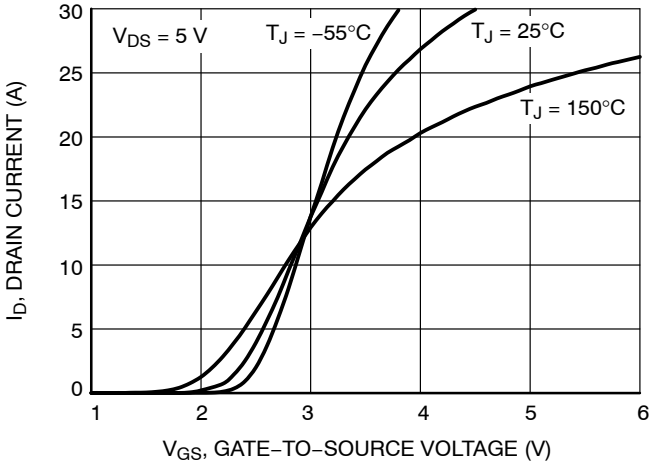


Figure 5. Transfer Characteristics

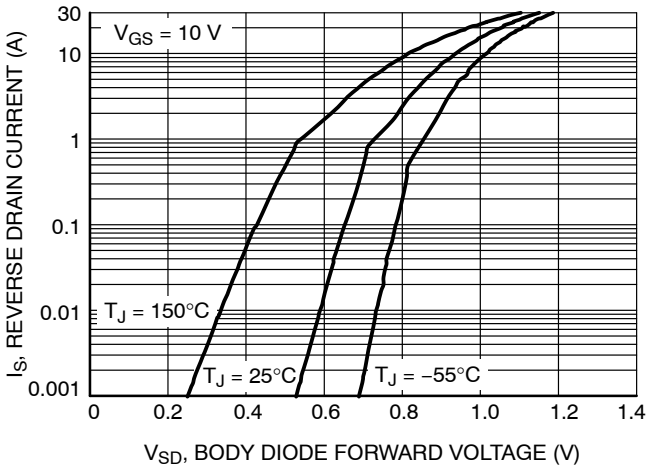


Figure 6. Diode Forward Voltage vs. Current

TYPICAL CHARACTERISTICS

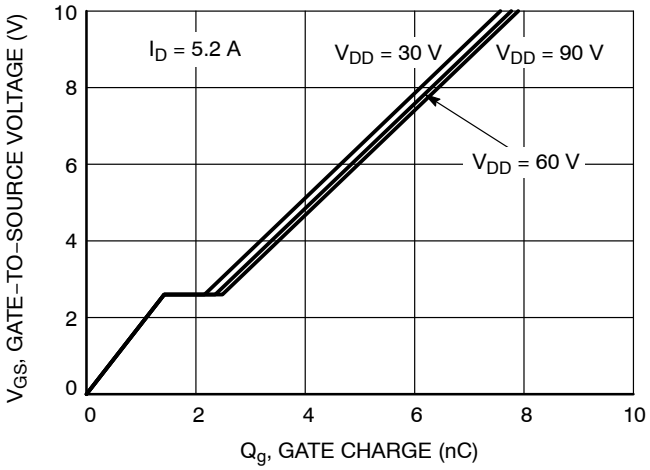


Figure 7. Gate−to−Source Voltage vs. Total Charge

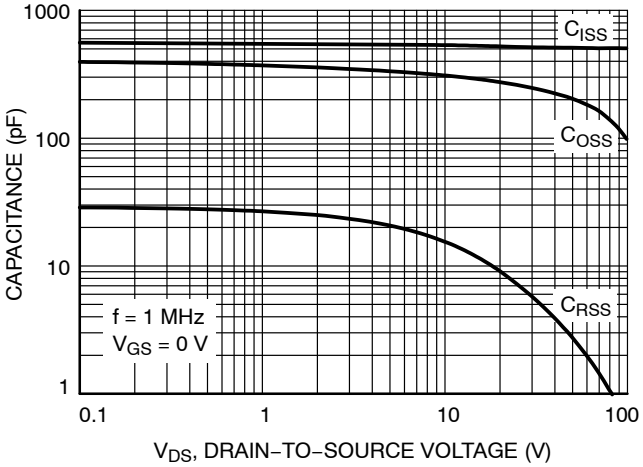


Figure 8. Capacitance vs. Drain−to−Source Voltage

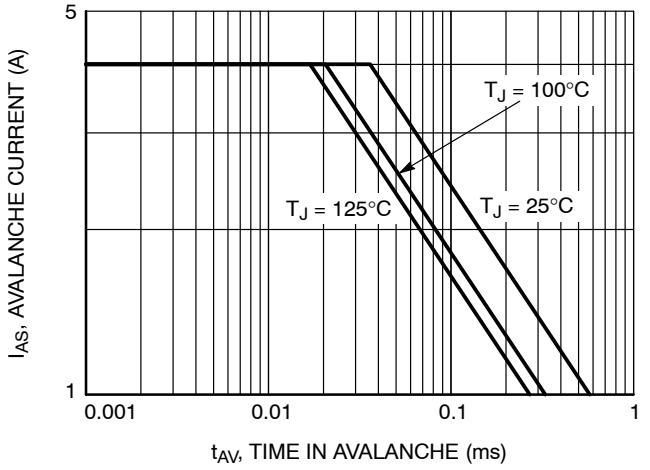


Figure 9. Unclamped Inductive Switching Capability

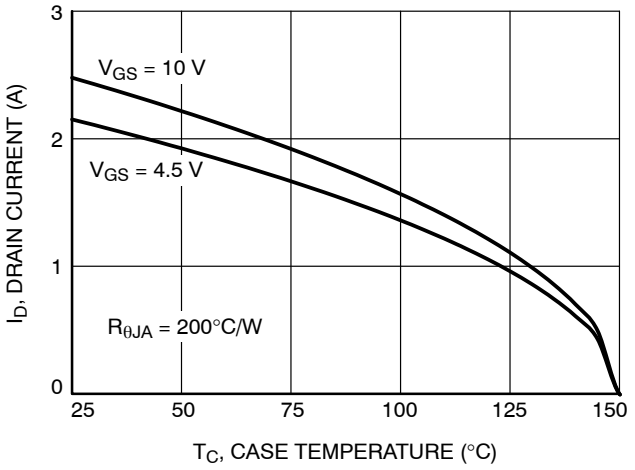


Figure 10. Maximum Continuous Drain Current vs. Case Temperature

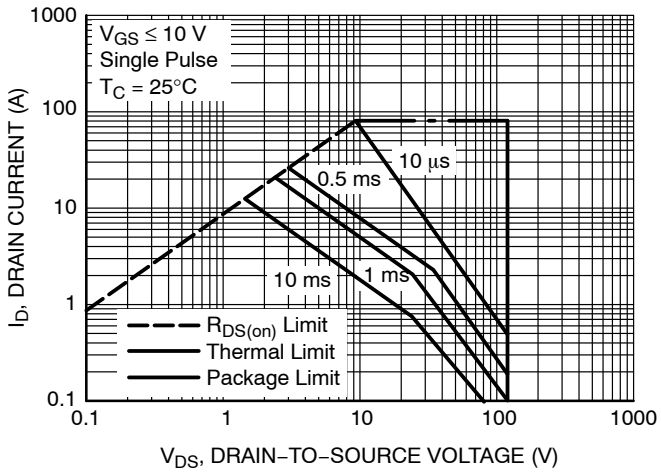


Figure 11. Safe Operating Area

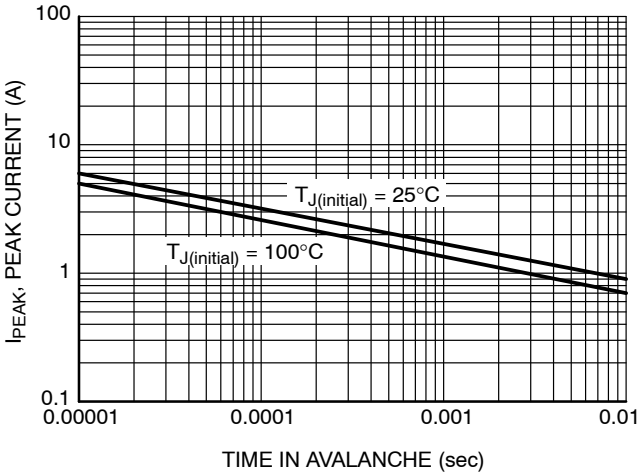


Figure 12. I_{PEAK} vs. Time in Avalanche

TYPICAL CHARACTERISTICS

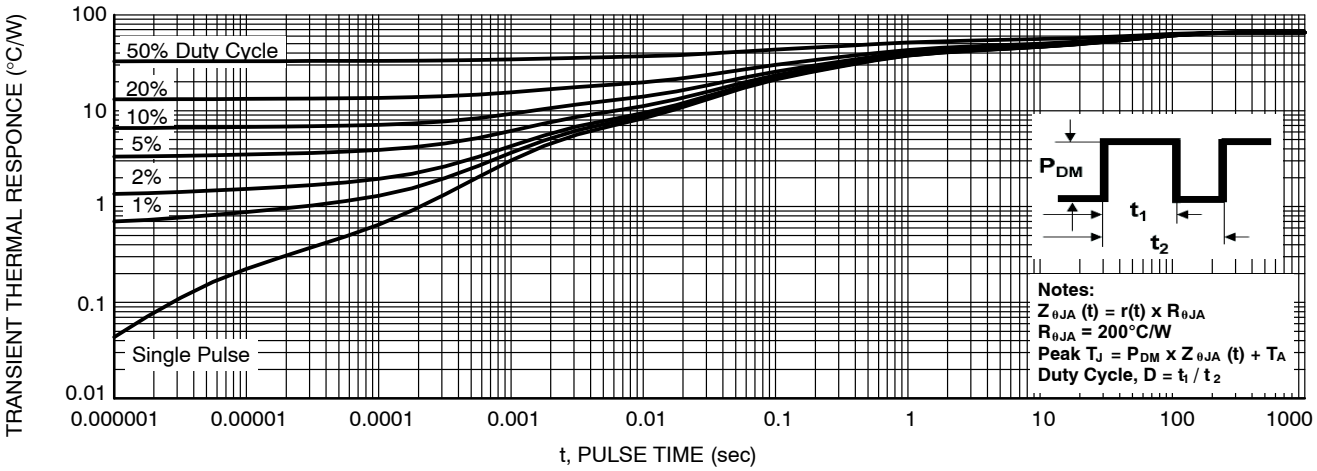


Figure 13. Transient Thermal Response Curve

DEVICE ORDERING INFORMATION

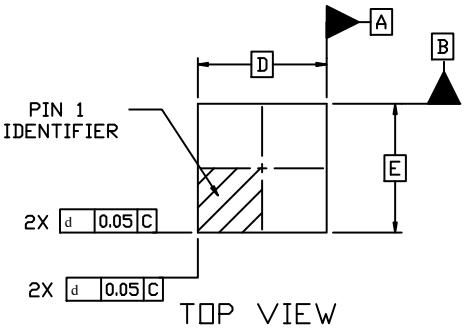
Device	Marking	Package	Shipping†
NVLJS053N12MCLTAG	AA	UDFN6 (Pb−Free)	3000 / Tape & Reel

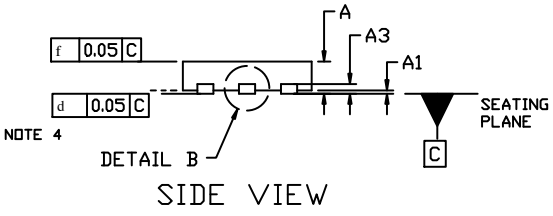
†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

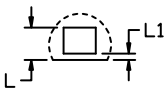
NVLJS053N12MCL

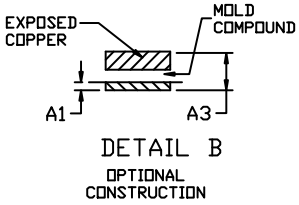
PACKAGE DIMENSIONS

UDFN6 2x2, 0.65P
CASE 517DZ
ISSUE A





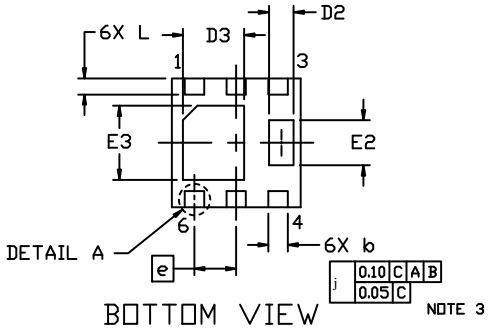


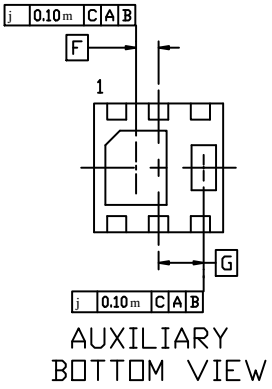


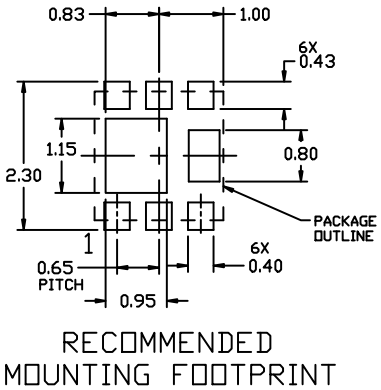
NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS
3. DIMENSION b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.15 AND 0.30 MM FROM THE TERMINAL TIP.
4. COPLANARITY APPLIES TO THE EXPOSED PADS AS WELL AS THE TERMINALS.

DIM	MILLIMETERS		
	MIN.	NOM.	MAX.
A	0.45	0.50	0.55
A1	0.00	0.025	0.05
A3		0.13 REF	
b	0.25	0.30	0.35
D	1.95	2.00	2.05
E	1.95	2.00	2.05
e		0.65 BSC	
D2	0.33	0.38	0.43
D3	0.85	0.95	1.05
E2	0.65	0.70	0.75
E3	1.05	1.15	1.25
F		0.325 BSC	
G		0.700 BSC	
L	0.20	0.25	0.30
L1	---		0.10







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