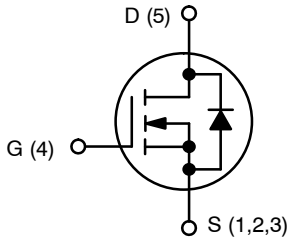
MOSFET – Power, Single N-Channel, Logic Level, DFN5/DFNW5

30 V, 0.67 mΩ, 370 A

NVMFS4C01N, NVMFS4C301N

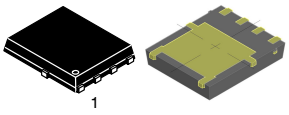
$V_{(BR)DSS}$	$R_{DS(ON)}$ MAX	I_D MAX
30 V	0.67 mΩ @ 10 V	370 A
	0.95 mΩ @ 4.5 V	



N-CHANNEL MOSFET

Features

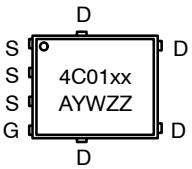
- Small Footprint (5x6 mm) for Compact Design
- Low $R_{DS(on)}$ to Minimize Conduction Losses
- Low Q_G and Capacitance to Minimize Driver Losses
- NVMFS4C01NWF – Wettable Flanks Option for Enhanced Optical Inspection
- AEC-Q101 Qualified and PPAP Capable
- These Devices are Pb-Free, Halogen Free/BFR Free and are RoHS Compliant



DFN5 (SO-8FL) CASE 488AA

DFNW5 CASE 507BE

MARKING DIAGRAM



4C01N = Specific Device Code for NVMFS4C01N
4C01WF= Specific Device Code of NVMFS4C01NWF
A = Assembly Location
Y = Year
W = Work Week
ZZ = Lot Traceabililty

MAXIMUM RATINGS (T_J = 25 °C unless otherwise noted)

Symbol	Parameter			Value	Unit
V_{DSS}	Drain-to-Source Voltage			30	V
V_{GS}	Gate-to-Source Voltage			±20	V
I_D	Continuous Drain Current $R_{\theta JC}$ (Notes 1, 3)	Steady State	T_C = 25 °C	370	A
P_D	Power Dissipation $R_{\theta JC}$ (Notes 1, 3)		T_C = 25 °C	161	W
I_D	Continuous Drain Current $R_{\theta JA}$ (Notes 1, 2, 3)	Steady State	T_A = 25 °C	57	A
P_D	Power Dissipation $R_{\theta JA}$ (Notes 1, 2, 3)		T_A = 25 °C	3.84	W
I_{DM}	Pulsed Drain Current	T_A = 25 °C, t_p = 10 μs		900	A
T_J, T_{stg}	Operating Junction and Storage Temperature			−55 to 175	°C
I_S	Source Current (Body Diode)			110	A
E_{AS}	Single Pulse Drain-to-Source Avalanche Energy ($I_{L(pk)}$ = 35 A)			862	mJ
T_L	Lead Temperature for Soldering Purposes (1/8″ from case for 10 s)			260	°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

THERMAL RESISTANCE MAXIMUM RATINGS (Note 1)

Symbol	Parameter	Value	Unit
$R_{\theta JC}$	Junction-to-Case – Steady State	0.93	°C/W
$R_{\theta JA}$	Junction-to-Ambient – Steady State (Note 2)	39	

1. The entire application environment impacts the thermal resistance values shown, they are not constants and are only valid for the particular conditions noted.
2. Surface-mounted on FR4 board using a 650 mm^2, 2 oz. Cu pad.
3. Maximum current for pulses as long as 1 second is higher but is dependent on pulse duration and duty cycle.

ORDERING INFORMATION

Device	Package	Shipping†
NVMFS4C01NT1G, NVMFS4C301NET1G	DFN5 (Pb-Free)	1500 / Tape & Reel
NVMFS4C01NT3G	DFN5 (Pb-Free)	5000 / Tape & Reel
NVMFS4C01NWFT1G, NVMFS4C301NWFET1G	DFNW5 (Pb-Free)	1500 / Tape & Reel

DISCONTINUED (Note 1)

NVMFS4C01NWFT3G	DFNW5 (Pb-Free)	5000 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specification Brochure, BRD8011/D.

1. **DISCONTINUED:** These devices are not recommended for new design. Please contact your **onsemi** representative for information. The most current information on these devices may be available on www.onsemi.com.

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ELECTRICAL CHARACTERISTICS (T_J = 25 °C unless otherwise specified)

Symbol	Parameter	Test Condition		Min	Typ	Max	Unit
OFF CHARACTERISTICS							
$V_{(BR)DSS}$	Drain-to-Source Breakdown Voltage	V_{GS} = 0 V, I_D = 250 μA		30			V
$V_{(BR)DSS}/T_J$	Drain-to-Source Breakdown Voltage Temperature Coefficient				16.3		mV/°C
I_{DSS}	Zero Gate Voltage Drain Current	V_{GS} = 0 V, V_{DS} = 24 V	T_J = 25 °C			1	μA
			T_J = 125 °C			100	
I_{GSS}	Gate-to-Source Leakage Current	V_{DS} = 0 V, V_{GS} = 20 V				100	nA
ON CHARACTERISTICS (Note 4)							
$V_{GS(TH)}$	Gate Threshold Voltage	V_{GS} = V_{DS}, I_D = 250 μA		1.3		2.2	V
$V_{GS(TH)}/T_J$	Negative Threshold Temperature Coefficient				5.8		mV/°C
$R_{DS(on)}$	Drain-to-Source On Resistance	V_{GS} = 10 V	I_D = 30 A		0.56	0.67	mΩ
		V_{GS} = 4.5 V	I_D = 30 A		0.76	0.95	
g_{FS}	Forward Transconductance	V_{DS} = 3 V, I_D = 30 A			183		S
R_G	Gate Resistance	T_A = 25 °C			1.0		Ω
CHARGES AND CAPACITANCES							
C_{ISS}	Input Capacitance	V_{GS} = 0 V, f = 1 MHz, V_{DS} = 15 V			10144		pF
C_{OSS}	Output Capacitance				5073		
C_{RSS}	Reverse Transfer Capacitance				148		
$Q_{G(TOT)}$	Total Gate Charge	V_{GS} = 4.5 V, V_{DS} = 15 V; I_D = 30 A			63		nC
$Q_{G(TH)}$	Threshold Gate Charge				18		
Q_{GS}	Gate-to-Source Charge				29		
Q_{GD}	Gate-to-Drain Charge				13		
$Q_{G(TOT)}$	Total Gate Charge	V_{GS} = 10 V, V_{DS} = 15 V, I_D = 30 A			139		nC
SWITCHING CHARACTERISTICS (Note 5)							
$t_{d(ON)}$	Turn-On Delay Time	V_{GS} = 4.5 V, V_{DS} = 15 V, I_D = 15 A, R_G = 3.0 Ω			29		ns
t_r	Rise Time				68		
$t_{d(OFF)}$	Turn-Off Delay Time				53		
t_f	Fall Time				36		
DRAIN-SOURCE DIODE CHARACTERISTICS							
V_{SD}	Forward Diode Voltage	V_{GS} = 0 V, I_S = 10 A	T_J = 25 °C		0.73	1.1	V
			T_J = 125 °C		0.55		
t_{RR}	Reverse Recovery Time	V_{GS} = 0 V, dI_S/dt = 100 A/μs, I_S = 30 A			87		ns
t_a	Charge Time				43		
t_b	Discharge Time				44		
Q_{RR}	Reverse Recovery Charge				147		nC

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

4. Pulse Test: pulse width ≤ 300 μs, duty cycle ≤ 2%.
5. Switching characteristics are independent of operating junction temperatures.

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TYPICAL CHARACTERISTICS

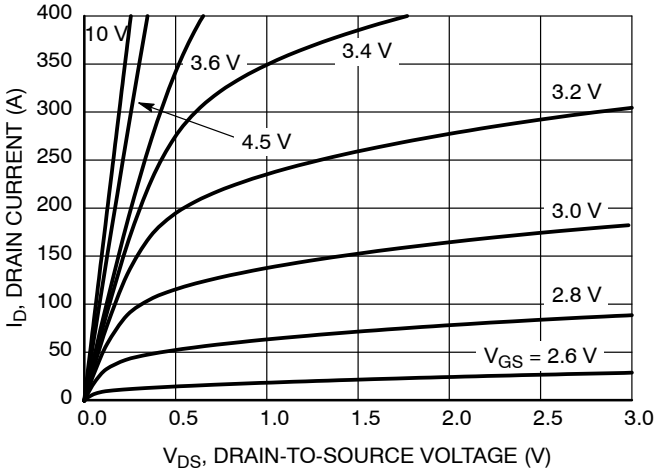


Figure 1. On-Region Characteristics

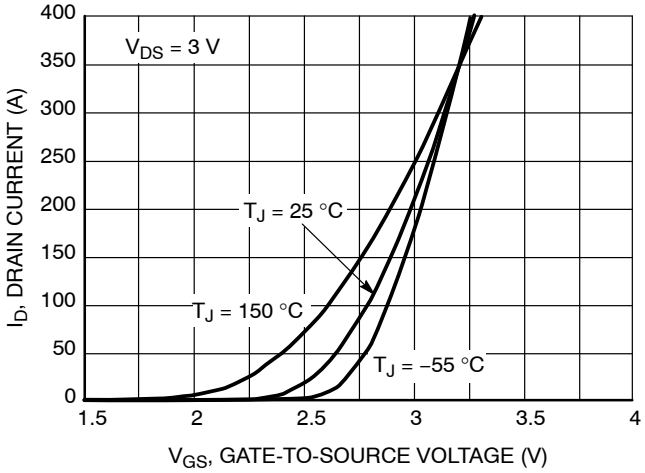


Figure 2. Transfer Characteristics

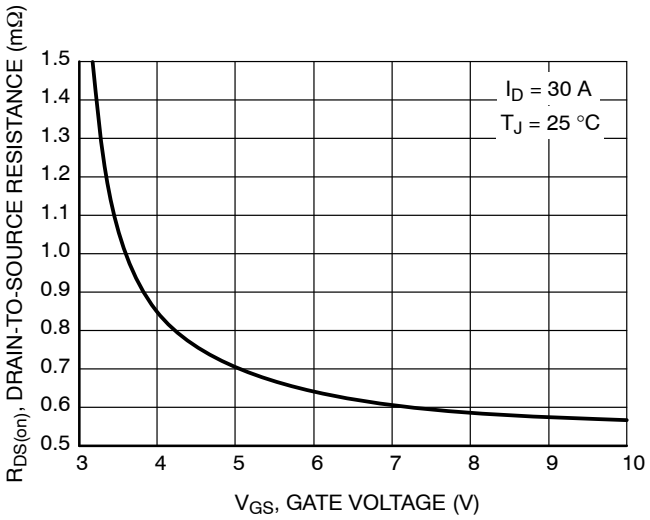


Figure 3. On-Resistance vs. Gate-to-Source Voltage

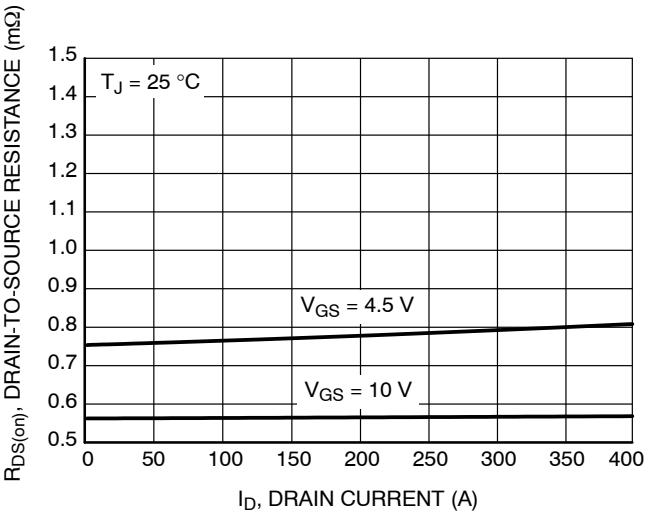


Figure 4. On-Resistance vs. Drain Current and Gate Voltage

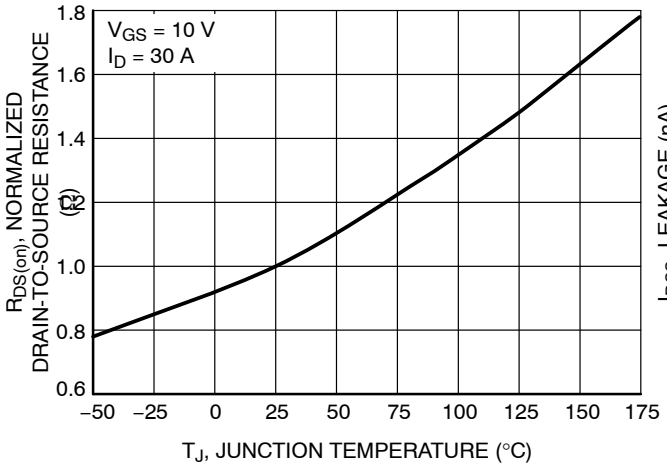


Figure 5. On-Resistance Variation with Temperature

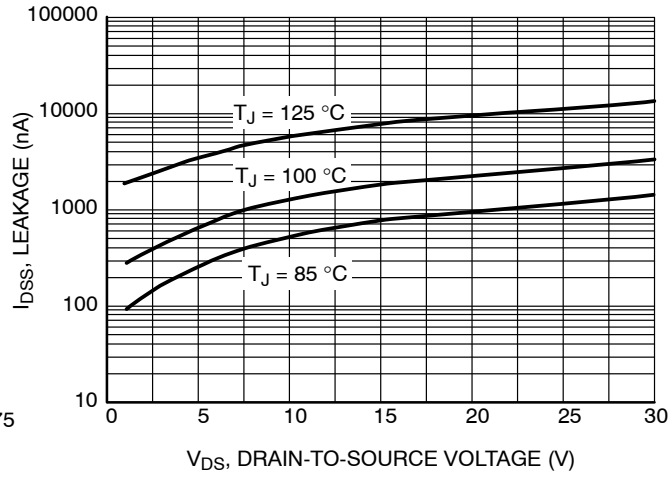


Figure 6. Drain-to-Source Leakage Current vs. Voltage

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TYPICAL CHARACTERISTICS (continued)

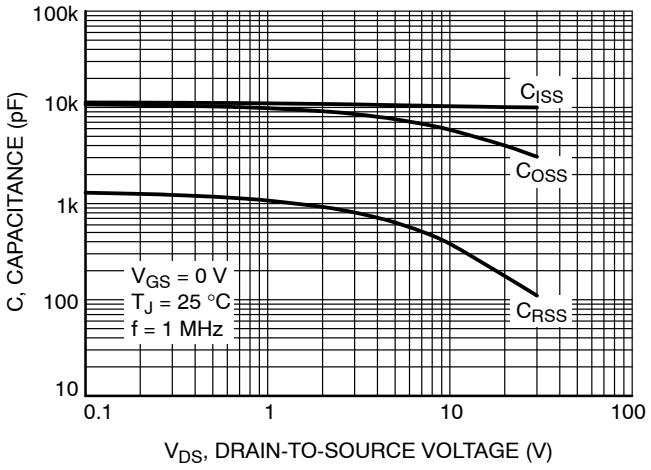


Figure 7. Capacitance Variation

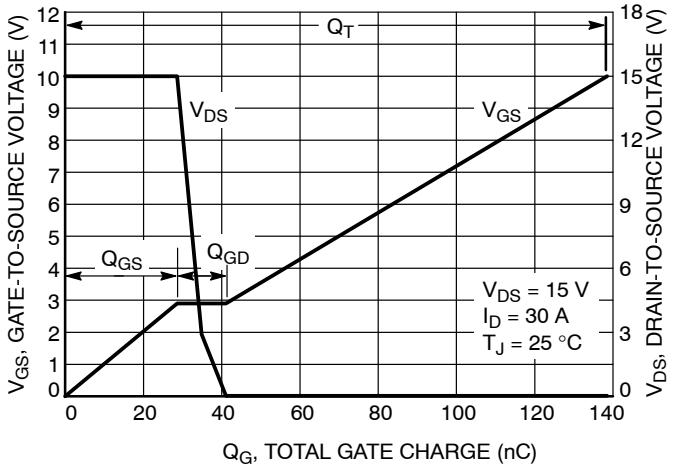


Figure 8. Gate-to-Source and Drain-to-Source Voltage vs. Total Charge

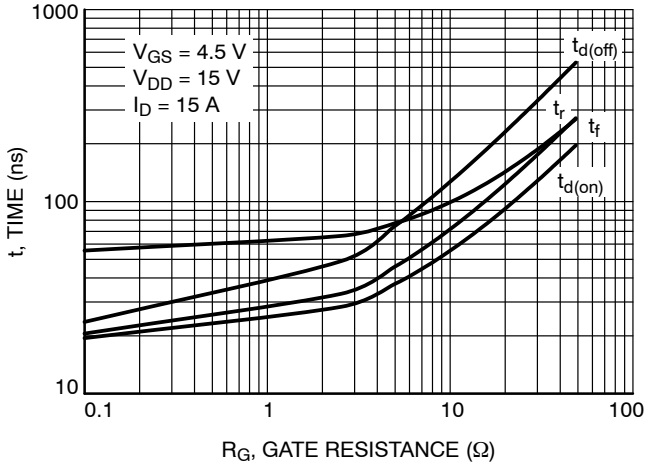


Figure 9. Resistive Switching Time Variation vs. Gate Resistance

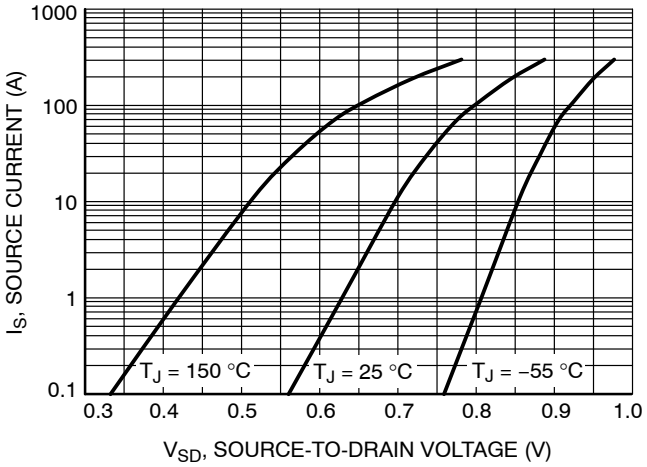


Figure 10. Diode Forward Voltage vs. Current

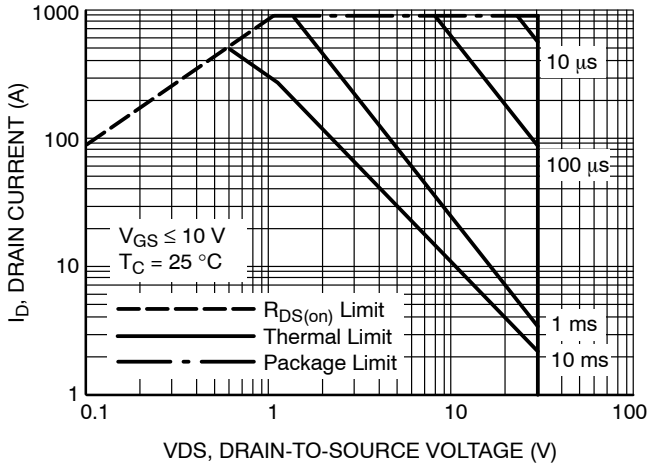


Figure 11. Maximum Rated Forward Biased Safe Operating Area

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TYPICAL CHARACTERISTICS (continued)

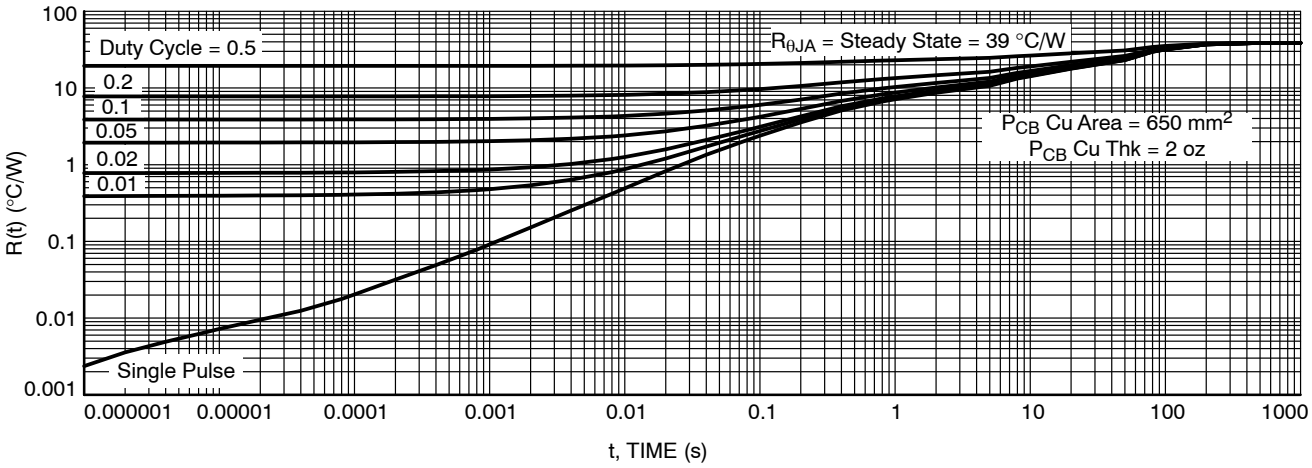


Figure 12. Thermal Impedance (Junction-to-Ambient)

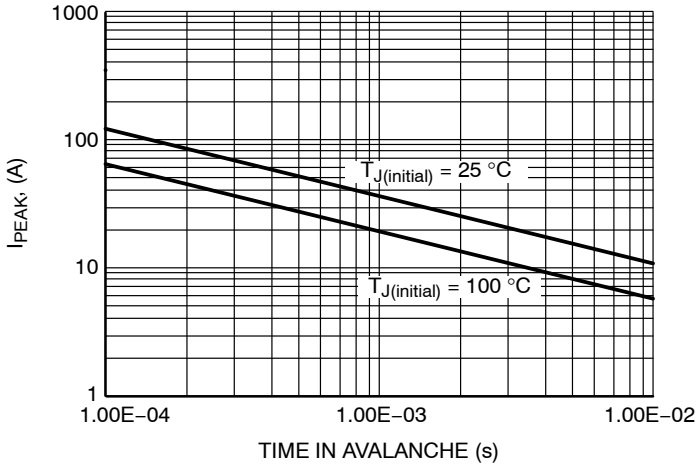


Figure 13. Avalanche Characteristics

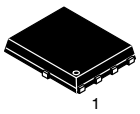
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REVISION HISTORY

Revision	Description of Changes	Date
5	Added a new device core number – NVMFS4C301N and two OPNs – NVMFS4C301NET1G, NVMFS4C301NWFET1G. Updated the main title – added DFNW5 package.	8/26/2025

This document has undergone updates prior to the inclusion of this revision history table. The changes tracked here only reflect updates made on the noted approval dates.

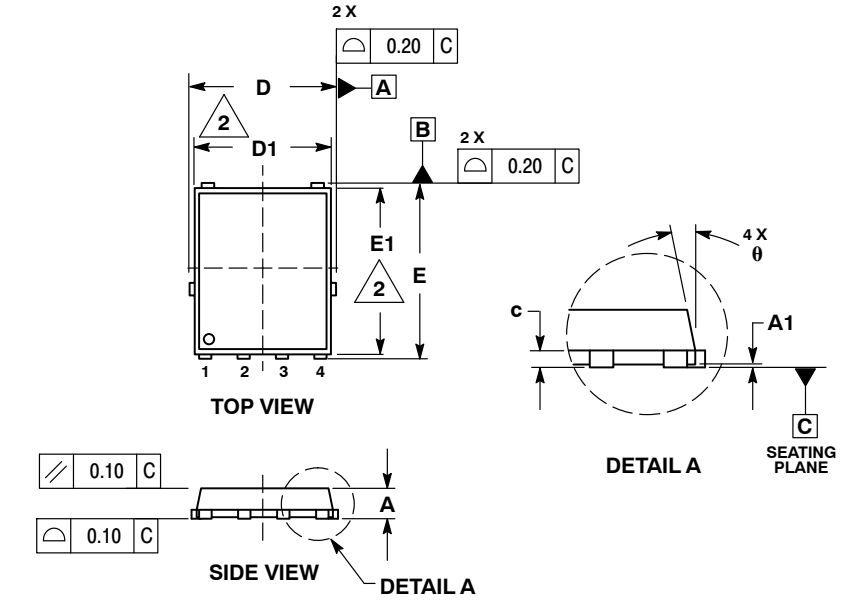
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SCALE 2:1

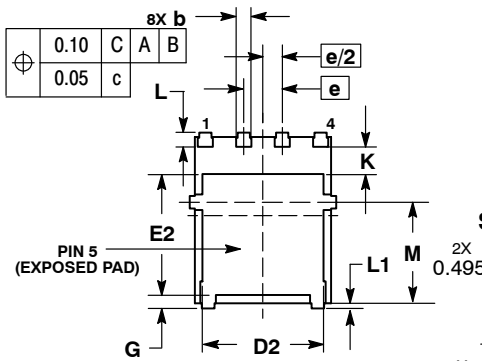
DFN5 5x6, 1.27P
(SO−8FL)
CASE 488AA
ISSUE N

DATE 25 JUN 2018

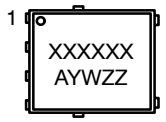


NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION D1 AND E1 DO NOT INCLUDE MOLD FLASH PROTRUSIONS OR GATE BURRS.

	MILLIMETERS		
DIM	MIN	NOM	MAX
A	0.90	1.00	1.10
A1	0.00	–––	0.05
b	0.33	0.41	0.51
c	0.23	0.28	0.33
D	5.00	5.15	5.30
D1	4.70	4.90	5.10
D2	3.80	4.00	4.20
E	6.00	6.15	6.30
E1	5.70	5.90	6.10
E2	3.45	3.65	3.85
e	1.27 BSC		
G	0.51	0.575	0.71
K	1.20	1.35	1.50
L	0.51	0.575	0.71
L1	0.125 REF		
M	3.00	3.40	3.80
θ	0 °	–––	12 °



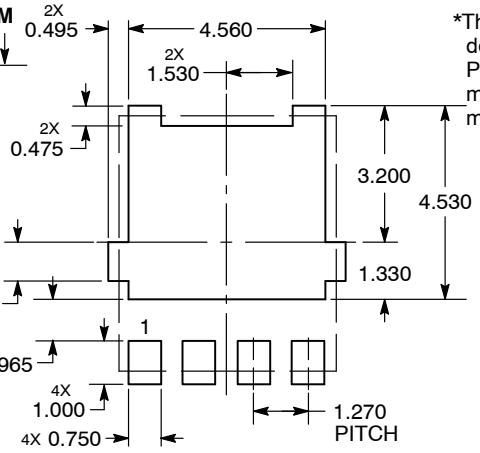
GENERIC MARKING DIAGRAM*



XXXXXX = Specific Device Code
A = Assembly Location
Y = Year
W = Work Week
ZZ = Lot Traceability

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, “G” or microdot “ ▪”, may or may not be present. Some products may not follow the Generic Marking.

RECOMMENDED SOLDERING FOOTPRINT*



DIMENSIONS: MILLIMETERS

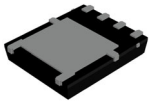
STYLE 1:
PIN 1. SOURCE
2. SOURCE
3. SOURCE
4. GATE
5. DRAIN

STYLE 2:
PIN 1. ANODE
2. ANODE
3. ANODE
4. NO CONNECT
5. CATHODE

*For additional information on our Pb−Free strategy and soldering details, please download the **onsemi** Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

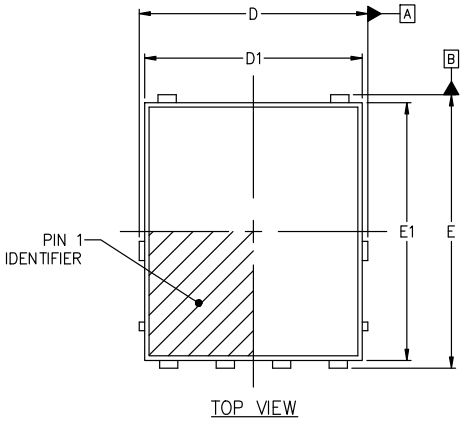
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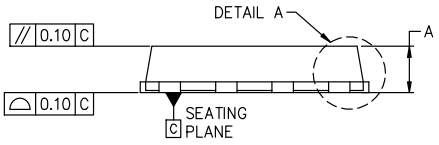
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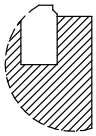


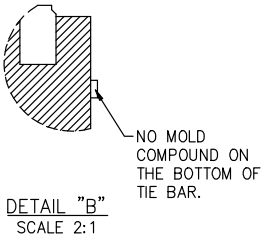
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CASE 507BE
ISSUE B

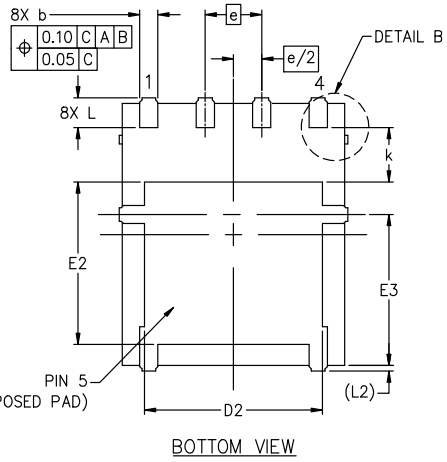
DATE 19 SEP 2024





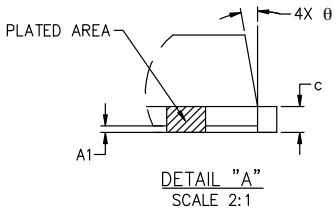




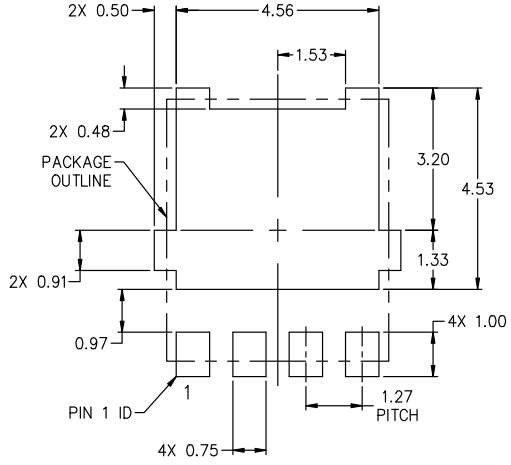


NOTES:

1. DIMENSIONING AND TOLERANCING CONFORM TO ASME Y14.5M−2018.
2. ALL DIMENSIONS ARE IN MILLIMETERS.
3. DIMENSIONS D1 AND E1 DO NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR GATE BURRS.
4. THIS PACKAGE CONTAINS WETTABLE FLANK DESIGN FEATURES TO AID IN FILLET FORMATION ON THE LEADS DURING MOUNTING.

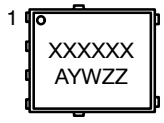


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A1	0.00	---	0.05
b	0.33	0.41	0.51
c	0.23	0.28	0.33
D	5.00	5.15	5.30
D1	4.70	4.90	5.10
D2	3.80	4.00	4.20
E	6.00	6.15	6.30
E1	5.70	5.90	6.10
E2	3.45	3.65	3.85
E3	3.00	3.40	3.80
e	1.27 BSC		
k	1.20	1.35	1.50
L	0.51	0.57	0.71
L2	0.15 REF.		
θ	0°	6°	12°



RECOMMENDED MOUNTING FOOTPRINT*
*FOR ADDITIONAL INFORMATION ON OUR Pb−FREE STRATEGY AND SOLDERING DETAILS, PLEASE DOWNLOAD THE ONSEMI SOLDERING AND MOUNTING TECHNIQUES REFERENCE MANUAL, SOLDERRM/D.

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ZZ = Lot Traceability

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, "G" or microdot " ▪", may or may not be present. Some products may not follow the Generic Marking.

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DESCRIPTION:	**DFNW5 4.90x5.90x1.00, 1.27P**	**PAGE 1 OF 1**

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