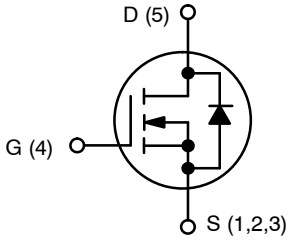
MOSFET – Power, Single N-Channel, STD Gate, SO8-FL

40 V, 0.7 mΩ, 323 A

NVMFWS0D7N04XM

$V_{(BR)DSS}$	$R_{DS(on)}$ MAX	I_D MAX
40 V	0.7 mΩ	323 A



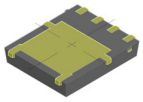
N-CHANNEL MOSFET

Features

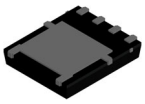
- Low $R_{DS(on)}$ to Minimize Conduction Losses
- Low Capacitance to Minimize Driver Losses
- Small Footprint (5 x 6 mm) with Compact Design
- AEC-Q101 Qualified and PPAP Capable
- These Devices are Pb-Free, Halogen Free/BFR Free and are RoHS Compliant

Applications

- Motor Drive
- Battery Protection
- Synchronous Rectification



DFNW5 (SO-8FL)
CASE 507BA



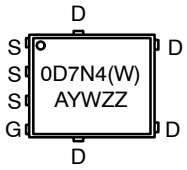
DFN-5 4.90x5.90x1.00, 1.27P
CASE 506FE

MAXIMUM RATINGS (T_J = 25 °C unless otherwise stated)

Parameter		Symbol	Value	Unit
Drain-to-Source Voltage		V_{DSS}	40	V
Gate-to-Source Voltage		V_{GS}	±20	V
Continuous Drain Current	T_C = 25 °C	I_D	323	A
	T_C = 100 °C		229	
Power Dissipation	T_C = 25 °C	P_D	134	W
Continuous Drain Current	T_A = 25 °C	I_{DA}	9.18	A
	T_A = 100 °C		6.49	
Pulsed Drain Current	T_C = 25 °C, t_p = 10 μs	I_{DM}	900	A
Pulsed Source Current (Body Diode)		I_{SM}	900	A
Operating Junction and Storage Temperature Range		T_J, T_{STG}	−55 to 175	°C
Source Current (Body Diode)		I_S	202	A
Single Pulse Avalanche Energy (I_{PK} = 21 A)		E_{AS}	987	mJ
Lead Temperature for Soldering Purposes (1/8″ from case for 10 s)		T_L	260	°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

MARKING DIAGRAM



0D7N4, 0D7N4W	= Specific Device Code
A	= Assembly Location
Y	= Year
W	= Work Week
ZZ	= Lot Traceability

ORDERING INFORMATION

See detailed ordering, marking and shipping information in the package dimensions section on page 5 of this data sheet.

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THERMAL CHARACTERISTICS

Parameter	Symbol	Value	Unit
Thermal Resistance, Junction-to-Case (Note 2)	$R_{\theta JC}$	1.11	°C/W
Thermal Resistance, Junction-to-Ambient (Notes 1, 2)	$R_{\theta JA}$	39.3	

1. Surface-mounted on FR4 board using 650 mm^2 pad, 2 oz Cu pad.
2. The entire application environment impacts the thermal resistance values shown, they are not constants and are only valid for the particular conditions noted.

ELECTRICAL CHARACTERISTICS (T_J = 25°C unless otherwise specified)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
OFF CHARACTERISTICS						
Drain-to-Source Breakdown Voltage	$V_{(BR)DSS}$	V_{GS} = 0 V, I_D = 250 μA	40			V
Drain-to-Source Breakdown Voltage Temperature Coefficient	$\Delta V_{(BR)DSS}/\Delta T_J$	I_D = 250 μA, Referenced to 25 °C		14.9		mV/°C
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = 40 V, T_J = 25 °C			1	μA
		V_{DS} = 40 V, T_J = 125 °C			40	
Gate-to-Source Leakage Current	I_{GSS}	V_{GS} = 20 V, V_{DS} = 0 V			100	nA
ON CHARACTERISTICS						
Drain-to-Source On Resistance	$R_{DS(on)}$	V_{GS} = 10 V, I_D = 50 A		0.59	0.7	mΩ
Gate Threshold Voltage	$V_{GS(TH)}$	V_{GS} = V_{DS}, I_D = 180 μA	2.5	3.0	3.5	V
Gate Threshold Voltage Temperature Coefficient	$\Delta V_{GS(TH)}/\Delta T_J$	V_{GS} = V_{DS}, I_D = 180 μA		−7.2		mV/°C
Forward Trans-conductance	g_{FS}	V_{DS} = 5 V, I_D = 50 A		244		S
CHARGES, CAPACITANCES & GATE RESISTANCE						
Input Capacitance	C_{ISS}	V_{GS} = 0 V, V_{DS} = 25 V, f = 1 MHz		4595		pF
Output Capacitance	C_{OSS}			2980		
Reverse Transfer Capacitance	C_{RSS}			41.8		
Total Gate Charge	$Q_{G(TOT)}$	V_{GS} = 10 V, V_{DD} = 32 V; I_D = 50 A		71.6		nC
Threshold Gate Charge	$Q_{G(TH)}$			13.5		
Gate-to-Source Charge	Q_{GS}			20.6		
Gate-to-Drain Charge	Q_{GD}			13		
Gate Resistance	R_G	f = 1 MHz		0.69		Ω
SWITCHING CHARACTERISTICS						
Turn-On Delay Time	$t_{d(ON)}$	V_{GS} = 0/10 V, V_{DD} = 32 V, I_D = 50 A, R_G = 0 Ω		7.33		ns
Rise Time	t_r			5.39		
Turn-Off Delay Time	$t_{d(OFF)}$			11.1		
Fall Time	t_f			4.48		
SOURCE TO DRAIN DIODE CHARACTERISTICS						
Forward Diode Voltage	V_{SD}	V_{GS} = 0 V, I_S = 50 A, T_J = 25 °C		0.81	1.2	V
		V_{GS} = 0 V, I_S = 50 A, T_J = 125 °C		0.66		
Reverse Recovery Time	t_{RR}	V_{DD} = 32 V, I_F = 36 A, dI/dt = 100 A/μs		62		ns
Charge Time	t_a			30		
Discharge Time	t_b			32		
Reverse Recovery Charge	Q_{RR}			100		nC

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

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TYPICAL CHARACTERISTICS

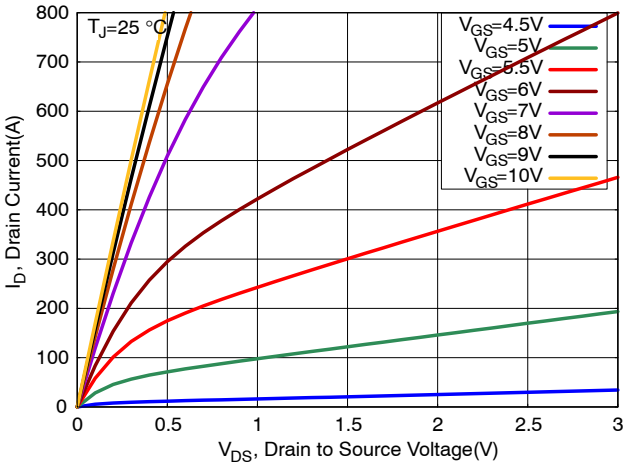


Figure 1. On-Region Characteristics

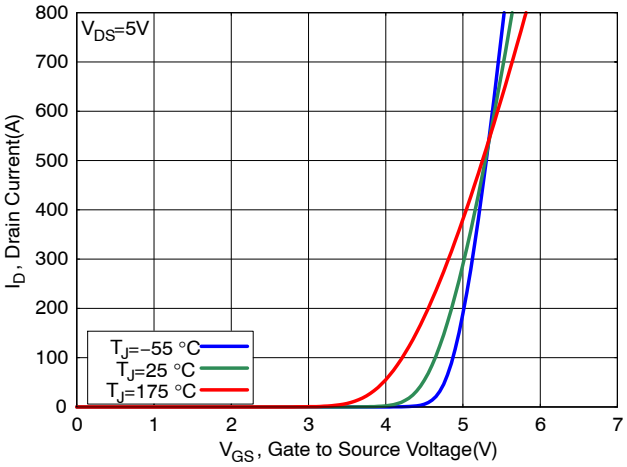


Figure 2. Transfer Characteristics

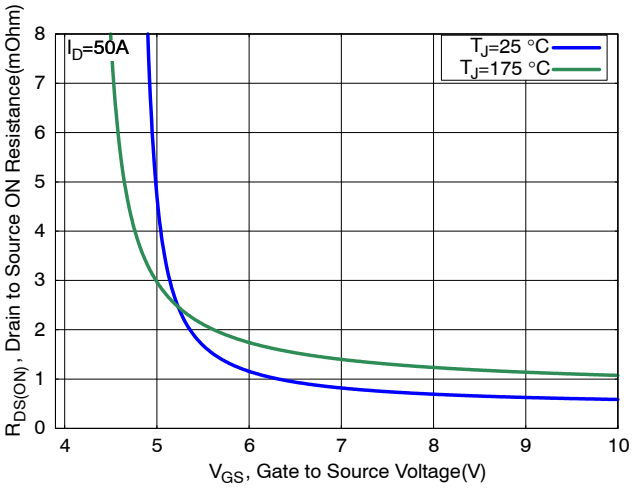


Figure 3. On-Resistance vs. Gate Voltage

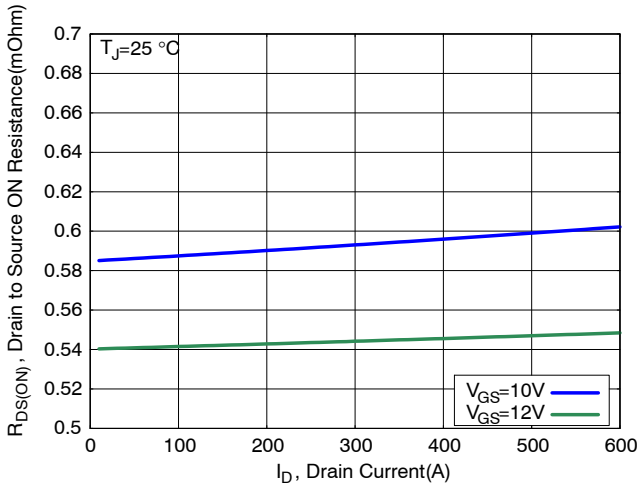


Figure 4. On-Resistance vs. Drain Current

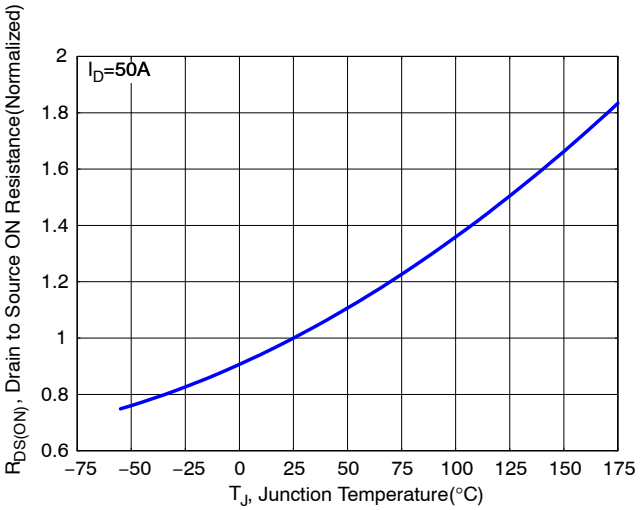


Figure 5. Normalized ON Resistance vs. Junction Temperature

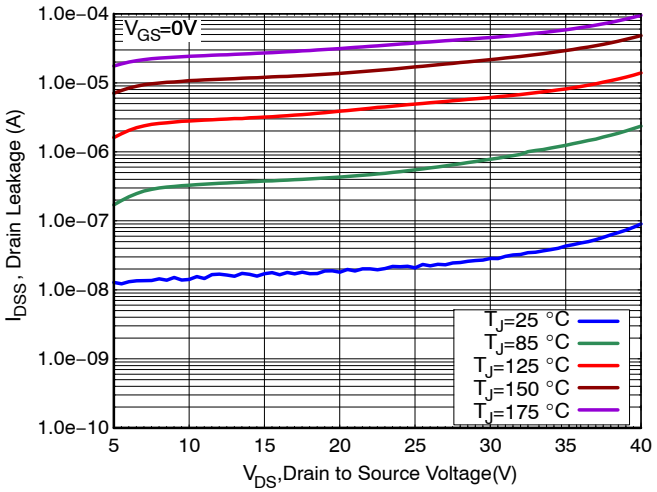


Figure 6. Drain Leakage vs. Drain-to-Source Voltage

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TYPICAL CHARACTERISTICS

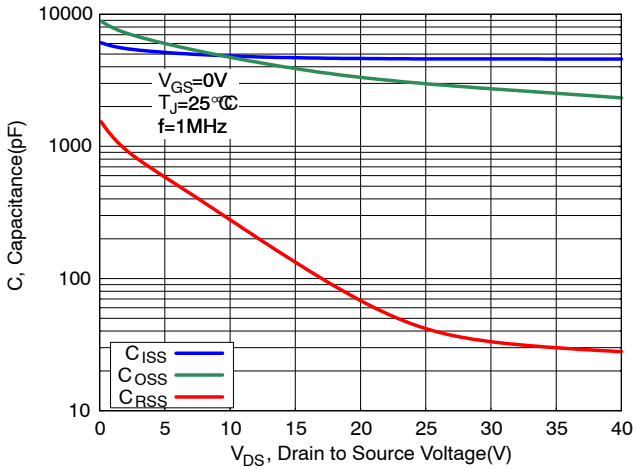


Figure 7. Capacitance Characteristics

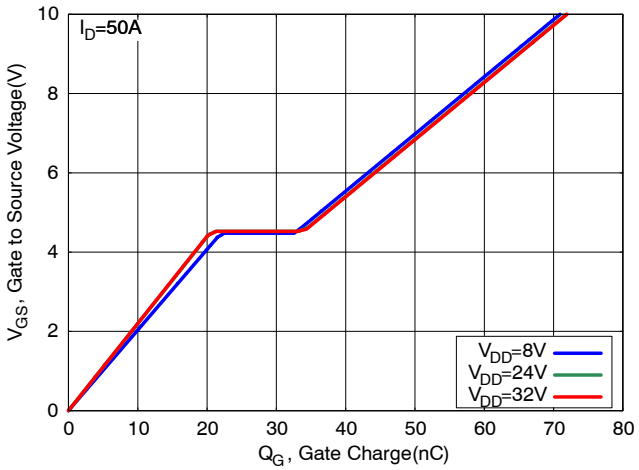


Figure 8. Gate Charge Characteristics

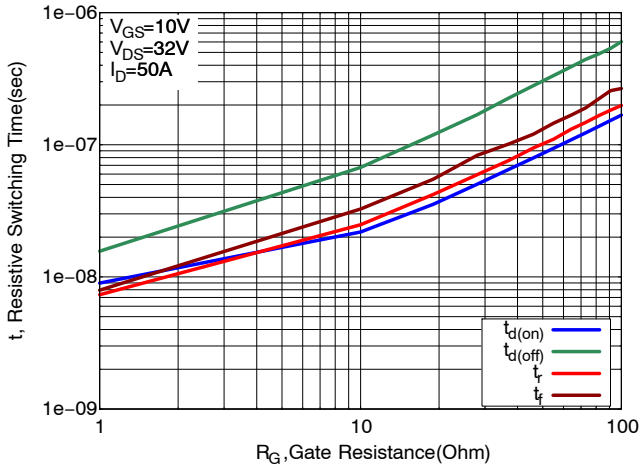


Figure 9. Resistive Switching Time Variation vs. Gate Resistance

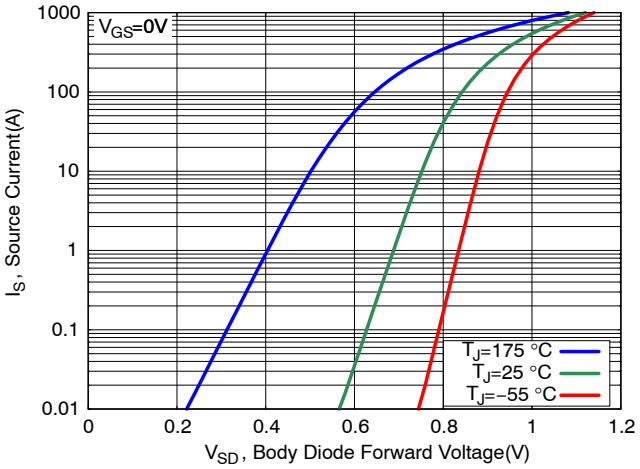


Figure 10. Diode Forward Characteristics

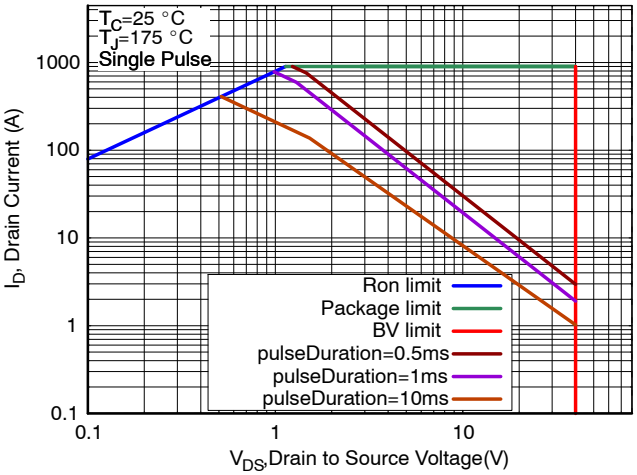


Figure 11. Maximum Rated Forward Biased Safe Operating Area

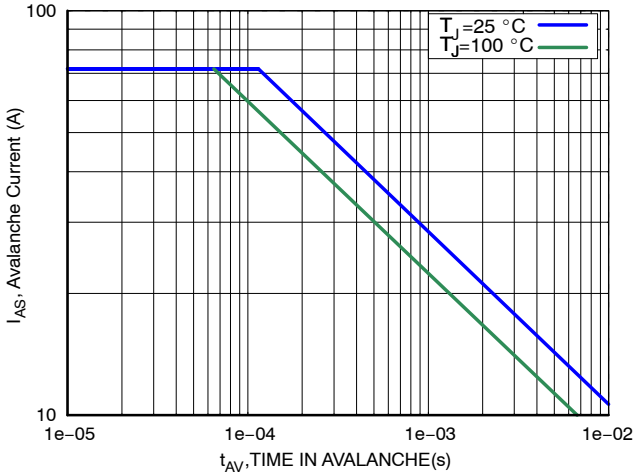


Figure 12. Ipeak vs. Time in Avalanche

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TYPICAL CHARACTERISTICS

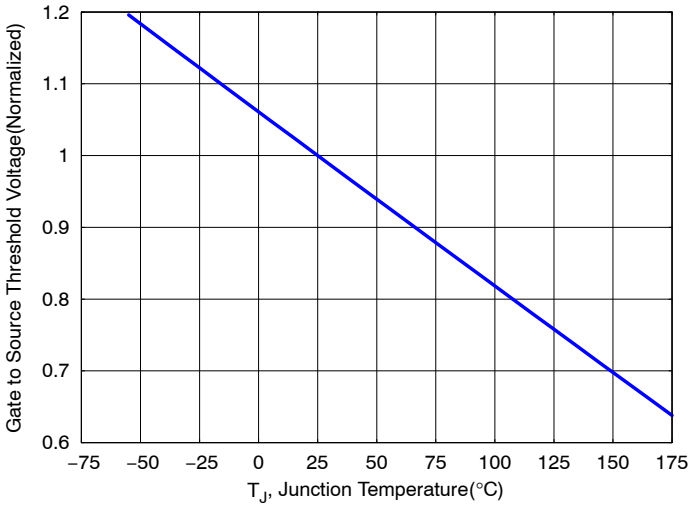


Figure 13. Gate Threshold Voltage vs. Junction Temperature

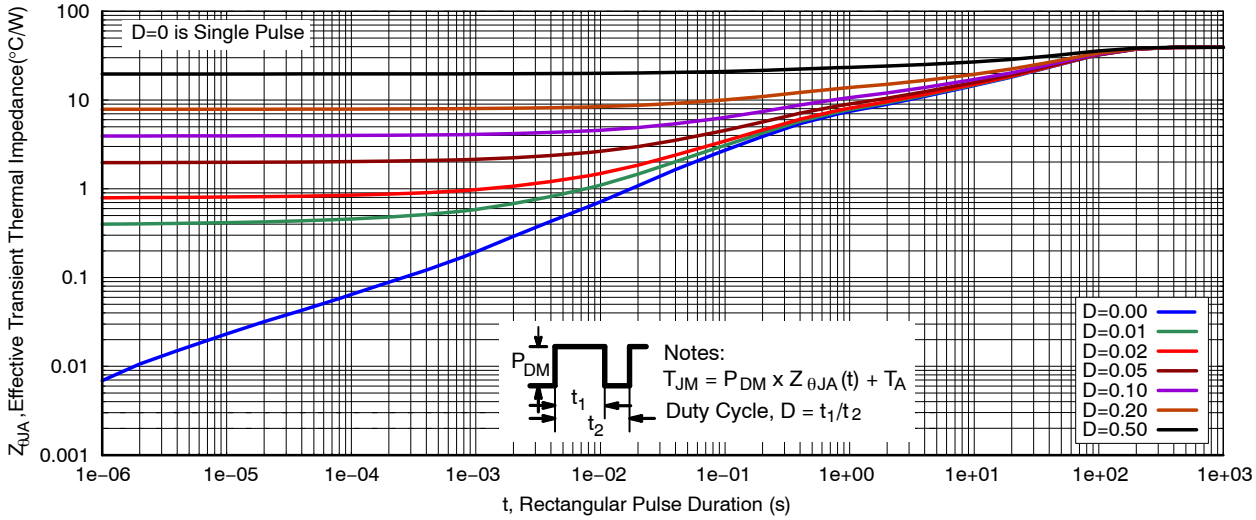


Figure 14. Thermal Response

ORDERING INFORMATION

Device	Marking	Package	Shipping†
NVMFWS0D7N04XMT1G	0D7N4W	DFNW5 (Pb-Free)	1500 / Tape & Reel
NVMFWS0D7N04XMET1G	0D7N4W	DFNW5 (Pb-Free)	1500 / Tape & Reel
NVMFS0D7N04XMET1G	0D7N4	DFN5 (Pb-Free)	1500 / Tape & Reel

† For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

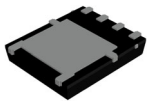
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REVISION HISTORY

Revision	Description of Changes	Date
5	Added non−Wettable Flank NVMFS0D7N04XMET1G and DFN5 ordering options. Added CASE 506FE package outline and DFN5 package diagram.	9/10/2026
6	Updated values of trr, ta, tb & Qrr.	10/26/2026

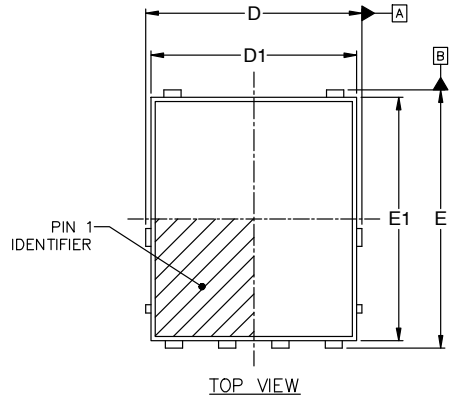
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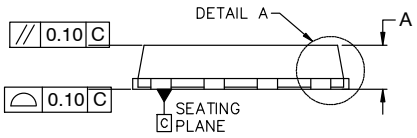
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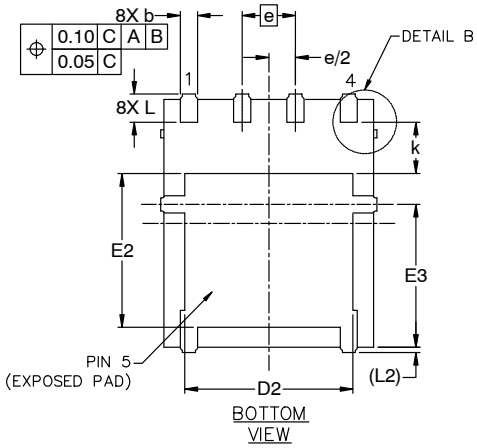


DFNW−5 4.90x5.90x1.00, 1.27P
CASE 507BA
ISSUE D

DATE 05 OCT 2026

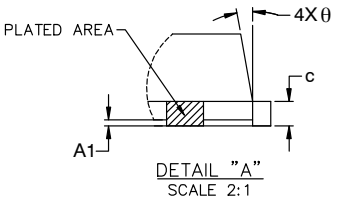


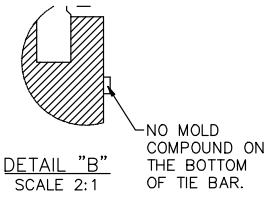




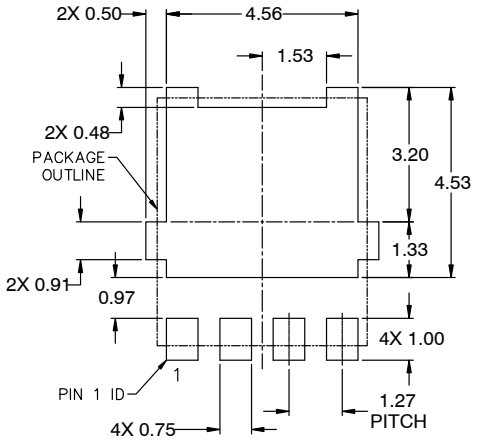
NOTES:

1. DIMENSIONING AND TOLERANCING CONFORM TO ASME Y14.5M−2018.
2. ALL DIMENSIONS ARE IN MILLIMETERS.
3. DIMENSIONS D1 AND E1 DO NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR GATE BURRS.
4. THIS PACKAGE CONTAINS WETTABLE FLANK DESIGN FEATURES TO AID IN FILLET FORMATION ON THE LEADS DURING MOUNTING.





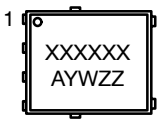
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	MIN	NOM	MAX
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A1	0.00	−−−	0.05
b	0.33	0.41	0.51
c	0.23	0.28	0.33
D	5.00	5.15	5.30
D1	4.70	4.90	5.10
D2	3.80	4.00	4.20
E	6.00	6.15	6.30
E1	5.70	5.90	6.10
E2	3.45	3.65	3.85
E3	3.00	3.40	3.80
e	1.27 BSC		
k	1.20	1.35	1.50
L	0.51	0.57	0.71
L2	0.15 REF.		
θ	0°	6°	12°



RECOMMENDED MOUNTING FOOTPRINT*

*FOR ADDITIONAL INFORMATION ON OUR Pb−FREE STRATEGY AND SOLDERING DETAILS, PLEASE DOWNLOAD THE ONSEMI SOLDERING AND MOUNTING TECHNIQUES REFERENCE MANUAL, SOLDERRM/D.

GENERIC MARKING DIAGRAM*



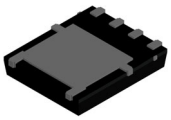
XXXXXX = Specific Device Code
A = Assembly Location
Y = Year
W = Work Week
ZZ = Lot Traceability

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, "G" or microdot " ▪", may or may not be present. Some products may not follow the Generic Marking.

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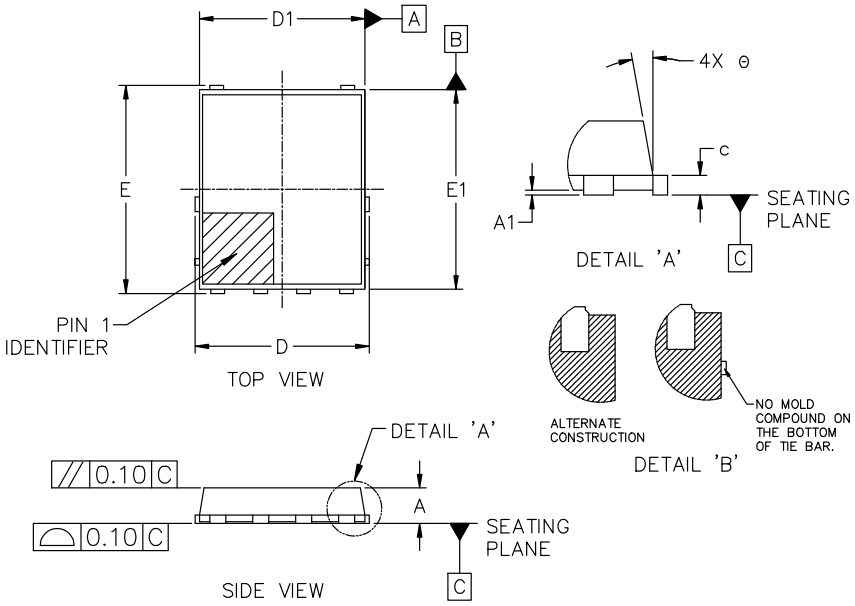
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MECHANICAL CASE OUTLINE
PACKAGE DIMENSIONS

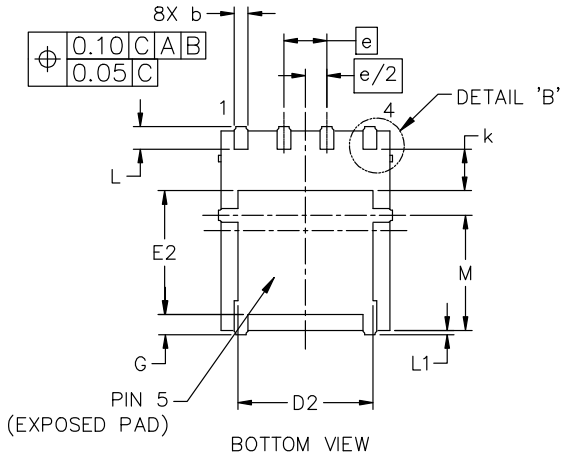


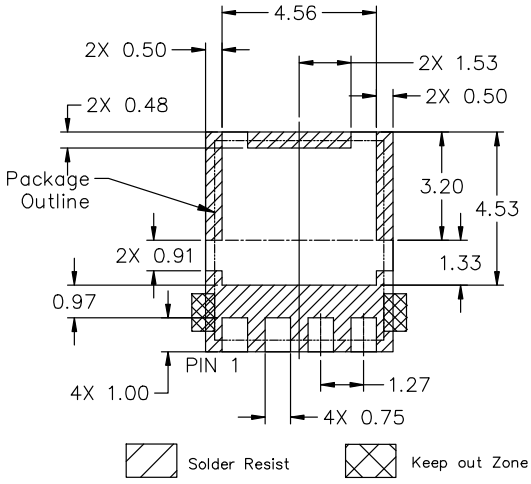
DFN−5 4.90x5.90x1.00, 1.27P
CASE 506FE
ISSUE B

DATE 17 AUG 2026



MILLIMETERS			
DIM	MIN	NOM	MAX
A	0.90	1.00	1.10
A1	0.00	−−−	0.05
b	0.33	0.41	0.51
c	0.23	0.28	0.33
D	5.00	5.15	5.30
D1	4.70	4.90	5.10
D2	3.80	4.00	4.20
E	6.00	6.15	6.30
E1	5.70	5.90	6.10
E2	3.45	3.65	3.85
e	1.27 BSC		
G	0.51	0.575	0.71
k	1.20	1.35	1.50
L	0.51	0.575	0.71
L2	0.150 REF		
M	3.00	3.40	3.80
θ	0°	−−−	12°





NOTES:
1. DIMENSIONING AND TOLERANCING AS PER ASME Y14.5M, 2018.
2. CONTROLLING DIMENSIONS: MILLIMETERS.
3. DIMENSIONS D1 AND E1 DO NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS.

RECOMMENDED MOUNTING FOOTPRINT

*For additional information on our Pb−Free strategy and soldering details, please download the onsemi Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

GENERIC MARKING DIAGRAM*



XXXX = Specific Device Code
A = Assembly Location
Y = Year
W = Work Week
ZZ = Assembly Lot Code

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, "G" or microdot "▪", may or may not be present. Some products may not follow the Generic Marking.

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