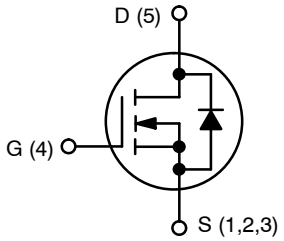
MOSFET - Power, Single N-Channel, STD Gate, SO8FL

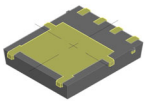
80 V, 2.1 mΩ, 181 A

NVMFWS2D1N08X

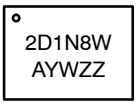
$V_{(BR)DSS}$	$R_{DS(ON)}$ MAX	I_D MAX
80 V	2.1 mΩ @ 10 V	181 A



N−CHANNEL MOSFET



DFNW5 (SO−8FL)
CASE 507BA



2D1N8W = Specific Device Code
A = Assembly Location
Y = Year
W = Work Week
ZZ = Assembly Lot Code

Features

- Low Q_{RR}, Soft Recovery Body Diode
- Low $R_{DS(on)}$ to Minimize Conduction Losses
- Low Q_G and Capacitance to Minimize Driver Losses
- AEC−Q101 Qualified and PPAP Capable
- These Devices are Pb−Free, Halogen Free/BFR Free and are RoHS Compliant

Applications

- Synchronous Rectification (SR) in DC−DC and AC−DC
- Primary Switch in Isolated DC−DC Converter
- Motor Drives
- Automotive 48 V System

MAXIMUM RATINGS (T_J = 25°C unless otherwise stated)

Parameter		Symbol	Value	Unit
Drain−to−Source Voltage		V_{DSS}	80	V
Gate−to−Source Voltage		V_{GS}	±20	V
Continuous Drain Current (Note 1)	T_C = 25°C	I_D	181	A
	T_C = 100°C		128	
Power Dissipation (Note 1)	T_C = 25°C	P_D	148	W
Pulsed Drain Current	T_C = 25°C, t_p = 100 μs	I_{DM}	761	A
Pulsed Source Current (Body Diode)		I_{SM}	761	
Operating Junction and Storage Temperature Range		T_J, T_{STG}	−55 to +175	°C
Source Current (Body Diode)		I_S	224	A
Single Pulse Avalanche Energy (I_{PK} = 55 A) (Note 2)		E_{AS}	151	mJ
Lead Temperature for Soldering Purposes (1/8″ from case for 10 s)		T_L	260	°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. The entire application environment impacts the thermal resistance values shown, they are not constants and are only valid for the particular conditions noted.
2. Actual continuous current will be limited by thermal & electromechanical application board design.
3. EAS of 151 mJ is based on started T_J = 25°C, I_{AS} = 55 A, V_{DD} = 64 V, V_{GS} =10 V, 100% avalanche tested

ORDERING INFORMATION

Device	Package	Shipping†
NVMFWS2D1N08XT1G	DFNW5	1500 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specification Brochure, BRD8011/D.

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THERMAL CHARACTERISTICS

Parameter	Symbol	Value	Unit
Thermal Resistance, Junction−to−Case	$R_{\theta JC}$	1.01	°C/W
Thermal Resistance, Junction−to−Ambient	$R_{\theta JA}$	39	

4. Surface−mounted on FR4 board using 1 in^2 pad size, 1 oz. Cu pad.
5. R_{JA} is determined by the user's board design.

ELECTRICAL CHARACTERISTICS (T_J = 25°C unless otherwise specified)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
OFF CHARACTERISTICS						
Drain−to−Source Breakdown Voltage	$V_{(BR)DSS}$	V_{GS} = 0 V, I_D = 1 mA	80			V
Drain−to−Source Breakdown Voltage Temperature Coefficient	$\Delta V_{(BR)DSS}/\Delta T_J$	I_D = 1 mA, Referenced to 25°C		31.6		mV/°C
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = 80 V, T_J = 25°C			1	μA
		V_{DS} = 80 V, T_J = 125°C			250	
Gate−to−Source Leakage Current	I_{GSS}	V_{DS} = 20 V, V_{DS} = 0 V			100	nA
ON CHARACTERISTICS						
Drain−to−Source On Resistance	$R_{DS(on)}$	V_{GS} = 10 V, I_D = 43 A, T_J = 25°C		1.9	2.1	mΩ
Gate Threshold Voltage	$V_{GS(TH)}$	V_{GS} = V_{DS}, I_D = 213 μA, T_J = 25°C	2.4		3.6	V
Gate Threshold Voltage Temperature Coefficient	$\Delta V_{GS(TH)}/\Delta T_J$	V_{GS} = V_{DS}, I_D = 213 μA		−7.5		mV/°C
Forward Transconductance	g_{FS}	V_{DS} = 5 V, I_D = 43 A		135		S
CHARGES, CAPACITANCES & GATE RESISTANCE						
Input Capacitance	C_{ISS}	V_{GS} = 0 V, V_{DS} = 40 V, f = 1 MHz		3800		pF
Output Capacitance	C_{OSS}			1100		
Reverse Transfer Capacitance	C_{RSS}			17		
Output Charge	Q_{OSS}			79		nC
Total Gate Charge	$Q_{G(TOT)}$	V_{GS} = 6 V, V_{DD} = 40 V, I_D = 43 A		33		
		V_{GS} = 10 V, V_{DD} = 40 V, I_D = 43 A		53		
Threshold Gate Charge	$Q_{G(TH)}$			12		
Gate−to−Source Charge	Q_{GS}			18		
Gate−to−Drain Charge	Q_{GD}			8		
Gate Plateau Voltage	V_{GP}			4.7		V
Gate Resistance	R_G	f = 1 MHz		0.8		Ω
SWITCHING CHARACTERISTICS						
Turn−On Delay Time	$t_{d(ON)}$	Resistive Load, V_{GS} = 0/10 V, V_{DD} = 64 V, I_D = 43 A, R_G = 2.5 Ω		26		ns
Rise Time	t_r			10		
Turn−Off Delay Time	$t_{d(OFF)}$			40		
Fall Time	t_f			6		
SOURCE−TO−DRAIN DIODE CHARACTERISTICS						
Forward Diode Voltage	V_{SD}	V_{GS} = 0 V, I_S = 43 A, T_J = 25°C		0.82	1.2	V
		V_{GS} = 0 V, I_S = 43 A, T_J = 125°C		0.66		

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ELECTRICAL CHARACTERISTICS (T_J = 25°C unless otherwise specified)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
SOURCE−TO−DRAIN DIODE CHARACTERISTICS						
Reverse Recovery Time	t_{RR}	V_{GS} = 0 V, dI/dt = 1000 A/μs, I_S = 43 A, V_{DD} = 64 V		25		ns
Charge Time	t_a			14		
Discharge Time	t_b			11		
Reverse Recovery Charge	Q_{RR}			189		nC

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

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TYPICAL CHARACTERISTICS

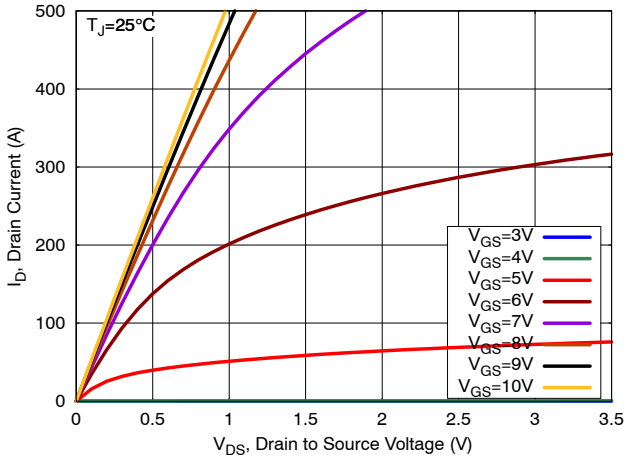


Figure 1. On−Region Characteristics

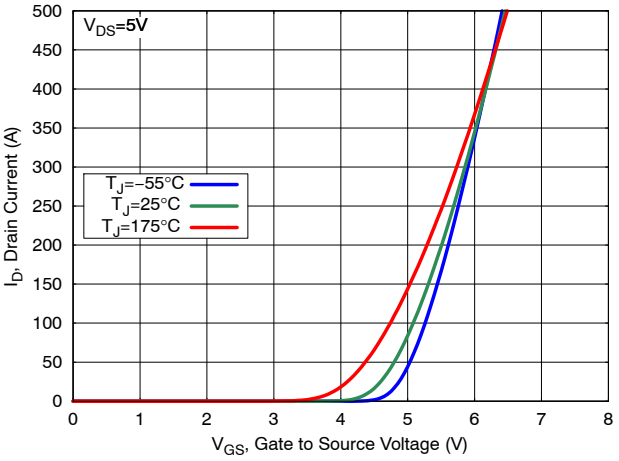


Figure 2. Transfer Characteristics

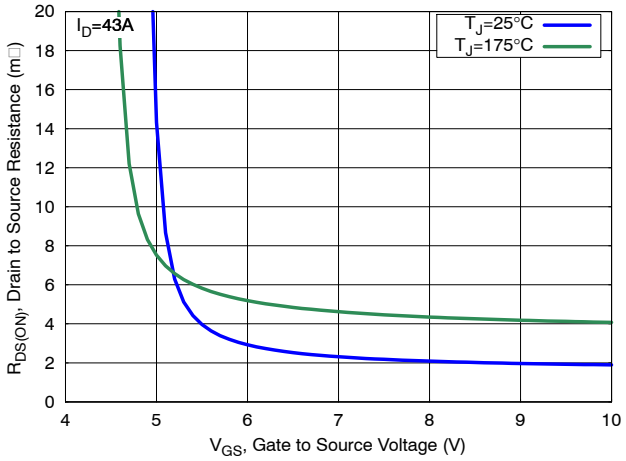


Figure 3. On−Resistance vs. Gate Voltage

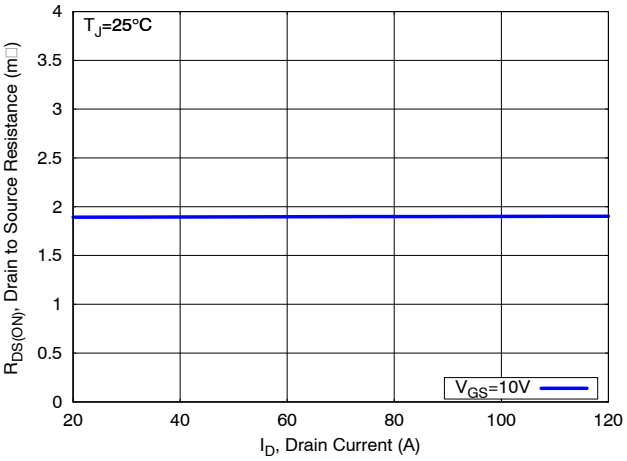


Figure 4. On−Resistance vs. Drain Current

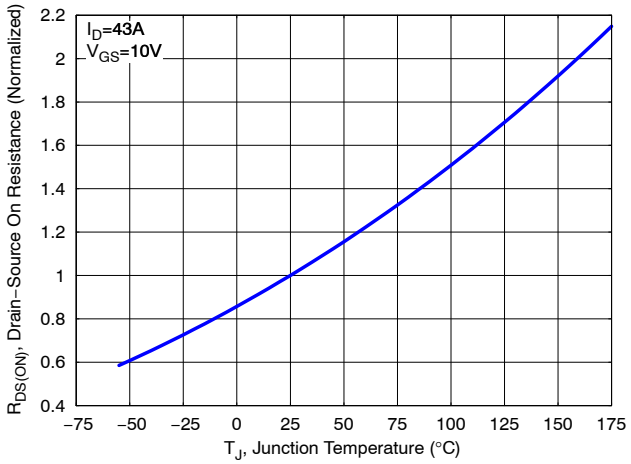


Figure 5. Normalized ON Resistance vs. Junction Temperature

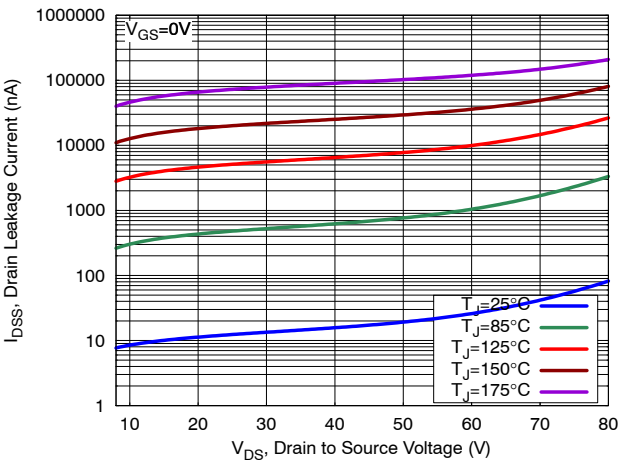


Figure 6. Drain Leakage Current vs. Drain Voltage

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TYPICAL CHARACTERISTICS

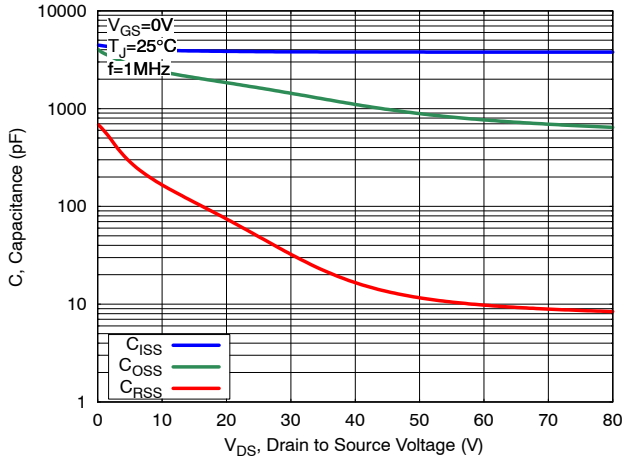


Figure 7. Capacitance Characteristics

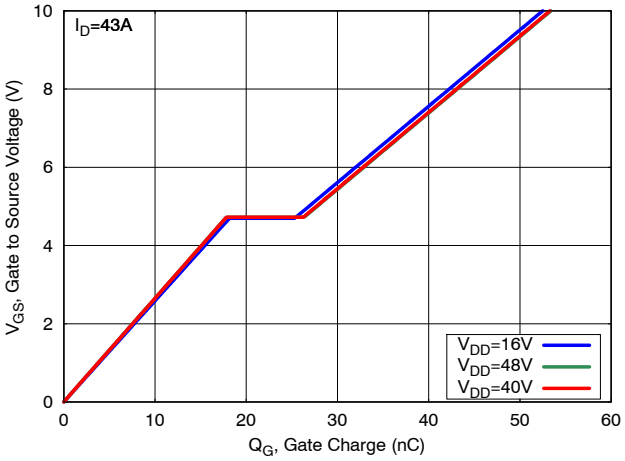


Figure 8. Gate Charge Characteristics

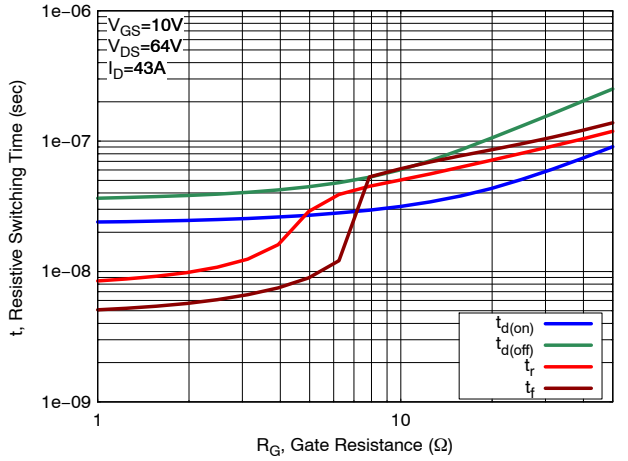


Figure 9. Resistive Switching Time Variation vs. Gate Resistance

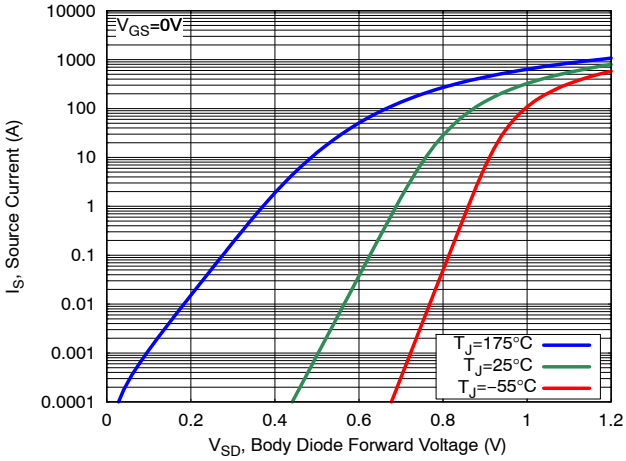


Figure 10. Diode Forward Characteristics

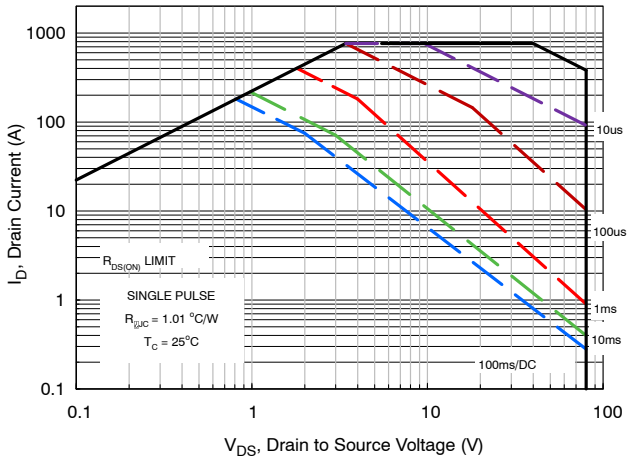


Figure 11. Safe Operating Area (SOA)

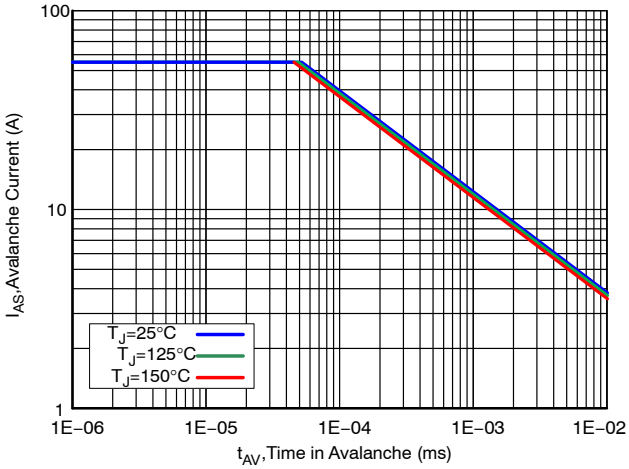


Figure 12. Avalanche Current vs Pulse Time (UIS)

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TYPICAL CHARACTERISTICS

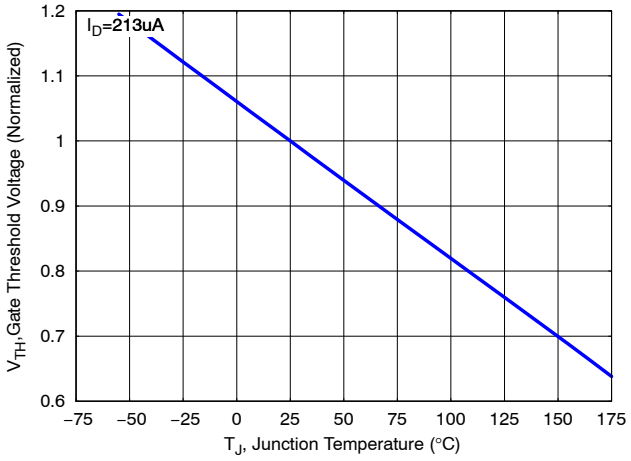


Figure 13. Gate Threshold Voltage vs Junction Temperature

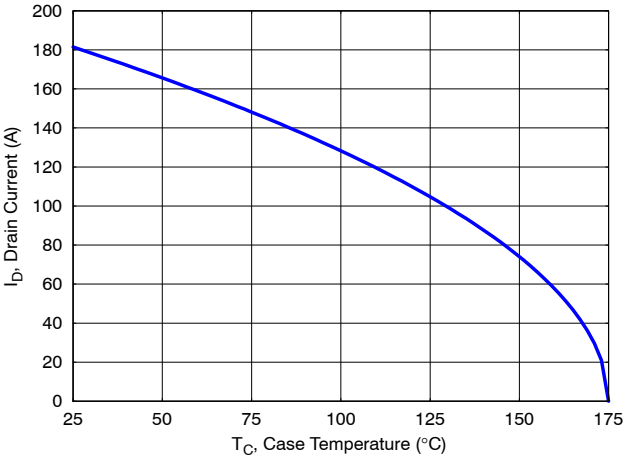


Figure 14. Maximum Current vs. Case Temperature

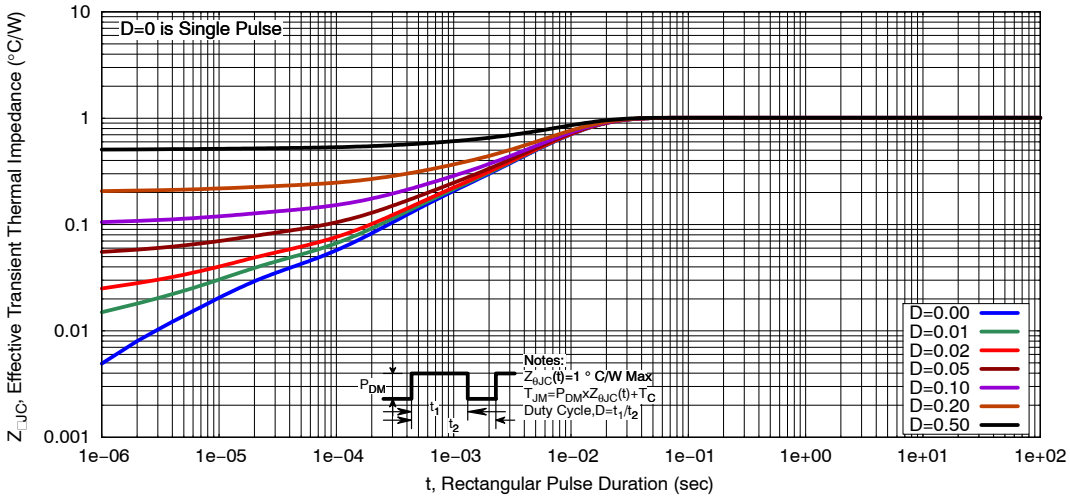
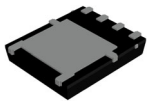


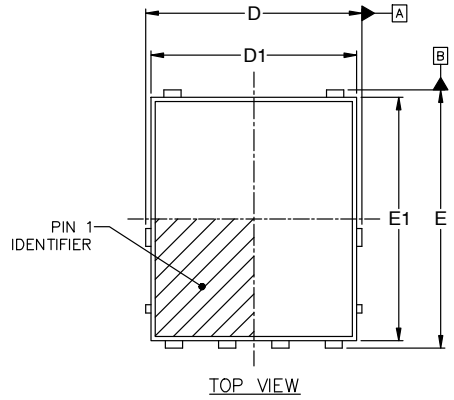
Figure 15. Transient Thermal Response

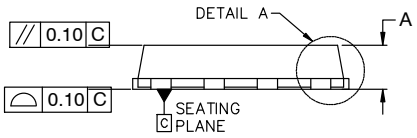
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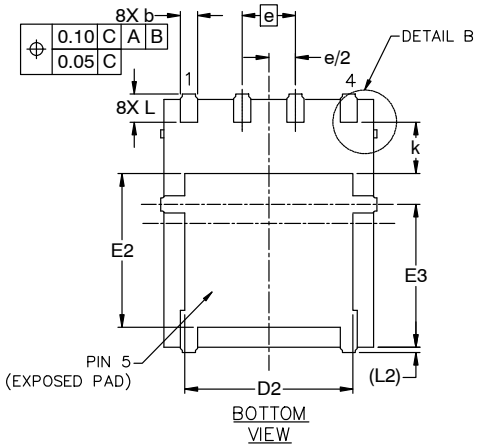


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CASE 507BA
ISSUE D

DATE 05 OCT 2026

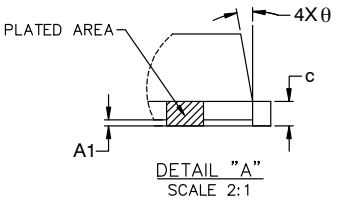


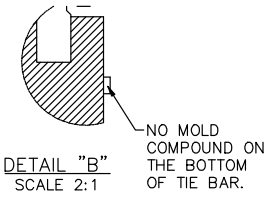




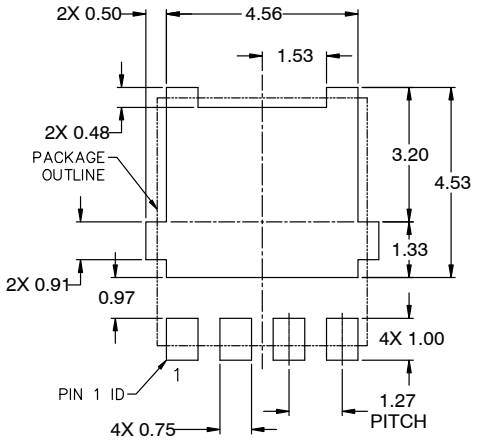
NOTES:

1. DIMENSIONING AND TOLERANCING CONFORM TO ASME Y14.5M−2018.
2. ALL DIMENSIONS ARE IN MILLIMETERS.
3. DIMENSIONS D1 AND E1 DO NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR GATE BURRS.
4. THIS PACKAGE CONTAINS WETTABLE FLANK DESIGN FEATURES TO AID IN FILLET FORMATION ON THE LEADS DURING MOUNTING.





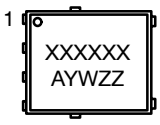
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	MIN	NOM	MAX
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A1	0.00	−−−	0.05
b	0.33	0.41	0.51
c	0.23	0.28	0.33
D	5.00	5.15	5.30
D1	4.70	4.90	5.10
D2	3.80	4.00	4.20
E	6.00	6.15	6.30
E1	5.70	5.90	6.10
E2	3.45	3.65	3.85
E3	3.00	3.40	3.80
e	1.27 BSC		
k	1.20	1.35	1.50
L	0.51	0.57	0.71
L2	0.15 REF.		
θ	0°	6°	12°



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GENERIC MARKING DIAGRAM*



XXXXXX = Specific Device Code
A = Assembly Location
Y = Year
W = Work Week
ZZ = Lot Traceability

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, "G" or microdot " ▪", may or may not be present. Some products may not follow the Generic Marking.

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