MOSFET – Power, Single N-Channel

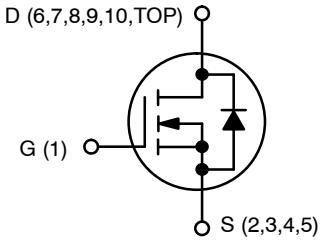
60 V, 1.49 mΩ, 198 A

NVMJST1D4N06CL

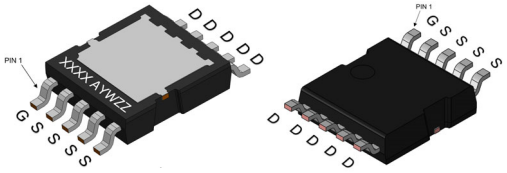
$V_{(BR)DSS}$	$R_{DS(ON)}$ MAX	I_D MAX
60 V	1.49 mΩ @ 10 V	198 A

Features

- Small Footprint (5x7 mm) for Compact Design
- Low $R_{DS(on)}$ to Minimize Conduction Losses
- Low Q_G and Capacitance to Minimize Driver Losses
- TCPAK57 Top Cool Package
- AEC−Q101 Qualified and PPAP Capable
- These Devices are Pb−Free and are RoHS Compliant



N−CHANNEL MOSFET



TCPAK57
CASE 760AG

MAXIMUM RATINGS (T_J = 25°C unless otherwise noted)

Parameter			Symbol	Value	Unit
Drain−to−Source Voltage			V_{DSS}	60	V
Gate−to−Source Voltage			V_{GS}	±20	V
Continuous Drain Current $R_{\theta JC}$ (Notes 1, 3)	Steady State	T_C = 25°C	I_D	198	A
		T_C = 100°C		140	
Power Dissipation $R_{\theta JC}$ (Note 1)		T_C = 25°C	P_D	116	W
		T_C = 100°C		58	
Continuous Drain Current $R_{\theta JA}$ (Notes 1, 2, 3)	Steady State	T_A = 25°C	I_D	42	A
		T_A = 100°C		30	
Power Dissipation $R_{\theta JA}$ (Notes 1, 2)		T_A = 25°C	P_D	5.3	W
		T_A = 100°C		2.6	
Pulsed Drain Current	T_A = 25°C, t_p = 10 μs		I_{DM}	900	A
Operating Junction and Storage Temperature Range			T_J, T_{stg}	−55 to +175	°C
Source Current (Body Diode)			I_S	96	A
Single Pulse Drain−to−Source Avalanche Energy ($I_{L(pk)}$ = 16.7 A)			E_{AS}	596	mJ
Lead Temperature for Soldering Purposes (1/8″ from case for 10 s)			T_L	260	°C

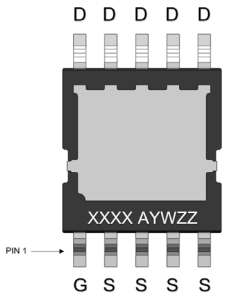
Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

THERMAL RESISTANCE MAXIMUM RATINGS

Parameter	Symbol	Value	Unit
Junction−to−Case − Steady State	$R_{\theta JC}$	0.3	°C/W
Junction−to−Ambient − Steady State (Note 2)	$R_{\theta JA}$	28.5	
Junction−to−Heatsink Top − Steady State (Note 2)	$R_{\psi JH}$	1.3	
Junction−to−Drain Lead	$R_{\psi JL}$	4.7	
Junction−to−Source Lead	$R_{\psi JL}$	5.1	

1. The entire application environment impacts the thermal resistance values shown, they are not constants and are only valid for the particular conditions noted.
2. 2s2p JEDEC51−7 standard PCB mounted to a 25x25x3 (mm) aluminum heatsink with a 12 w/mK TIM interface.
3. Maximum current for pulses as long as 1 second is higher but is dependent on pulse duration and duty cycle.

MARKING DIAGRAM



XXXX = Specific Device Code
A = Assembly Location
Y = Year
W = Work Week
ZZ = Assembly Lot Code

ORDERING INFORMATION

See detailed ordering, marking and shipping information in the package dimensions section on page 5 of this data sheet.

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ELECTRICAL CHARACTERISTICS (T_J = 25°C unless otherwise specified)

Parameter	Symbol	Test Condition		Min	Typ	Max	Unit
OFF CHARACTERISTICS							
Drain−to−Source Breakdown Voltage	$V_{(BR)DSS}$	V_{GS} = 0 V, I_D = 250 μA		60			V
Drain−to−Source Breakdown Voltage Temperature Coefficient	$V_{(BR)DSS}/T_J$				27.9		mV/°C
Zero Gate Voltage Drain Current	I_{DSS}	V_{GS} = 0 V, V_{DS} = 60 V	T_J = 25 °C			10	μA
			T_J = 125°C			250	
Gate−to−Source Leakage Current	I_{GSS}	V_{DS} = 0 V, V_{GS} = ±16 V				±100	nA
ON CHARACTERISTICS (Note 4)							
Gate Threshold Voltage	$V_{GS(TH)}$	V_{GS} = V_{DS}, I_D = 250 μA		1.2		2	V
Threshold Temperature Coefficient	$V_{GS(TH)}/T_J$				−6.11		mV/°C
Drain−to−Source On Resistance	$R_{DS(on)}$	V_{GS} = 10 V	I_D = 50 A		1.27	1.49	mΩ
Forward Transconductance	g_{FS}	V_{DS} = 5 V, I_D = 50 A			217		S
CHARGES, CAPACITANCES & GATE RESISTANCE							
Input Capacitance	C_{ISS}	V_{GS} = 0 V, f = 1 MHz, V_{DS} = 25 V			6555		pF
Output Capacitance	C_{OSS}				3695		
Reverse Transfer Capacitance	C_{RSS}				37.5		
Total Gate Charge	$Q_{G(TOT)}$	V_{GS} = 10 V, V_{DS} = 48 V; I_D = 50 A			92.2		nC
Threshold Gate Charge	$Q_{G(TH)}$	V_{GS} = 10 V, V_{DS} = 48 V; I_D = 50 A			9.5		
Gate−to−Source Charge	Q_{GS}				16.2		
Gate−to−Drain Charge	Q_{GD}				10.5		
Plateau Voltage	V_{GP}				2.8		V
SWITCHING CHARACTERISTICS (Note 5)							
Turn−On Delay Time	$t_{d(ON)}$	V_{GS} = 10 V, V_{DS} = 48 V, I_D = 50 A, R_G = 1.0 Ω			16		ns
Rise Time	t_r				25		
Turn−Off Delay Time	$t_{d(OFF)}$				60		
Fall Time	t_f				11		
DRAIN−SOURCE DIODE CHARACTERISTICS							
Forward Diode Voltage	V_{SD}	V_{GS} = 0 V, I_S = 50 A	T_J = 25°C		0.8	1.2	V
			T_J = 125°C		0.66		
Reverse Recovery Time	t_{RR}	V_{GS} = 0 V, dIS/dt = 100 A/μs, I_S = 50 A			82.1		ns
Charge Time	t_a				42.4		
Discharge Time	t_b				40		
Reverse Recovery Charge	Q_{RR}				119		nC

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

4. Pulse Test: pulse width ≤ 300 μs, duty cycle ≤ 2%.
5. Switching characteristics are independent of operating junction temperatures.

TYPICAL CHARACTERISTICS

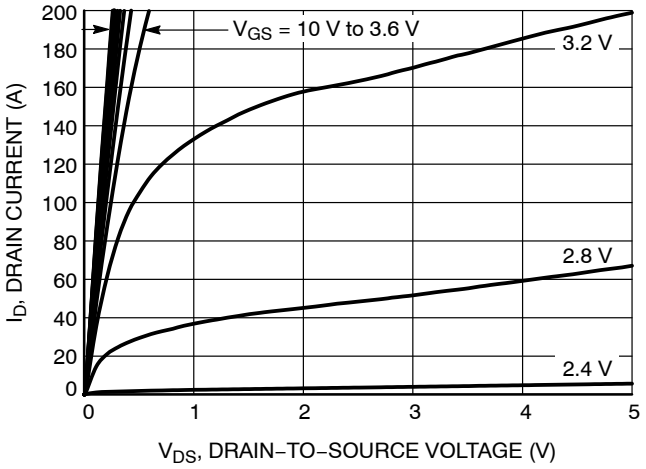


Figure 1. On−Region Characteristics

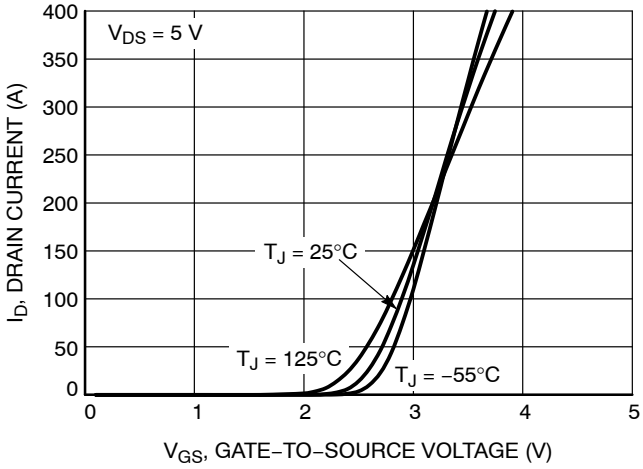


Figure 2. Transfer Characteristics

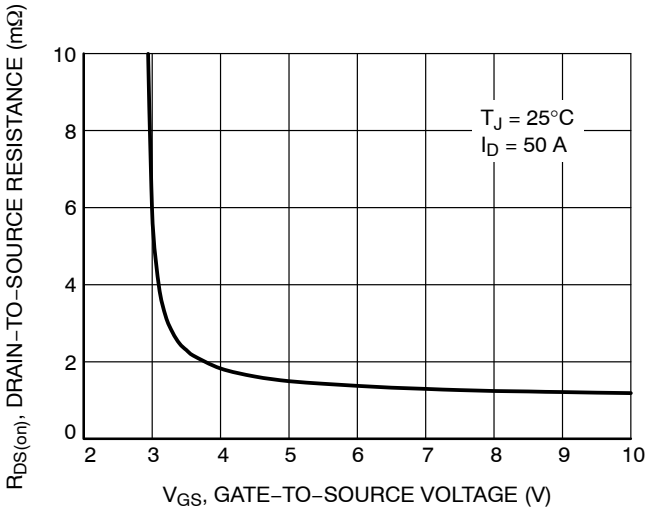


Figure 3. On−Resistance vs. Gate−to−Source Voltage

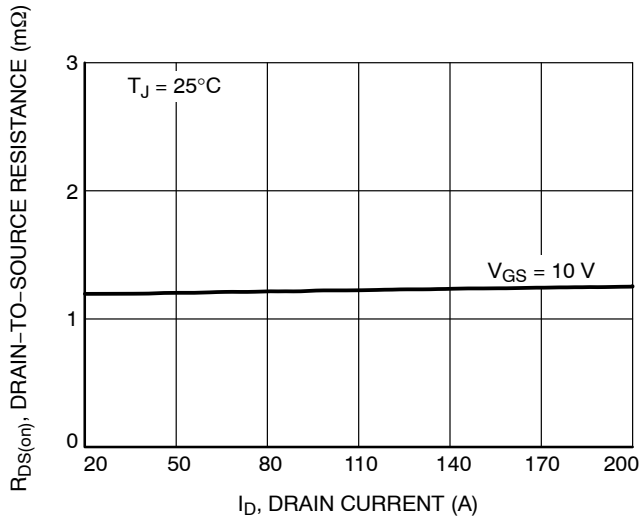


Figure 4. On−Resistance vs. Drain Current and Gate Voltage

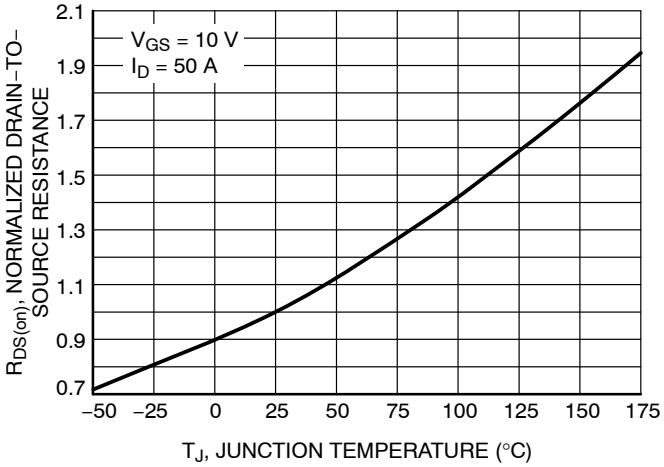


Figure 5. On−Resistance Variation with Temperature

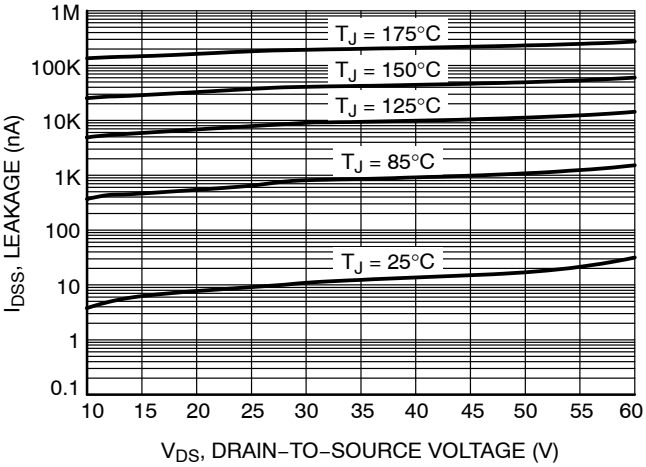


Figure 6. Drain−to−Source Leakage Current vs. Voltage

TYPICAL CHARACTERISTICS

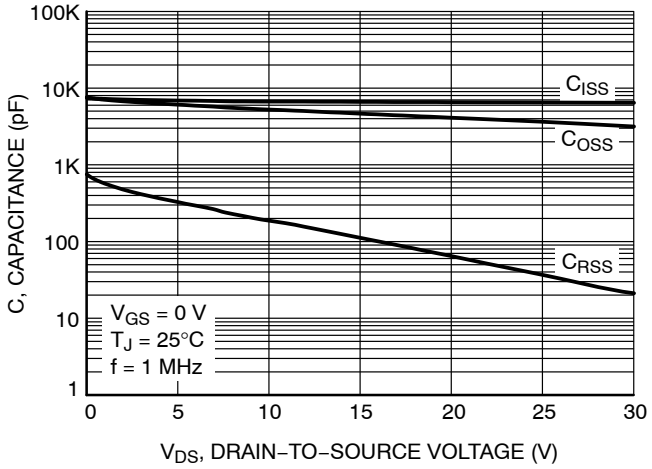


Figure 7. Capacitance Variation

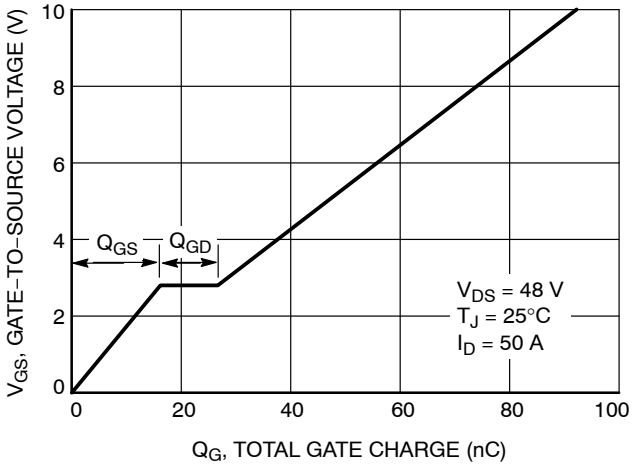


Figure 8. Gate−to−Source and Drain−to−Source Voltage vs. Total Charge

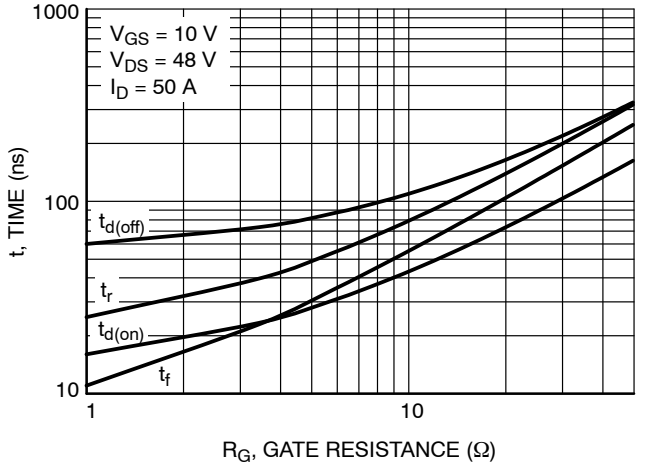


Figure 9. Resistive Switching Time Variation vs. Gate Resistance

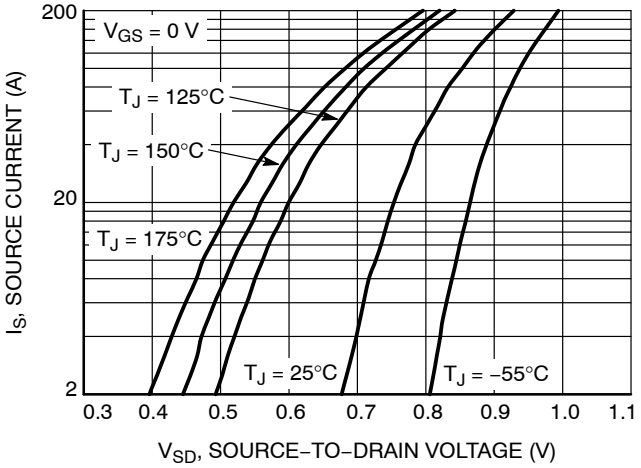


Figure 10. Diode Forward Voltage vs. Current

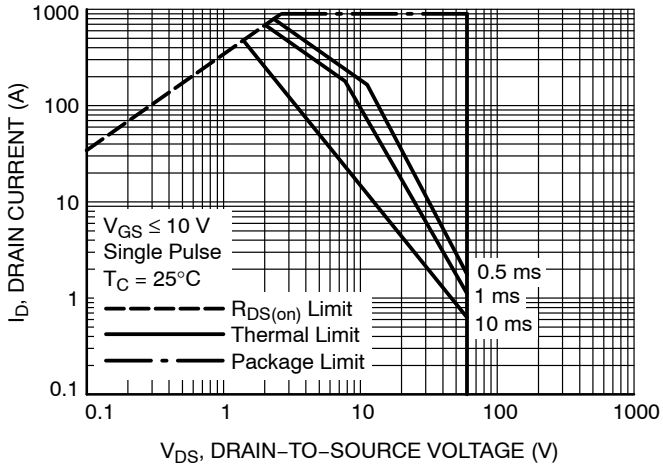


Figure 11. Safe Operating Area

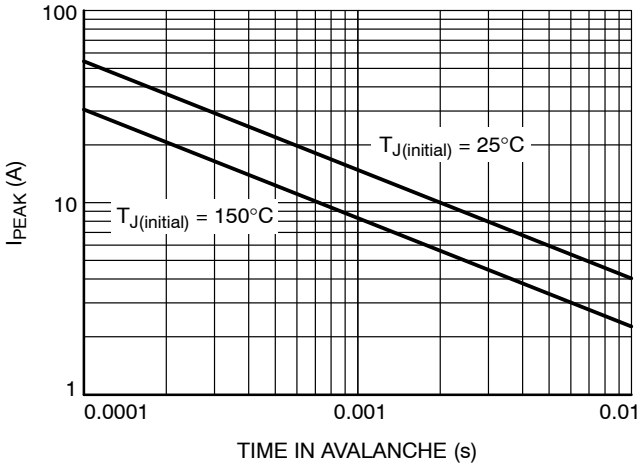


Figure 12. I_{PEAK} vs. Time in Avalanche

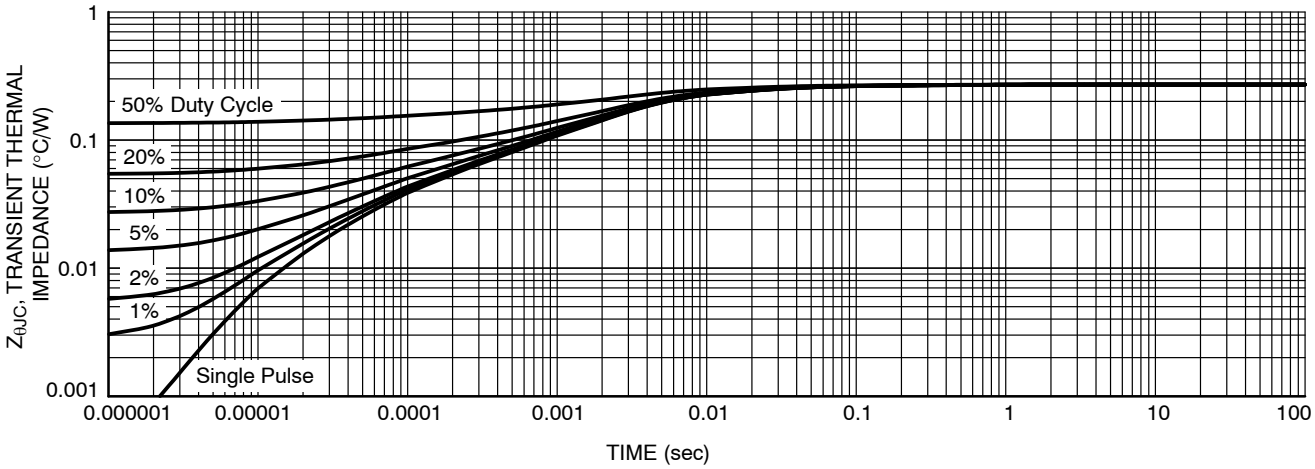


Figure 13. Thermal Characteristics

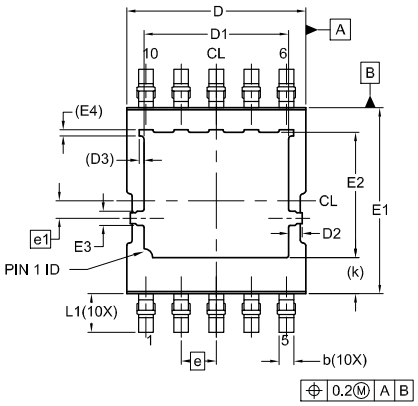
DEVICE ORDERING INFORMATION

Device	Marking	Package	Shipping†
NVMJST1D4N06CLTXG	1D46L	TCPAK57 (Pb−Free)	3000 / Tape & Reel

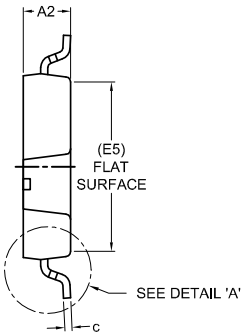
†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

PACKAGE DIMENSIONS

TCPAK10 5.1x7.5, 1.0P
CASE 760AG
ISSUE D

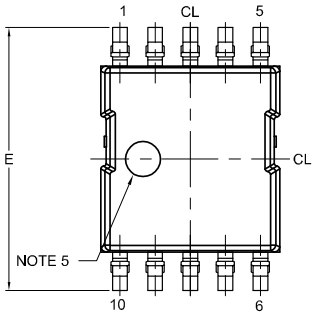


TOP VIEW

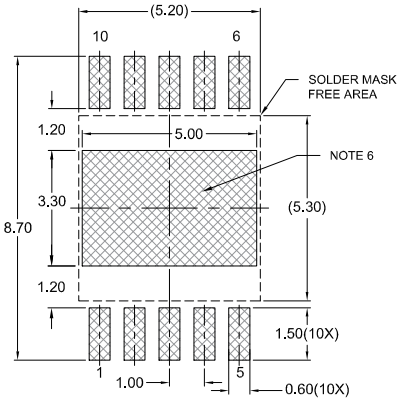


SIDE VIEW

NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. UNIT DIMENSION: MILLIMETERS
3. DIMENSIONS D AND E DO NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR BURRS. MOLD FLASH PROTRUSIONS OR GATE BURRS SHALL NOT EXCEED 0.150mm PER SIDE.
4. DIMENSIONS D AND E1 ARE DETERMINED AT THE OUTERMOST EXTREMES OF THE PLASTIC BODY.
5. OPTIONAL MOLD FEATURE.
6. LAND PAD UNDER THE PACKAGE BODY IS FOR MECHANICAL SUPPORT ONLY, SOLDER CONNECTION IS NOT REQUIRED.
7. DIMENSION A1 IS THE LEAD STAND-OFF FROM THE BOTTOM SURFACE OF THE PACKAGE BODY.



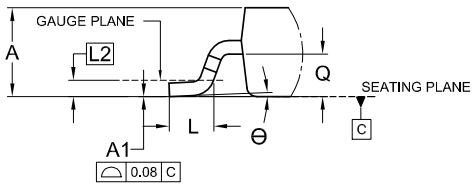
BOTTOM VIEW



LAND PAD RECOMMENDATION

*FOR ADDITIONAL INFORMATION ON OUR PB-FREE STRATEGY AND SOLDERING DETAILS, PLEASE DOWNLOAD THE ON SEMICONDUCTOR SOLDERING AND MOUNTING TECHNIQUES REFERENCE MANUAL, SOLDERRM/D.

MILLIMETERS			
DIM	MIN	NOM	MAX
A	1.30	1.35	1.45
A1	-0.05	0.00	0.05
A2	1.30	1.35	1.40
b	0.36	0.41	0.46
c	0.16	0.21	0.26
D	5.00	5.10	5.20
D1	4.02	4.12	4.22
D2	0.30	0.40	0.50
D3	0.14 REF		
E	7.40	7.50	7.60
E1	5.20	5.30	5.40
E2	3.47	3.57	3.67
E3	0.30	0.40	0.50
E4	0.17 REF		
E5	4.82 REF		
e	1.00 BSC		
e1	0.50 BSC		
k	1.03 REF		
L	0.49	0.69	0.89
L1	0.90	1.10	1.30
L2	0.25 BSC		
Q	0.60	0.65	0.70
Θ	0°	2.5°	5°



DETAIL 'A'

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Entegreden kapasitöre tüm elektronik komponent kategorileri.

Kategorilere göz atın

Üreticiler

Aradığınız üreticinin ürünlerini tek sayfada inceleyin.

Üreticileri görün

Toplu alım ve teklif

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Teklif isteyin

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