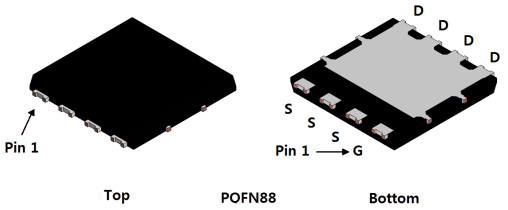
MOSFET – Power, Single N-Channel

60 V, 0.68 mΩ, 477 A

NVMTS0D7N06CL

$V_{(BR)DSS}$	$R_{DS(ON)}$ MAX	I_D MAX
60 V	0.68 mΩ @ 10 V	477 A
	0.90 mΩ @ 4.5 V	



TDFNW8
CASE 507AP

Features

- Small Footprint (8x8 mm) for Compact Design
- Low $R_{DS(on)}$ to Minimize Conduction Losses
- Low Q_G and Capacitance to Minimize Driver Losses
- Power 88 Package, Industry Standard
- AEC-Q101 Qualified and PPAP Capable
- Wettable Flank Option for Enhanced Optical Inspection
- These Devices are Pb-Free, Halogen Free/BFR Free and are RoHS Compliant

MAXIMUM RATINGS (T_J = 25 °C unless otherwise noted)

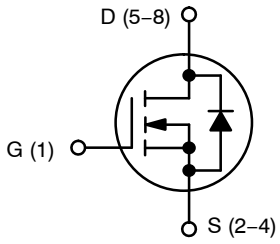
Symbol	Parameter			Value	Unit
V_{DSS}	Drain-to-Source Voltage			60	V
V_{GS}	Gate-to-Source Voltage			±20	V
I_D	Continuous Drain Current $R_{\theta JC}$ (Notes 1, 3)	Steady State	T_C = 25 °C	477	A
			T_C = 100 °C	337.6	
P_D	Power Dissipation $R_{\theta JC}$ (Note 1)		T_C = 25 °C	294.6	W
			T_C = 100 °C	147.3	
I_D	Continuous Drain Current $R_{\theta JA}$ (Notes 1, 2, 3)	Steady State	T_A = 25 °C	62.2	A
			T_A = 100 °C	44.0	
P_D	Power Dissipation $R_{\theta JA}$ (Notes 1, 2)		T_A = 25 °C	5.0	W
			T_A = 100 °C	2.5	
I_{DM}	Pulsed Drain Current	T_A = 25 °C, t_p = 10 μs		900	A
T_J, T_{stg}	Operating Junction and Storage Temperature Range			−55 to +175	°C
I_S	Source Current (Body Diode)			245.5	A
E_{AS}	Single Pulse Drain-to-Source Avalanche Energy ($I_{L(pk)}$ = 40 A)			1754	mJ
T_L	Lead Temperature for Soldering Purposes (1/8″ from case for 10 s)			260	°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

THERMAL RESISTANCE MAXIMUM RATINGS

Parameter	Symbol	Value	Unit
Junction-to-Case - Steady State	$R_{\theta JC}$	0.5	°C/W
Junction-to-Ambient - Steady State (Note 2)	$R_{\theta JA}$	30	

1. The entire application environment impacts the thermal resistance values shown, they are not constants and are only valid for the particular conditions noted.
2. Surface-mounted on FR4 board using a 650 mm^2, 2 oz. Cu pad.
3. Maximum current for pulses as long as 1 second is higher but is dependent on pulse duration and duty cycle.



N-CHANNEL MOSFET

MARKING DIAGRAM



A = Assembly Location
WL = Wafer Lot Code
Y = Year Code
WW = Work Week Code

ORDERING INFORMATION

See detailed ordering, marking and shipping information in the package dimensions section on page 5 of this data sheet.

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ELECTRICAL CHARACTERISTICS (T_J = 25 °C unless otherwise specified)

Symbol	Parameter	Test Condition		Min	Typ	Max	Unit
OFF CHARACTERISTICS							
$V_{(BR)DSS}$	Drain-to-Source Breakdown Voltage	V_{GS} = 0 V, I_D = 250 μA		60	–	–	V
$V_{(BR)DSS}/T_J$	Drain-to-Source Breakdown Voltage Temperature Coefficient	I_D = 250 μA, ref to 25 °C		–	16.8	–	mV/°C
I_{DSS}	Zero Gate Voltage Drain Current	V_{GS} = 0 V, V_{DS} = 60 V	T_J = 25 °C	–	–	10	μA
			T_J = 125 °C	–	–	250	
I_{GSS}	Gate-to-Source Leakage Current	V_{DS} = 0 V, V_{GS} = 20 V		–	–	100	nA
ON CHARACTERISTICS (Note 4)							
$V_{GS(TH)}$	Gate Threshold Voltage	V_{GS} = V_{DS}, I_D = 250 μA		1.0	–	2.5	V
$V_{GS(TH)}/T_J$	Threshold Temperature Coefficient	I_D = 250 μA, ref to 25 °C		–	−5.63	–	mV/°C
$R_{DS(on)}$	Drain-to-Source On Resistance	V_{GS} = 10 V	I_D = 50 A	–	0.52	0.68	mΩ
		V_{GS} = 4.5 V	I_D = 50 A	–	0.69	0.90	
g_{FS}	Forward Transconductance	V_{DS} =15 V, I_D = 50 A		–	310	–	S
CHARGES, CAPACITANCES & GATE RESISTANCE							
C_{ISS}	Input Capacitance	V_{GS} = 0 V, f = 1 MHz, V_{DS} = 25 V		–	16200	–	pF
C_{OSS}	Output Capacitance			–	8490	–	
C_{RSS}	Reverse Transfer Capacitance			–	270	–	
$Q_{G(TOT)}$	Total Gate Charge	V_{GS} = 4.5 V, V_{DS} = 30 V; I_D = 50 A		–	103	–	nC
$Q_{G(TOT)}$	Total Gate Charge	V_{GS} = 10 V, V_{DS} = 30 V; I_D = 50 A		–	225	–	
$Q_{G(TH)}$	Threshold Gate Charge	V_{GS} = 10 V, V_{DS} = 30 V; I_D = 50 A		–	21.6	–	
Q_{GS}	Gate-to-Source Charge			–	36.5	–	
Q_{GD}	Gate-to-Drain Charge			–	20.7	–	
V_{GP}	Plateau Voltage			–	2.46	–	V
SWITCHING CHARACTERISTICS (Note 5)							
$t_{d(ON)}$	Turn-On Delay Time	V_{GS} = 10 V, V_{DS} = 30 V, I_D = 50 A, R_G = 2.5 Ω		–	35.3	–	ns
t_r	Rise Time			–	26.3	–	
$t_{d(OFF)}$	Turn-Off Delay Time			–	263	–	
t_f	Fall Time			–	60.7	–	
DRAIN-SOURCE DIODE CHARACTERISTICS							
V_{SD}	Forward Diode Voltage	V_{GS} = 0 V, I_S = 50 A	T_J = 25 °C	–	0.67	1.2	V
			T_J = 125 °C	–	0.59	–	
t_{RR}	Reverse Recovery Time	V_{GS} = 0 V, dIS/dt = 100 A/μs, I_S = 50 A		–	115	–	ns
t_a	Charge Time			–	70	–	
t_b	Discharge Time			–	45	–	
Q_{RR}	Reverse Recovery Charge			–	307	–	nC

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

4. Pulse Test: pulse width ≤ 300 μs, duty cycle ≤ 2%.
5. Switching characteristics are independent of operating junction temperatures.

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TYPICAL CHARACTERISTICS

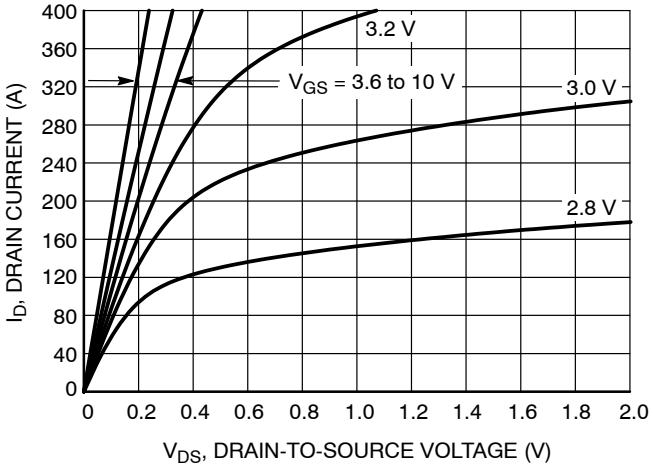


Figure 1. On-Region Characteristics

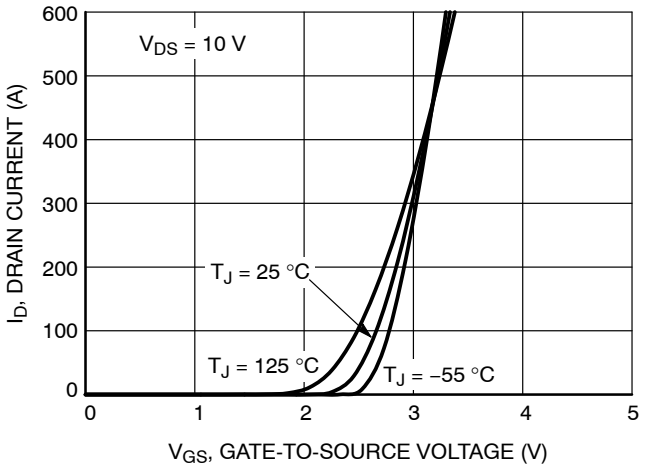


Figure 2. Transfer Characteristics

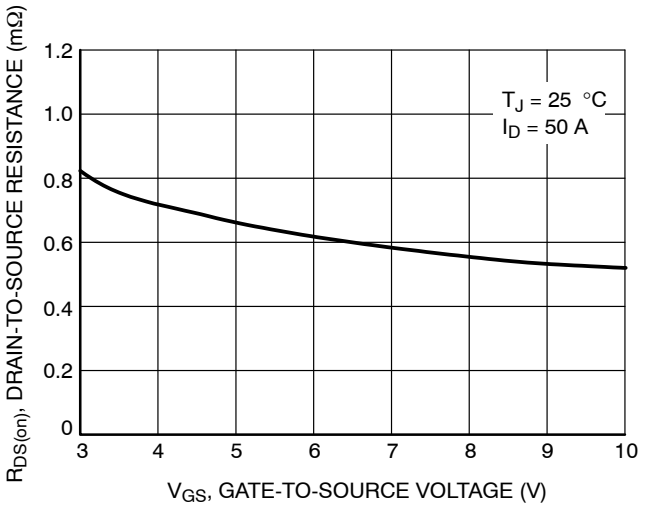


Figure 3. On-Resistance vs. Gate-to-Source Voltage

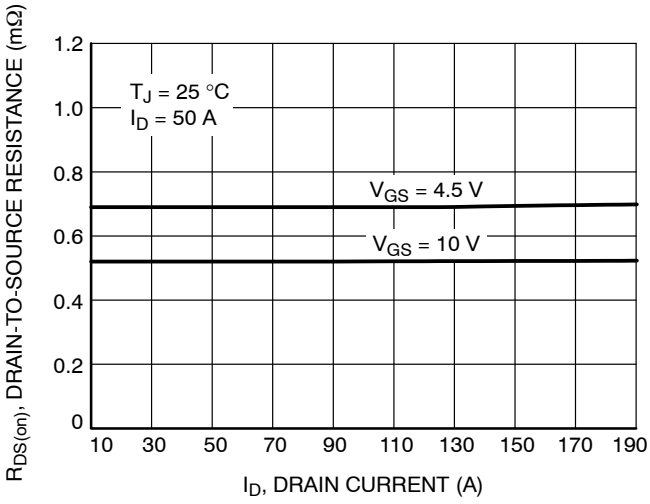


Figure 4. On-Resistance vs. Drain Current and Gate Voltage

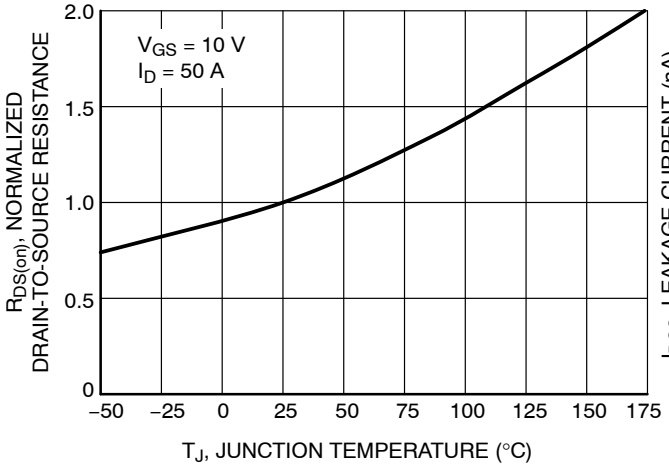


Figure 5. On-Resistance Variation with Temperature

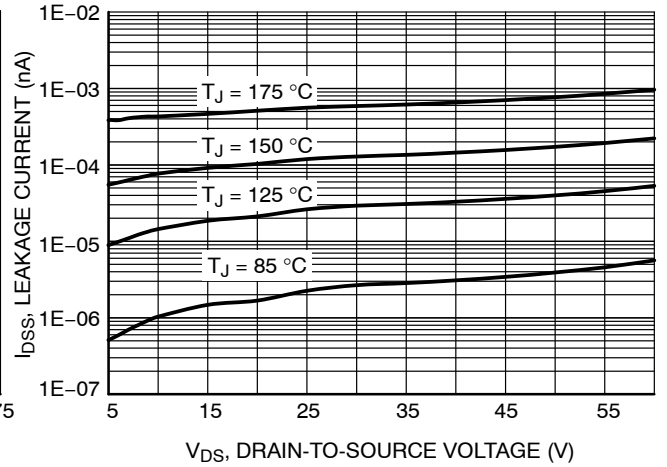


Figure 6. Drain-to-Source Leakage Current vs. Voltage

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TYPICAL CHARACTERISTICS (continued)

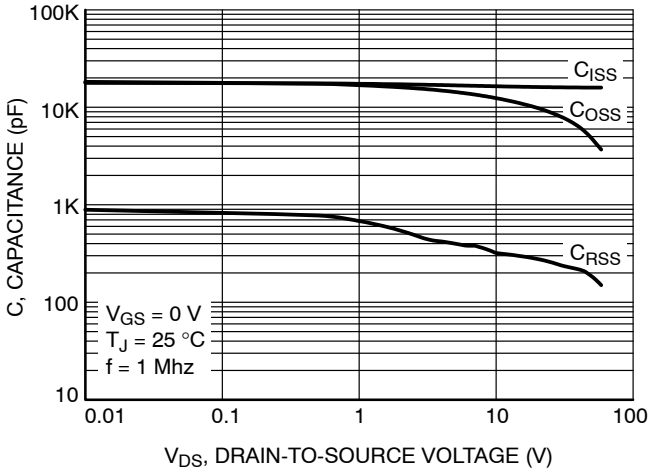


Figure 7. Capacitance Variation

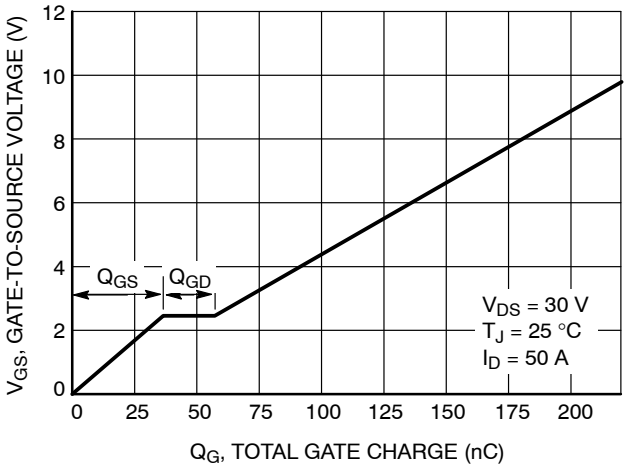


Figure 8. Gate-to-Source Voltage vs. Total Charge

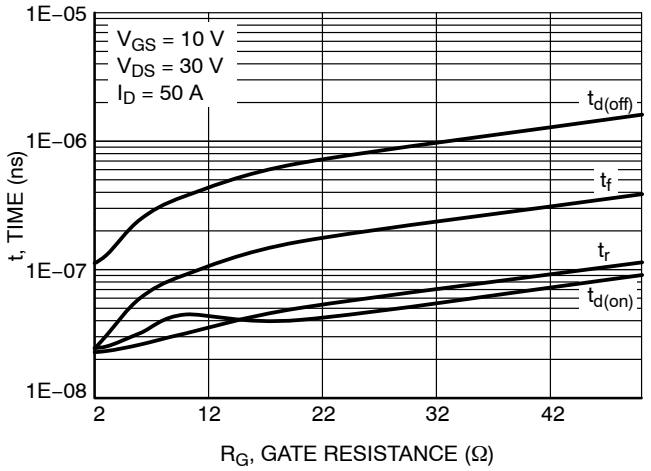


Figure 9. Resistive Switching Time Variation vs. Gate Resistance

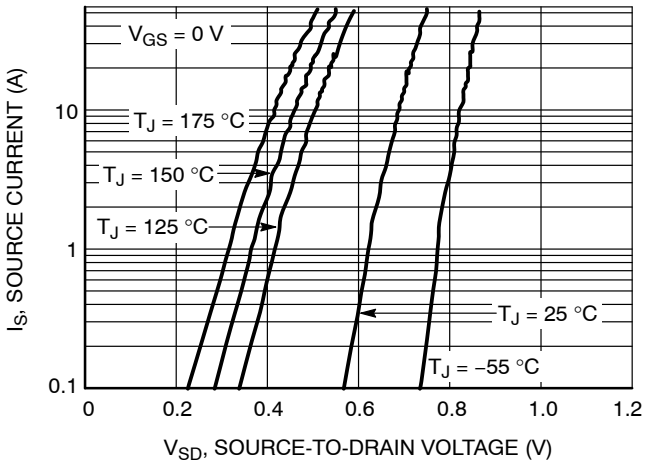


Figure 10. Diode Forward Voltage vs. Current

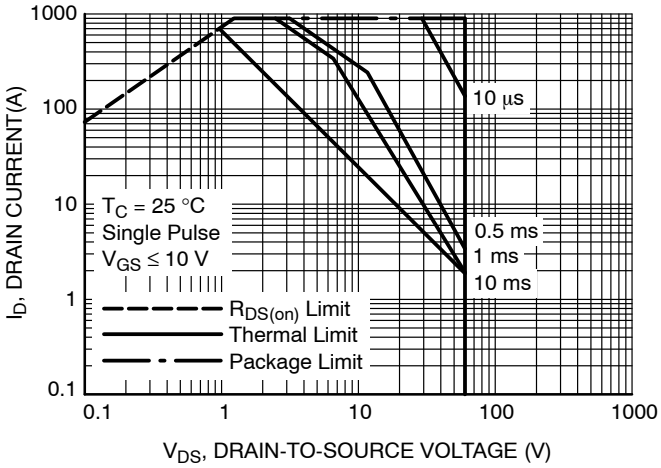


Figure 11. Maximum Rated Forward Biased Safe Operating Area

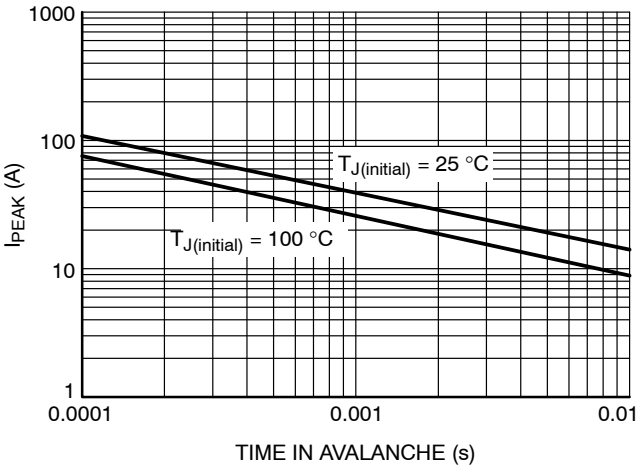


Figure 12. Maximum Drain Current vs. Time in Avalanche

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TYPICAL CHARACTERISTICS (continued)

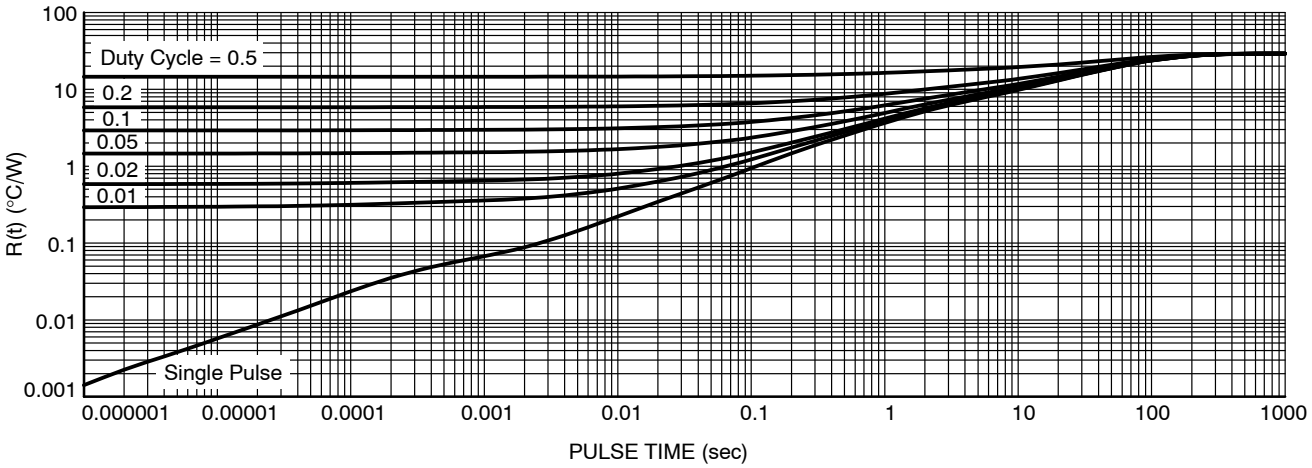


Figure 13. Thermal Characteristics

DEVICE ORDERING INFORMATION

Device	Marking	Package	Shipping†
NVMTS0D7N06CLTXG	0D7N06CL	TDFNW8 (Pb-Free)	3000 / Tape & Reel
NVMTS0D7N06CLETXG	0D7N06CL	TDFNW8 (Pb-Free)	3000 / Tape & Reel

† For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

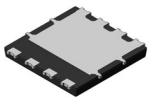
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REVISION HISTORY

Revision	Description of Changes	Date
4	Rebranded the Data Sheet to **onsemi** format.	1/23/2026
5	OPN NVMTS0D7N06CLETXG added to the data sheet.	7/13/2026

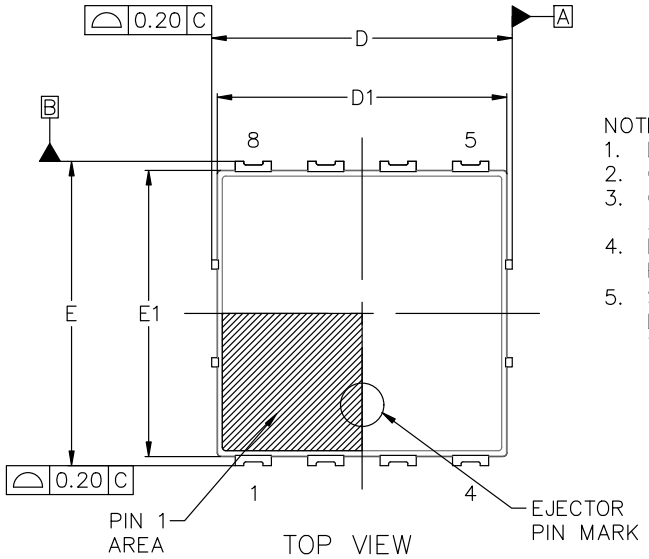
This document has undergone updates prior to the inclusion of this revision history table. The changes tracked here only reflect updates made on the noted approval dates.

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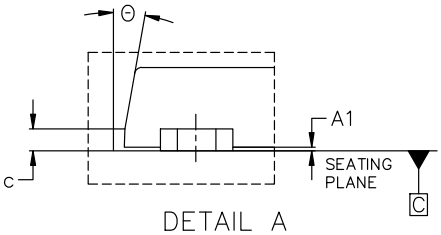
TDFNW−8 8.30x8.40x1.10, 2.00P
CASE 507AP
ISSUE F

DATE 26 OCT 2026

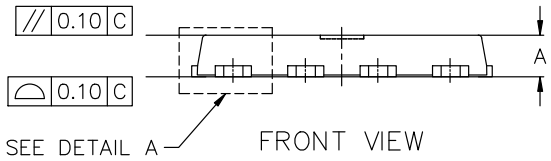


TOP VIEW
SCALE 1:1

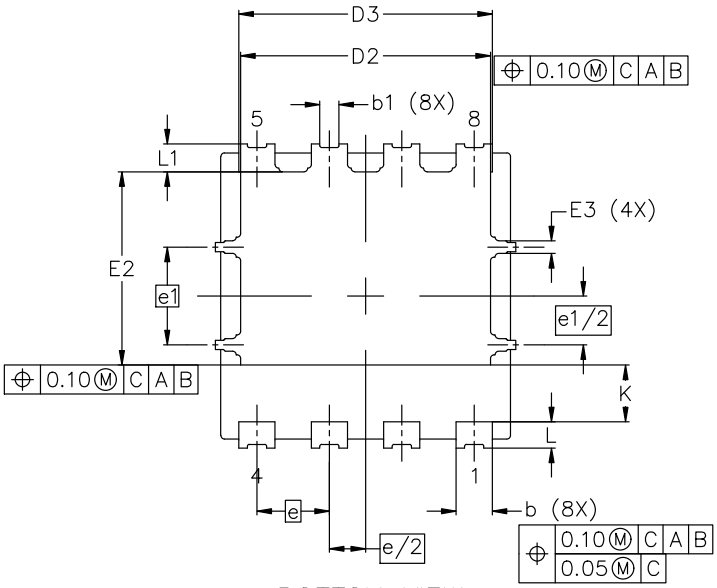
NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 2009.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. COPLANARITY APPLIES TO THE EXPOSED PADS AS WELL AS THE TERMINALS.
4. DIMENSIONS D1 AND E1 DO NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR GATE BURRS.
5. SEATING PLANE IS DEFINED BY THE TERMINALS. "A1" IS DEFINED AS THE DISTANCE FROM THE SEATING PLANE TO THE LOWEST POINT ON THE PACKAGE BODY.



DETAIL A
SCALE 2:1



FRONT VIEW
SCALE 1:1



BOTTOM VIEW
SCALE 1:1

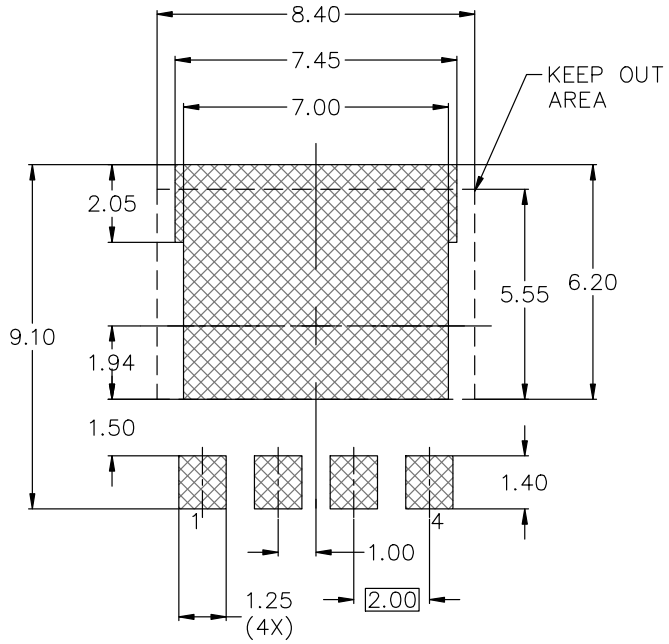
DIM	MILLIMETERS		
	MIN.	NOM.	MAX.
A	1.00	1.10	1.20
A1	0.00	0.02	0.05
b	0.90	1.00	1.10
b1	0.35	0.45	0.55
c	0.23	0.28	0.33
D	8.20	8.30	8.40
D1	7.90	8.00	8.10
D2	6.80	6.90	7.00
D3	6.90	7.00	7.10
E	8.30	8.40	8.50
E1	7.80	7.90	8.00
E2	5.24	5.34	5.44
E3	0.25	0.35	0.45
e	2.00 BSC		
e/2	1.00 BSC		
e1	2.70 BSC		
e1/2	1.35 BSC		
K	1.50	1.57	1.70
L	0.64	0.74	0.84
L1	0.67	0.77	0.87
Θ	0°	−−−	12°

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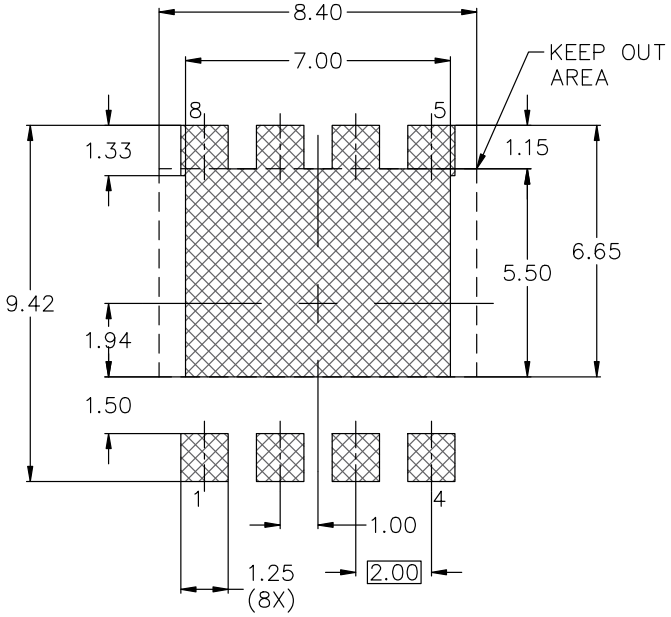
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CASE 507AP
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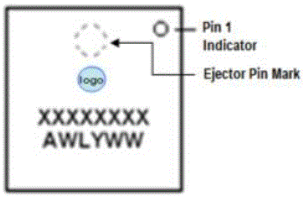


UNIVERSAL LAND PATTERN



RECOMMENDED MOUNTING FOOTPRINT
*FOR ADDITIONAL INFORMATION ON OUR Pb−FREE STRATEGY AND SOLDERING DETAILS, PLEASE DOWNLOAD THE onsemi SOLDERING AND MOUNTING TECHNIQUES REFERENCE MANUAL, SOLDERRM/D.

GENERIC MARKING DIAGRAM*



XXXX = Specific Device Code
A = Assembly Location
WL = Wafer Lot Code
Y = Year Code
WW = Work Week Code

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, “G” or microdot “ ▪”, may or may not be present. Some products may not follow the Generic Marking.

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