# MOSFET - Power, Single P-Channel, SOT-23

## -60 V, 230 mΩ, -1.1 A

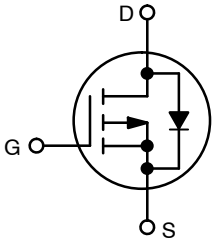
# NVR5124PL

| $V_{(BR)DSS}$ | $R_{DS(on)}$ MAX | $I_D$ MAX |
|---|---|---|
| −60 V | 230 mΩ @ −10 V | −1.1 A |
| | 365 mΩ @ −4.5 V | |

**Features**

- Trench Technology
- NVR Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC−Q101 Qualified and PPAP Capable
- These Devices are Pb−Free and are RoHS Compliant

**P−Channel**




**MAXIMUM RATINGS** ($T_J$ = 25°C unless otherwise noted)

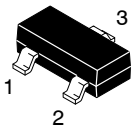
| Parameter | | | Symbol | Value | Unit |
|---|---|---|---|---|---|
| Drain−to−Source Voltage | | | $V_{DSS}$ | −60 | V |
| Gate−to−Source Voltage | | | $V_{GS}$ | ±20 | V |
| Continuous Drain Current $R_{\theta JA}$ (Notes 1, 2, 3) | Steady State | $T_A$ = 25°C | $I_D$ | −1.1 | A |
| | | $T_A$ = 100°C | | −0.67 | |
| Power Dissipation $R_{\theta JA}$ (Notes 1, 2) | | $T_A$ = 25°C | $P_D$ | 0.47 | W |
| | | $T_A$ = 100°C | | 0.19 | |
| Pulsed Drain Current | $T_A$ = 25°C, $t_p$ = 10 μs | | $I_{DM}$ | 25 | A |
| Operating Junction and Storage Temperature Range | | | $T_J$, $T_{stg}$ | −55 to +150 | °C |
| Source Current (Body Diode) | | | $I_S$ | −0.6 | A |
| Lead Temperature for Soldering Purposes (1/8″ from case for 10 s) | | | $T_L$ | 260 | °C |

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

**THERMAL RESISTANCE MAXIMUM RATINGS** (Note 1)

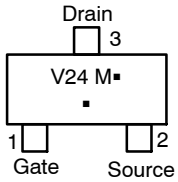
| Parameter | Symbol | Value | Unit |
|---|---|---|---|
| Junction−to−Ambient − Steady State (Note 2) | $R_{\theta JA}$ | 268 | °C/W |

1. The entire application environment impacts the thermal resistance values shown, they are not constants and are only valid for the particular conditions noted.
2. Surface−mounted on FR4 board using a 650 $mm^2$, 2 oz. Cu pad.
3. Continuous DC current rating. Maximum current for pulses as long as 1 second is higher but is dependent on pulse duration and duty cycle.




**SOT−23**
**CASE 318**
**STYLE 21**

**MARKING DIAGRAM/ PIN ASSIGNMENT**




V24 = Device Code
M = Date Code*
▪ = Pb−Free Package

(Note: Microdot may be in either location)

*Date Code orientation may vary depending upon manufacturing location.

**ORDERING INFORMATION**

| Device | Package | Shipping† |
|---|---|---|
| NVR5124PLT1G | SOT−23 (Pb−Free) | 3000 / Tape & Reel |

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

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**ELECTRICAL CHARACTERISTICS** ($T_J$ = 25°C unless otherwise noted)

| Parameter | Symbol | Test Condition | | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|---|
| **OFF CHARACTERISTICS** | | | | | | | |
| Drain−to−Source Breakdown Voltage | $V_{(BR)DSS}$ | $V_{GS}$ = 0 V, $I_D$ = −250 μA | | −60 | – | – | V |
| Zero Gate Voltage Drain Current | $I_{DSS}$ | $V_{GS}$ = 0 V, $V_{DS}$ = −60 V | $T_J$ = 25°C | – | – | −1.0 | μA |
| | | | $T_J$ = 125°C | – | – | −10 | |
| Gate−to−Source Leakage Current | $I_{GSS}$ | $V_{DS}$ = 0 V, $V_{GS}$ = ±20 V | | – | – | ±100 | nA |
| **ON CHARACTERISTICS** (Note 4) | | | | | | | |
| Gate Threshold Voltage | $V_{GS(TH)}$ | $V_{GS}$ = $V_{DS}$, $I_D$ = −250 μA | | −1.5 | – | −2.5 | V |
| Drain−to−Source On Resistance | $R_{DS(on)}$ | $V_{GS}$ = −10 V, $I_D$ = −3 A | | – | 183 | 230 | mΩ |
| | | $V_{GS}$ = −4.5 V, $I_D$ = −3 A | | – | 280 | 365 | |
| Forward Transconductance | $g_{FS}$ | $V_{DS}$ = −15 V, $I_D$ = −5 A | | 4 | – | – | S |
| **CHARGES AND CAPACITANCES** | | | | | | | |
| Input Capacitance | $C_{iss}$ | $V_{GS}$ = 0 V, f = 1.0 MHz, $V_{DS}$ = −25 V | | – | 240 | – | pF |
| Output Capacitance | $C_{oss}$ | | | – | 27.6 | – | |
| Reverse Transfer Capacitance | $C_{rss}$ | | | – | 18.5 | – | |
| Total Gate Charge | $Q_{G(TOT)}$ | $V_{GS}$ = −4.5 V, $V_{DS}$ = −48 V, $I_D$ = −3 A | | – | 2.3 | – | nC |
| Threshold Gate Charge | $Q_{G(TH)}$ | | | – | 0.5 | – | |
| Gate−to−Source Charge | $Q_{GS}$ | | | – | 0.9 | – | |
| Gate−to−Drain Charge | $Q_{GD}$ | | | – | 1.0 | – | |
| Total Gate Charge | $Q_{G(TOT)}$ | $V_{GS}$ = −10 V, $V_{DS}$ = −48 V, $I_D$ = −3 A | | – | 4.3 | – | |
| **SWITCHING CHARACTERISTICS** (Note 5) | | | | | | | |
| Turn−On Delay Time | $t_{d(on)}$ | $V_{GS}$ = −4.5 V, $V_{DS}$ = −48 V, $I_D$ = −3 A, $R_G$ = 2.5 Ω | | – | 6.6 | – | ns |
| Rise Time | $t_r$ | | | – | 10.6 | – | |
| Turn−Off Delay Time | $t_{d(off)}$ | | | – | 12.2 | – | |
| Fall Time | $t_f$ | | | – | 3.5 | – | |
| **DRAIN−SOURCE DIODE CHARACTERISTICS** | | | | | | | |
| Forward Diode Voltage | $V_{SD}$ | $V_{GS}$ = 0 V, $I_S$ = −3 A | $T_J$ = 25°C | – | −0.88 | −1.0 | V |
| | | | $T_J$ = 125°C | – | −0.76 | – | |
| Reverse Recovery Time | $t_{RR}$ | $V_{GS}$ = 0 V, $dI_S/dt$ = 100 A/μs, $I_S$ = −3 A | | – | 15 | – | ns |
| Charge Time | $t_a$ | | | – | 13 | – | |
| Discharge Time | $t_b$ | | | – | 2.4 | – | |
| Reverse Recovery Charge | $Q_{RR}$ | | | – | 10 | – | nC |

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

4. Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2%.
5. Switching characteristics are independent of operating junction temperatures.

## TYPICAL CHARACTERISTICS

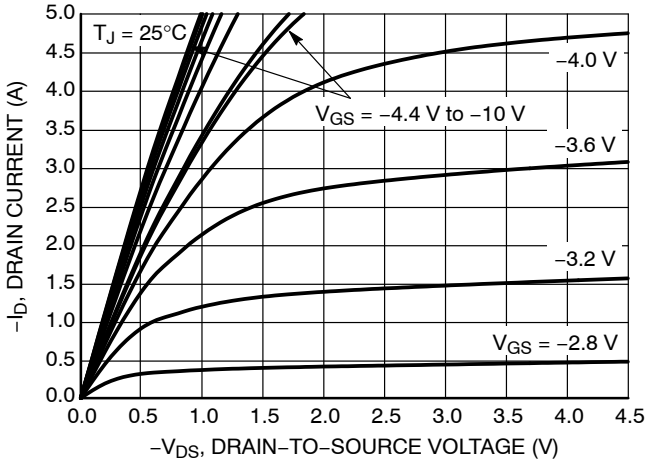



**Figure 1. On−Region Characteristics**

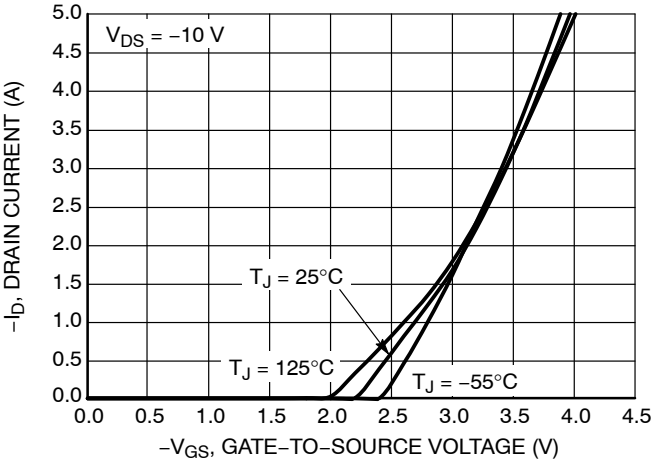



**Figure 2. Transfer Characteristics**

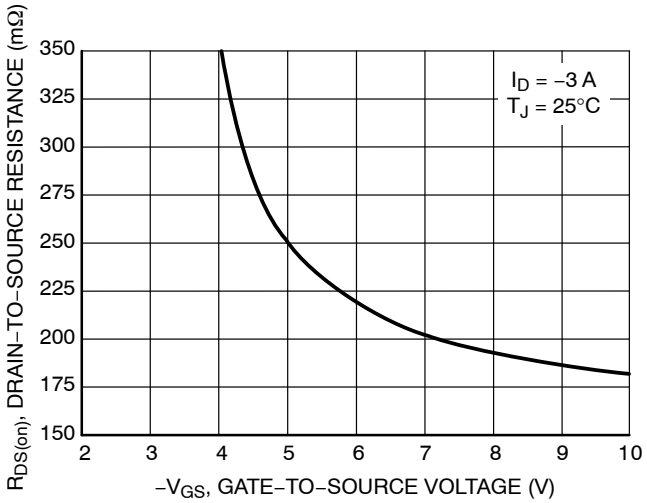



**Figure 3. On−Resistance vs. Gate−to−Source Voltage**

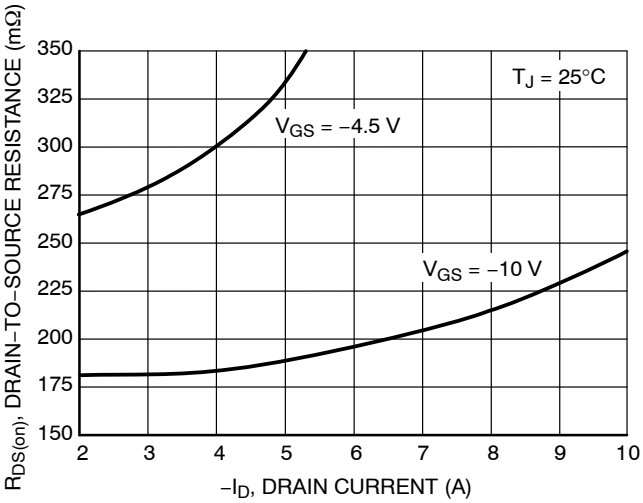



**Figure 4. On−Resistance vs. Drain Current and Gate Voltage**

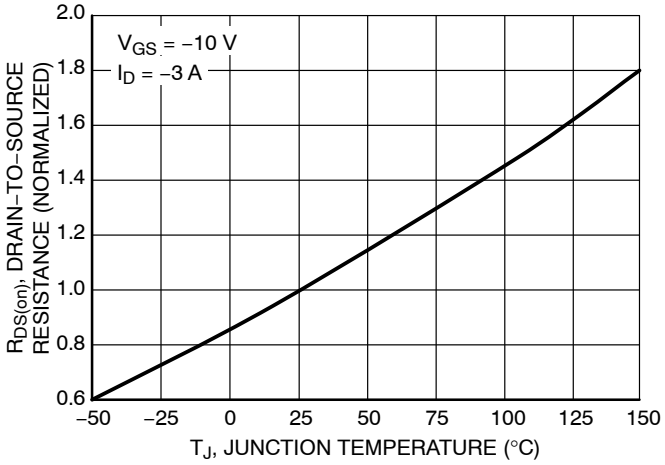



**Figure 5. On−Resistance Variation with Temperature**

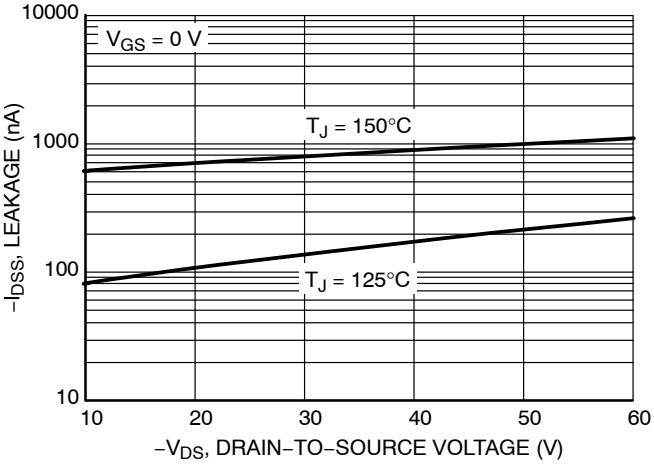



**Figure 6. Drain−to−Source Leakage Current vs. Voltage**

## TYPICAL CHARACTERISTICS

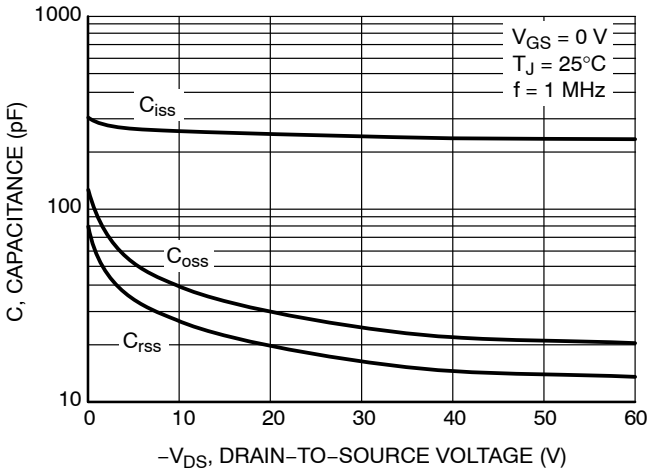



**Figure 7. Capacitance Variation**

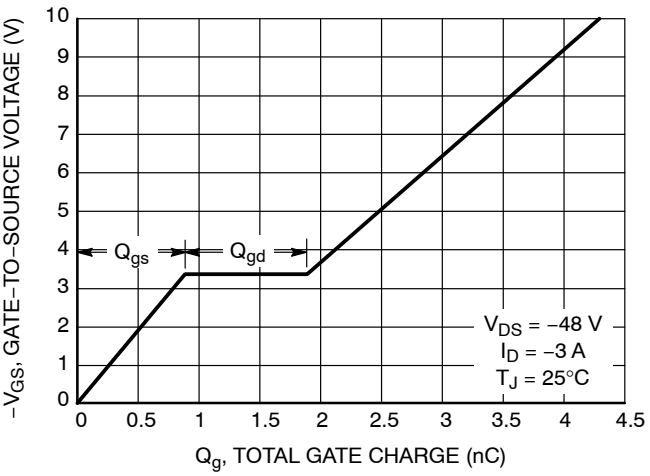



**Figure 8. Gate−to−Source Voltage vs. Total Charge**

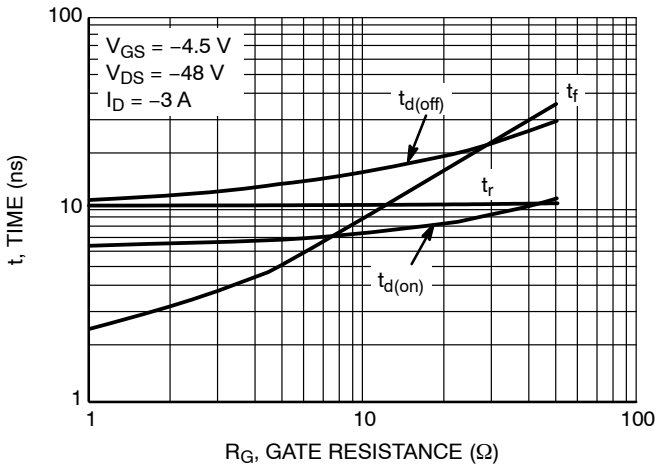



**Figure 9. Resistive Switching Time Variation vs. Gate Resistance**

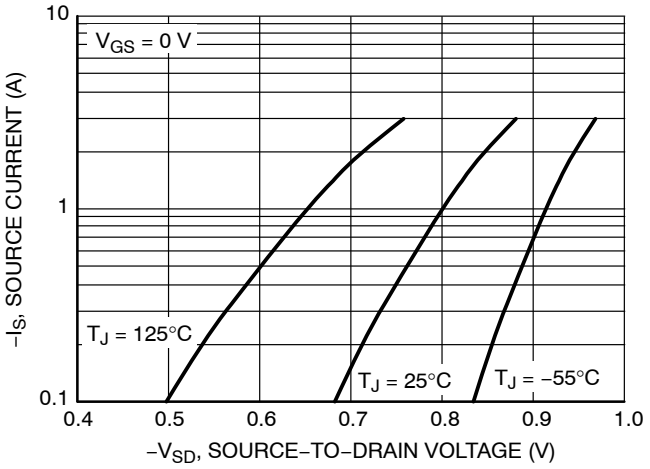



**Figure 11. Diode Forward Voltage vs. Current**

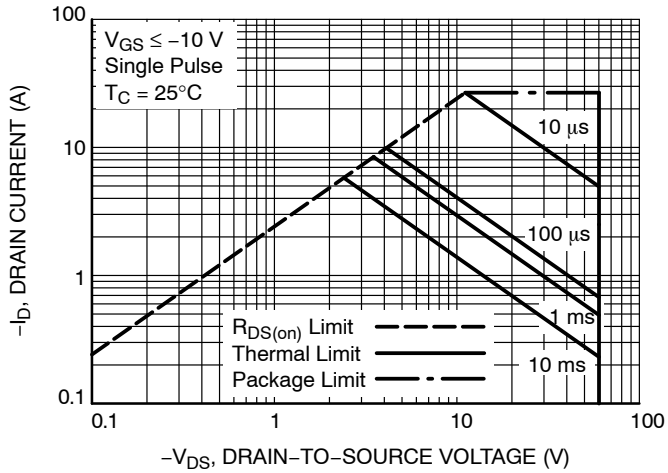



**Figure 10. Maximum Rated Forward Biased Safe Operating Area**

## TYPICAL CHARACTERISTICS

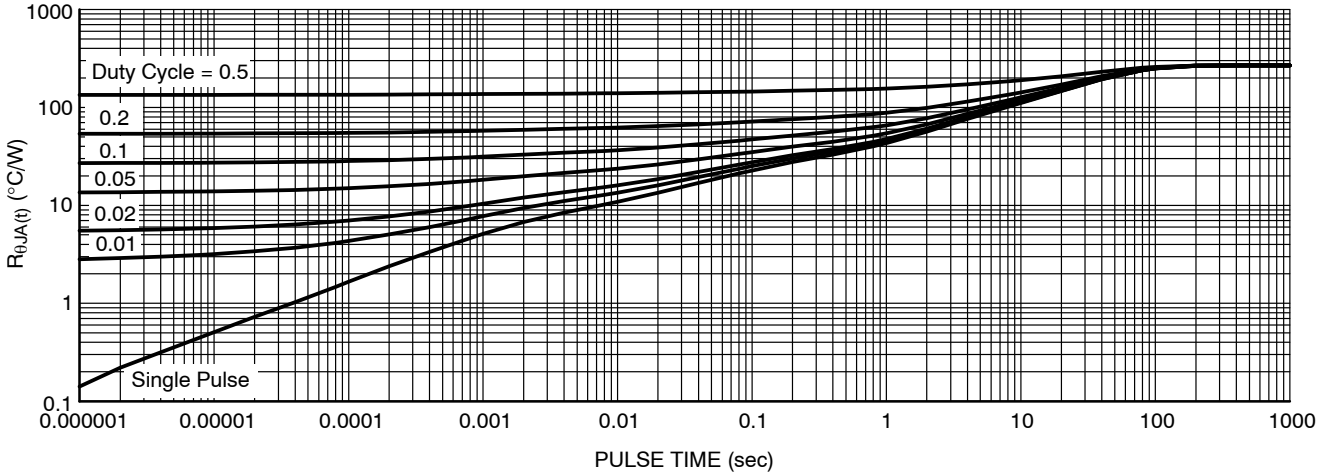
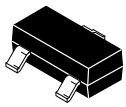


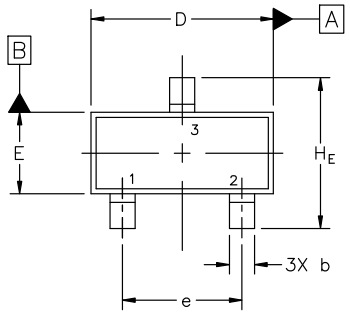

**Figure 12. Thermal Response**



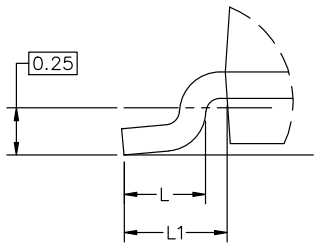
**SCALE 4:1**

**SOT−23 (TO−236) 2.90x1.30x1.00 1.90P**
CASE 318
ISSUE AU

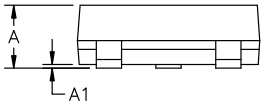
DATE 14 AUG 2024



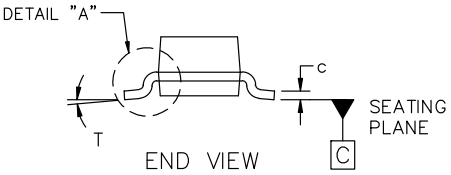

TOP VIEW




DETAIL "A"
Scale 3:1




SIDE VIEW

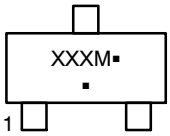



END VIEW

| MILLIMETERS | | | |
|---|---|---|---|
| DIM | MIN | NOM | MAX |
| A | 0.89 | 1.00 | 1.11 |
| A1 | 0.01 | 0.06 | 0.10 |
| b | 0.37 | 0.44 | 0.50 |
| c | 0.08 | 0.14 | 0.20 |
| D | 2.80 | 2.90 | 3.04 |
| E | 1.20 | 1.30 | 1.40 |
| e | 1.78 | 1.90 | 2.04 |
| L | 0.30 | 0.43 | 0.55 |
| L1 | 0.35 | 0.54 | 0.69 |
| $H_E$ | 2.10 | 2.40 | 2.64 |
| T | 0° | −−− | 10° |

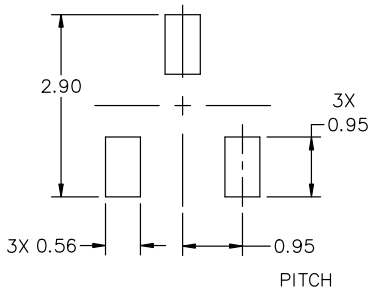
NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 2018.
2. CONTROLLING DIMENSIONS: MILLIMETERS.
3. MAXIMUM LEAD THICKNESS INCLUDES LEAD FINISH. MINIMUM LEAD THICKNESS IS THE MINIMUM THICKNESS OF THE BASE MATERIAL.
4. DIMENSIONS D AND E DO NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR GATE BURRS.

**GENERIC**
**MARKING DIAGRAM***




XXX = Specific Device Code
M = Date Code
▪ = Pb−Free Package

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, "G" or microdot "▪", may or may not be present. Some products may not follow the Generic Marking.




RECOMMENDED
MOUNTING FOOTPRINT

* For additional information on our Pb−Free strategy and soldering details, please download the onsemi Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

**STYLES ON PAGE 2**

| | | | |
|---|---|---|---|
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**SOT−23 (TO−236) 2.90x1.30x1.00 1.90P**
CASE 318
ISSUE AU

DATE 14 AUG 2024

STYLE 1 THRU 5:
CANCELLED

STYLE 6:
PIN 1. BASE
2. EMITTER
3. COLLECTOR

STYLE 7:
PIN 1. EMITTER
2. BASE
3. COLLECTOR

STYLE 8:
PIN 1. ANODE
2. NO CONNECTION
3. CATHODE

STYLE 9:
PIN 1. ANODE
2. ANODE
3. CATHODE

STYLE 10:
PIN 1. DRAIN
2. SOURCE
3. GATE

STYLE 11:
PIN 1. ANODE
2. CATHODE
3. CATHODE−ANODE

STYLE 12:
PIN 1. CATHODE
2. CATHODE
3. ANODE

STYLE 13:
PIN 1. SOURCE
2. DRAIN
3. GATE

STYLE 14:
PIN 1. CATHODE
2. GATE
3. ANODE

STYLE 15:
PIN 1. GATE
2. CATHODE
3. ANODE

STYLE 16:
PIN 1. ANODE
2. CATHODE
3. CATHODE

STYLE 17:
PIN 1. NO CONNECTION
2. ANODE
3. CATHODE

STYLE 18:
PIN 1. NO CONNECTION
2. CATHODE
3. ANODE

STYLE 19:
PIN 1. CATHODE
2. ANODE
3. CATHODE−ANODE

STYLE 20:
PIN 1. CATHODE
2. ANODE
3. GATE

STYLE 21:
PIN 1. GATE
2. SOURCE
3. DRAIN

STYLE 22:
PIN 1. RETURN
2. OUTPUT
3. INPUT

STYLE 23:
PIN 1. ANODE
2. ANODE
3. CATHODE

STYLE 24:
PIN 1. GATE
2. DRAIN
3. SOURCE

STYLE 25:
PIN 1. ANODE
2. CATHODE
3. GATE

STYLE 26:
PIN 1. CATHODE
2. ANODE
3. NO CONNECTION

STYLE 27:
PIN 1. CATHODE
2. CATHODE
3. CATHODE

STYLE 28:
PIN 1. ANODE
2. ANODE
3. ANODE




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